

# Vanguard Astra - Petascale ARM Platform for U.S. DOE/ASC Supercomputing



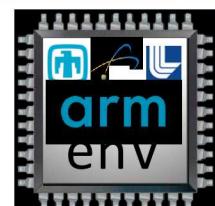
# VANGUARD

*PRESENTED BY*

Andrew J. Younge

PIs: James H. Laros III, Kevin Pedretti, Si Hammond

Sandia National Laboratories



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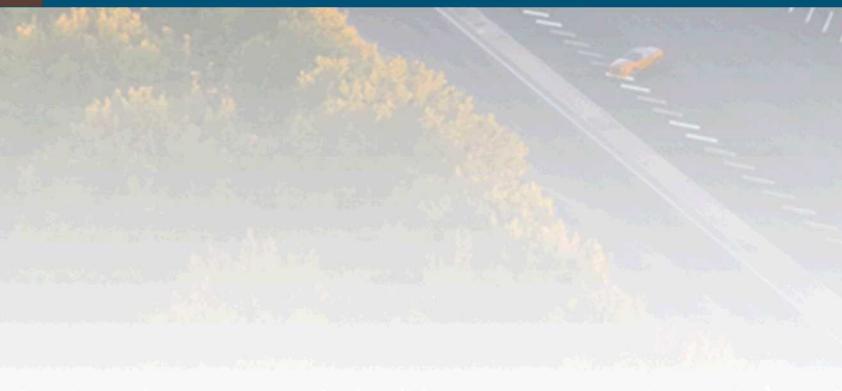
SAND2018-8216C

# Outline

- Overview of Vanguard
  - Prototype HPC Architectures
- Astra – Petascale ARM platform
- ATSE – Advanced Tri-lab Software Environment
- R&D Opportunities
- Conclusion



# Vanguard Overview



## Vanguard Program: Advanced Architecture Prototype Systems

- Prove viability of advanced technologies for NNSA integrated codes, at scale
- Expand the HPC-ecosystem by developing emerging unproven technologies
  - Is it viable for future ATS/CTS platforms?
  - Increase technology AND integrator choices
- Buy down risk and increase technology and vendor choices for future platforms
  - Ability to accept higher risk allows for more/faster technology advancement
  - Lowers/eliminates mission risk and significantly reduces investment
- Jointly address hardware and software challenges
- First prototype platform targeting ARM

# Where Vanguard Fits



## Test Beds

- Small testbeds (~10-100 nodes)
- Breadth of architectures
- **Brave users**

## Vanguard

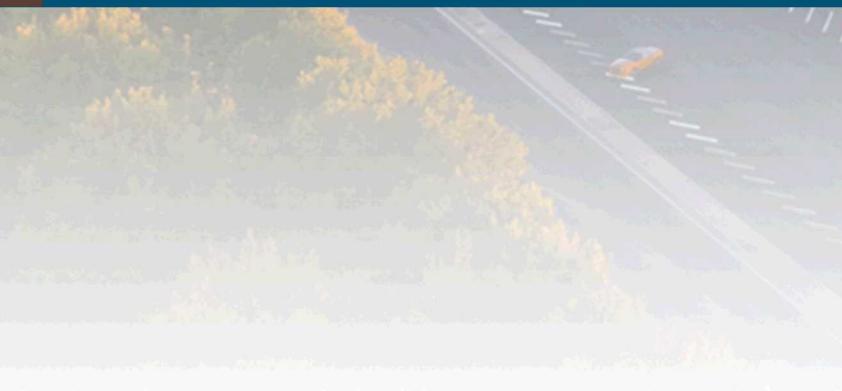
- Larger-scale experimental systems
- Focused efforts to mature new technologies
- Broader user-base
- **Demonstrate viability for production use**
- NNSA Tri-lab resource

## ATS/CTS Platforms

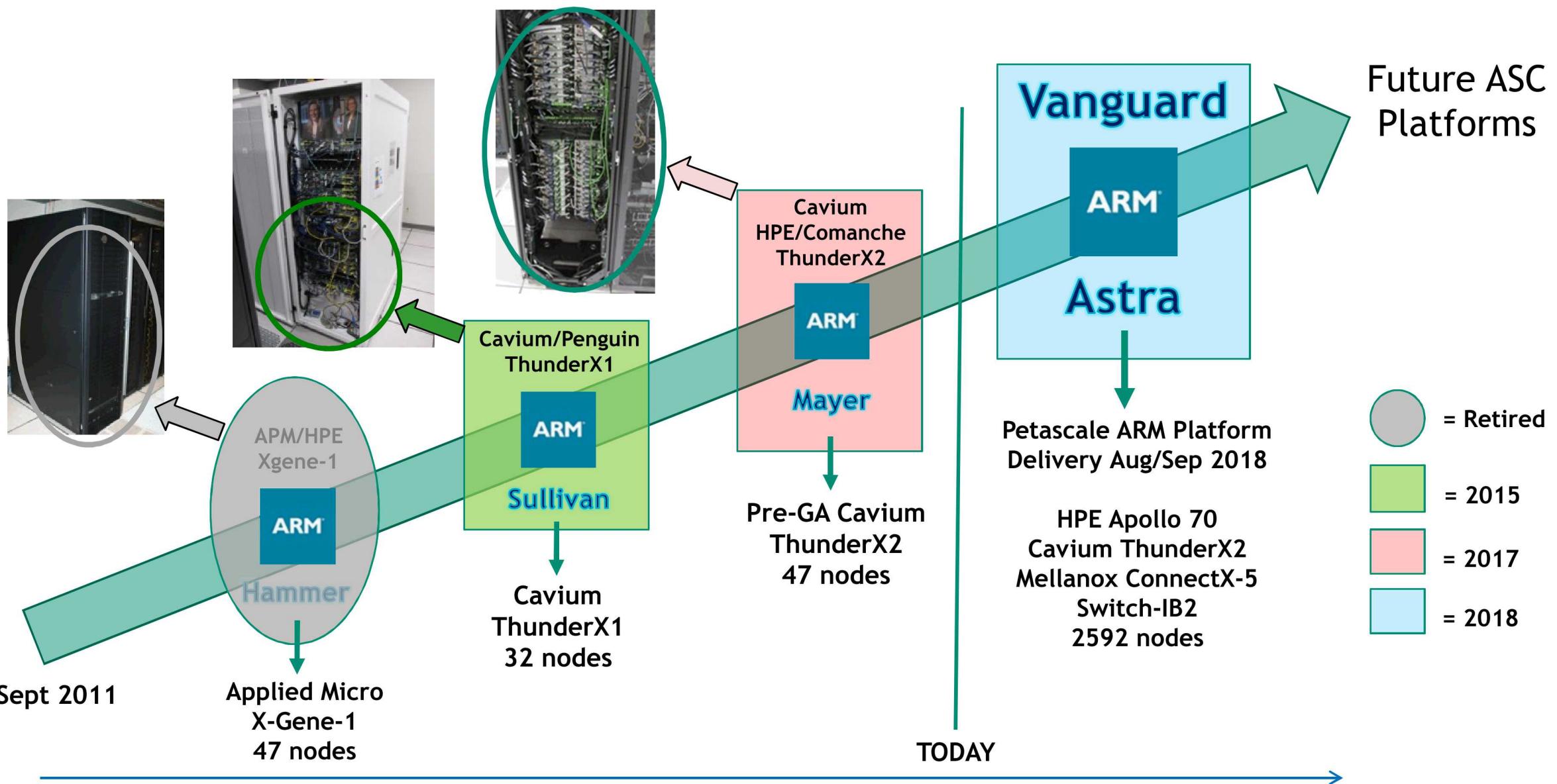
- Leadership-class systems (Petascale, Exascale, ...)
- Advanced technologies, sometimes first-of-kind
- Broad user-base
- **Production use**



# Vanguard Phase I:Astra

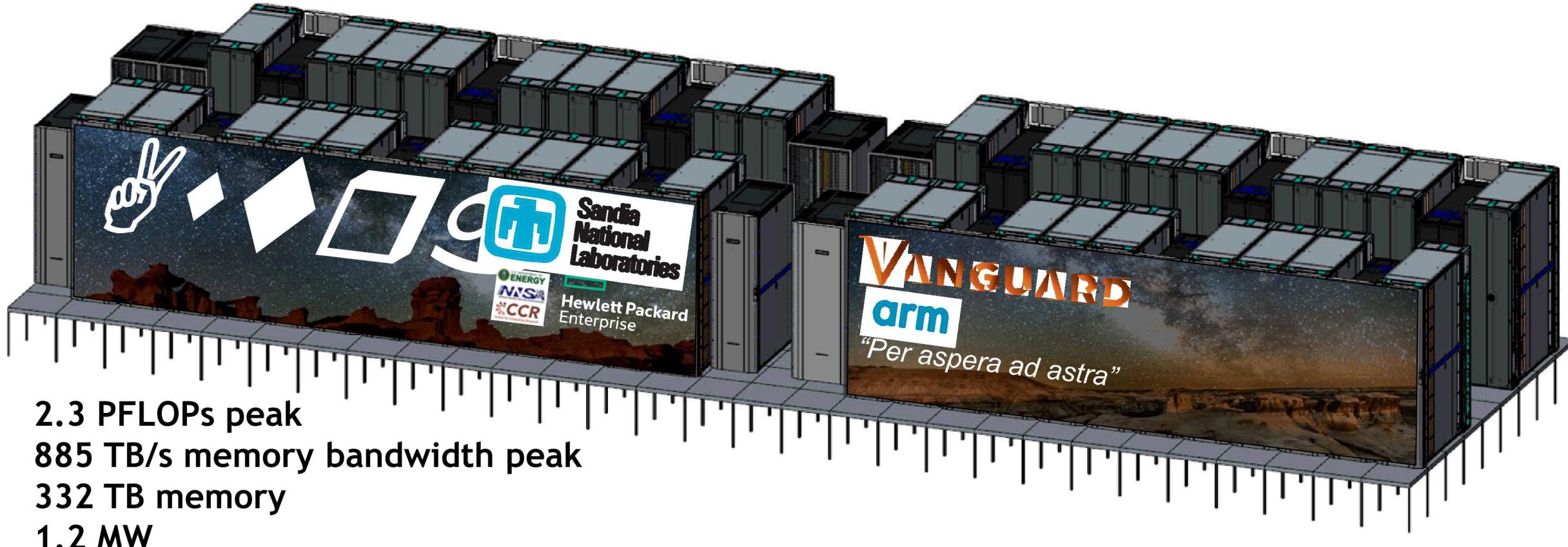


# Sandia's NNSA/ASC ARM Platforms



# *per aspera ad astra*

through difficulties to the stars



Demonstrate viability of ARM for U.S. DOE Supercomputing

# Vanguard-Astra Compute Node Building Block

Hewlett Packard  
Enterprise

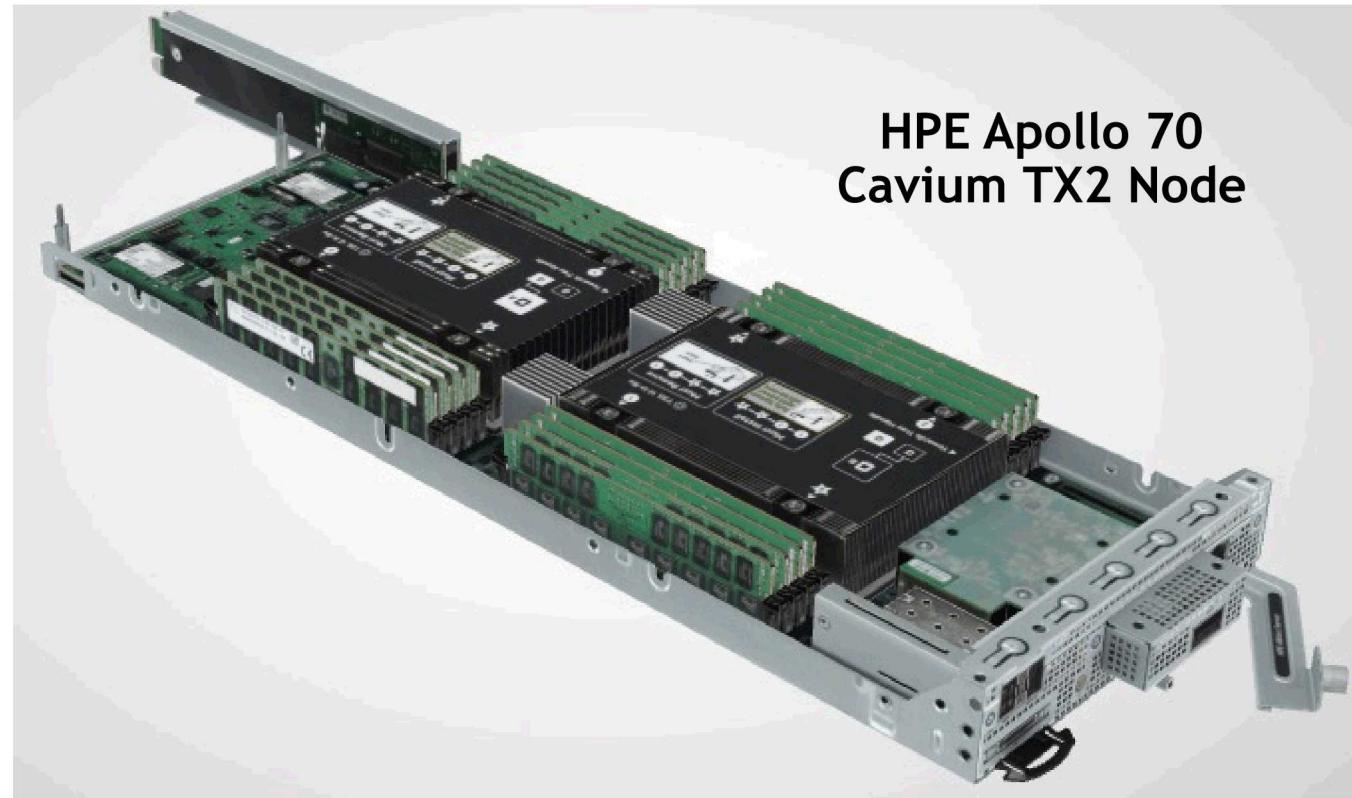
arm

CAVIUM

Mellanox  
TECHNOLOGIES

redhat

- Dual socket Cavium Thunder-X2
  - CN99xx
  - 28 cores @ 2.0 GHz
- 8 DDR4 controllers per socket
- One 8 GB DDR4-2666 dual-rank DIMM per controller
- Mellanox EDR InfiniBand ConnectX-5 VPI OCP
- Tri-Lab Operating System Stack based on RedHat 7.5+



# Vanguard-Astra Compute Node



8 DDR4 channels/socket, 1 DIMM/channel  
Each socket has its own PCIe x8 link to NIC

8 GB DDR4-2666 DR  
8 GB DDR4-2666 DR

Cavium Thunder-X2  
ARM v8.1  
28 cores @ 2.0 GHz

Cavium Thunder-X2  
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28 cores @ 2.0 GHz

8 GB DDR4-2666 DR  
8 GB DDR4-2666 DR

Management  
Ethernet  
1 Gbps

1 Gbps

PCIe Gen3

PCIe Gen3

Mellanox ConnectX-5  
OCP Network Interface

x8

x8

1 EDR link, 100 Gbps

# Vanguard-Astra System Packaging

HPE Apollo 70 Chassis: 4 nodes



36 compute racks  
(9 scalable units, each 4 racks)

2592 compute nodes  
(5184 TX2 processors)

3 IB spine switches  
(each 540-port)

HPE Apollo 70 Rack

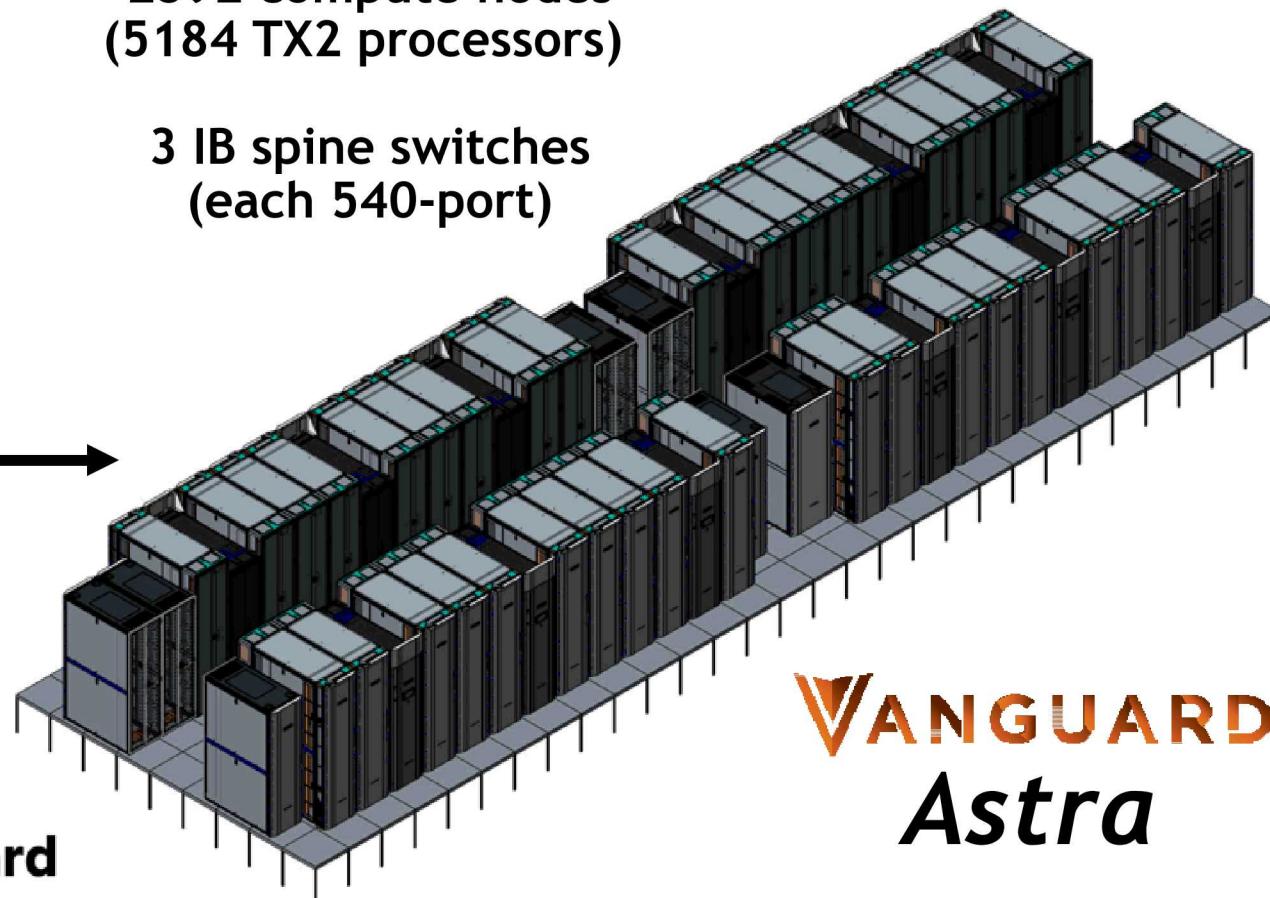
18 chassis/rack

72 nodes/rack

3 IB switches/rack  
(one 36-port switch per 6 chassis)



 **Hewlett Packard**  
Enterprise



# Vanguard-Astra Infrastructure

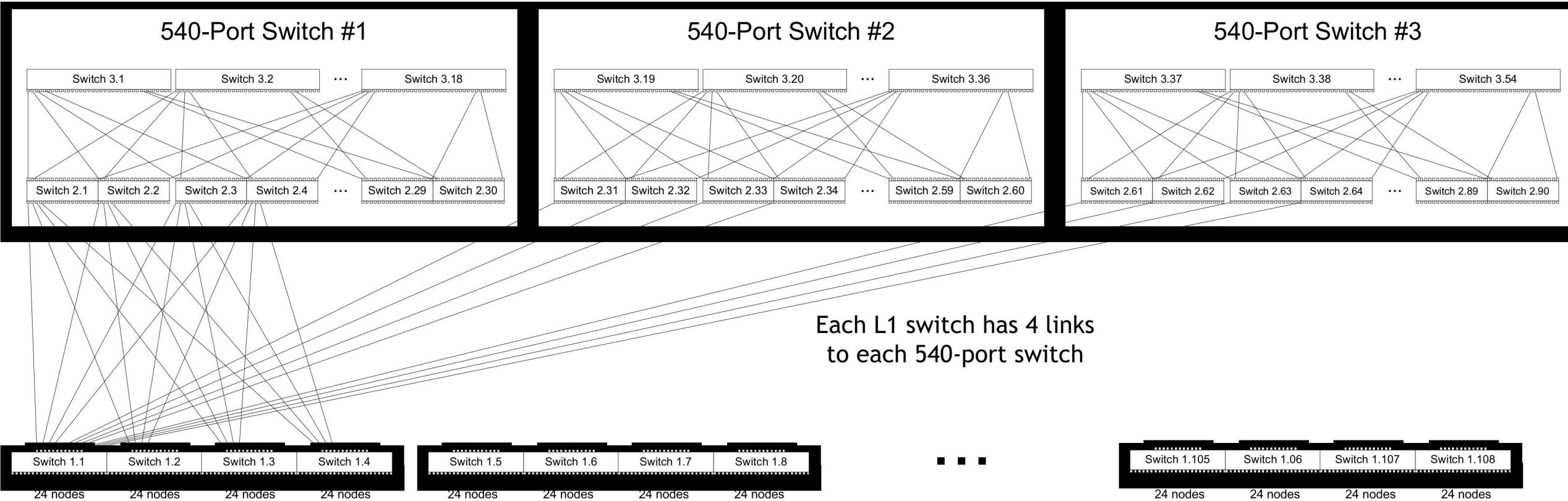


<b>Login &amp; Service Nodes</b>	4 login/compilation nodes 3 Lustre routers to connect to external Sandia filesystem(s) 2 general service nodes
<b>Interconnect</b>	EDR InfiniBand in fat tree topology 2:1 oversubscribed for compute nodes 1:1 full bandwidth for in-platform Lustre storage
<b>System Management</b>	Dual HA management nodes running HPE Performance Software - Cluster Manager (HPCM) Ethernet management network, connects to all nodes One boot server per scalable unit (288 nodes)
<b>In-platform Storage</b>	All-flash Lustre storage system 403 TB usable capacity 244 GB/s throughput

# Network Topology



Mellanox Switch-IB2 EDR, Radix 36 switches, 3 level fat tree, 2:1 taper at L1

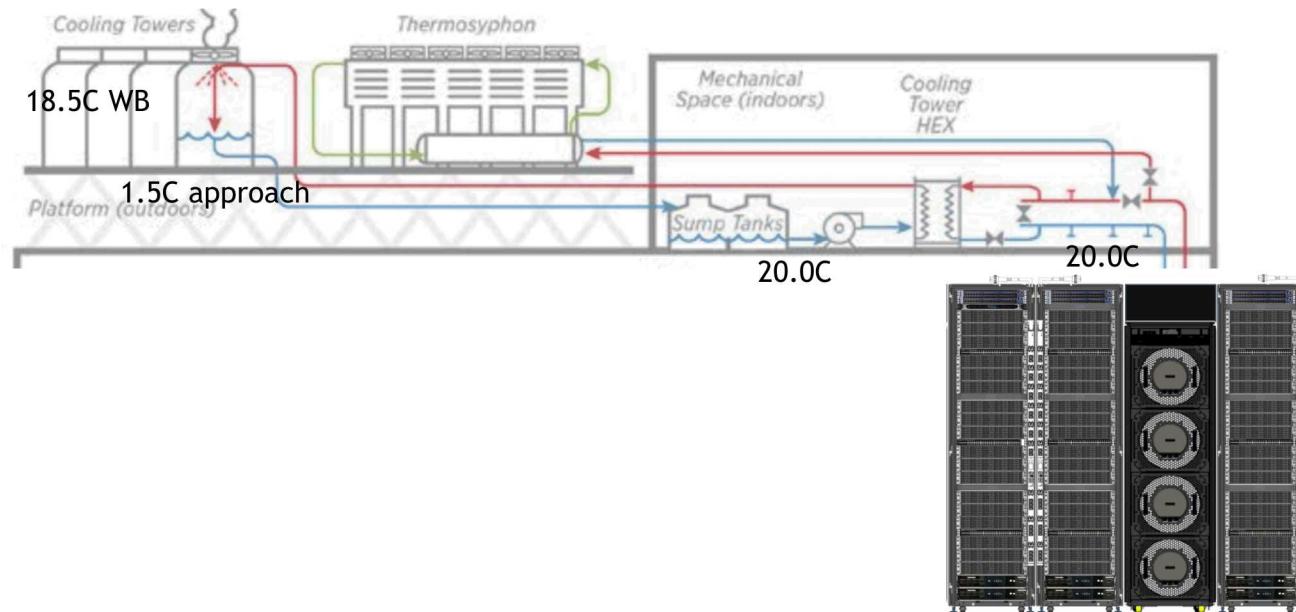


$$108 \text{ L1 switches} * 24 \text{ nodes/switch} = 2592 \text{ compute nodes}$$

# Vanguard-Astra Advanced Power & Cooling

## Extreme Efficiency:

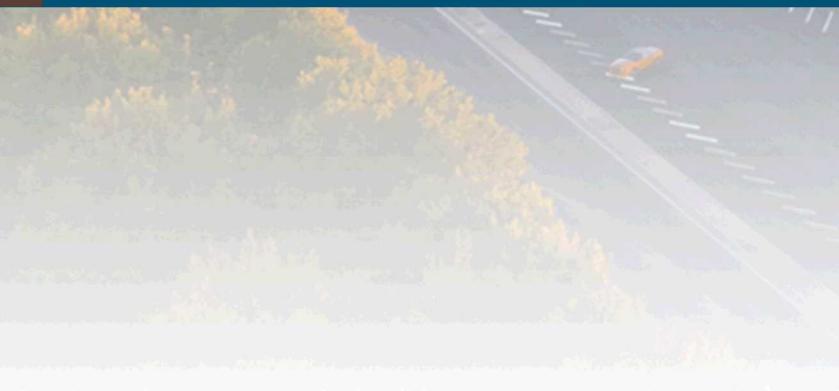
- Total 1.2 MW in the 36 compute racks are cooled by only 12 fan coils
- These coils are cooled without compressors year round. No evaporative water at all almost 6000 hours a year
- 99% of the compute racks heat never leaves the cabinet, yet the system doesn't require the internal plumbing of liquid disconnects and cold plates running across all CPUs and DIMMs
- Builds on work by NREL and Sandia:  
<https://www.nrel.gov/esif/partnerships-jc.html>



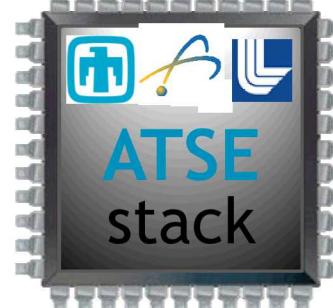
Projected power of the system by component					
per constituent rack type (W)				total (kW)	
	wall	peak	nominal (linpack)	idle	racks
Node racks	39888	35993	33805	6761	36
MCS300	10500	7400	7400	170	12
Network	12624	10023	9021	9021	3
Storage	11520	10000	10000	1000	2
utility	8640	5625	4500	450	1
					1631.5
					1440.3
					1357.3
					274.9



# ATSE – Advanced Tri-lab Software Environment



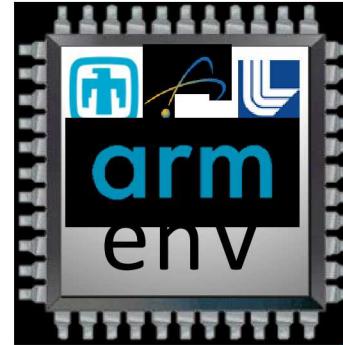
# Advanced Tri-lab Software Environment Goals



- Build an open, modular, extensible, community-inspired, and vendor-adaptable ecosystem
- Prototype new technologies that may improve the DOE ASC computing environment (e.g., ML frameworks, containers, VMs, etc)
- Leverage existing efforts
  - Tri-lab OS (TOSS)
  - OpenHPC & other programming environments
  - Exascale Computing Project (ECP) software technologies



# Tri-Lab Software Effort for ARM



- Accelerate ARM ecosystem for ASC computing
  - Prove viability for ASC integrated codes running at scale
  - Harden compilers, math libraries, tools, communication libraries
    - Heavily templated C++, Fortran 2003/2008, Gigabyte+ binaries, long compiles
  - Optimize performance, verify expected results
- Build integrated software stack
  - Programming environment (compilers, math libs, tools, MPI, OMP, SHMEM, I/O, ...)
  - Low-level OS (optimized Linux, network, filesystems, containers/VMs, ...)
  - Job scheduling and management (WLM, app launcher, user tools, ...)
  - System management (boot, system monitoring, image management, ...)

Improve 0 to 60 time... ARM system arrival to useful work done

# ARM Tri-lab Software Environment (ATSE)

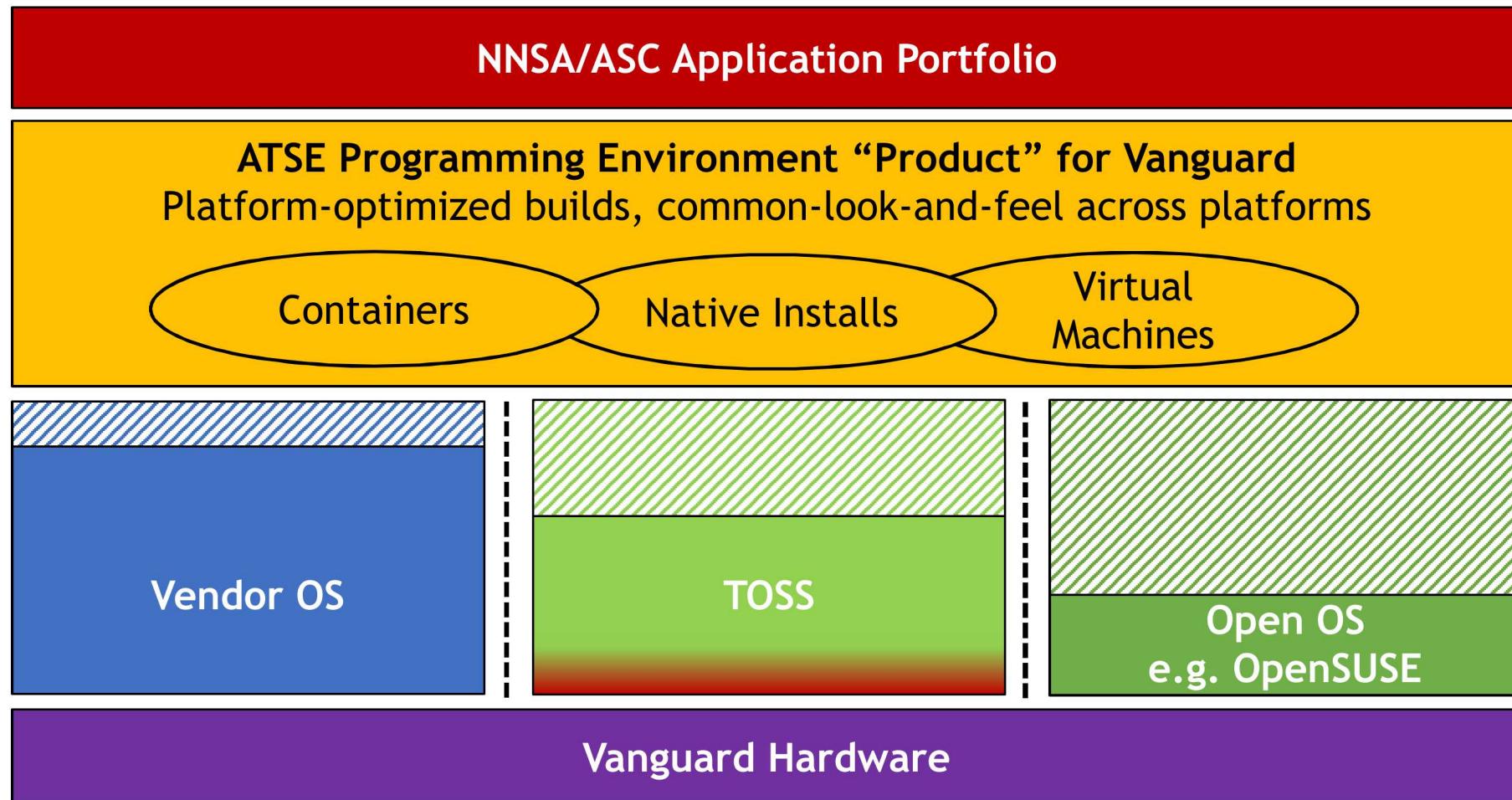


User-facing  
Programming Env

ATSE Packaging

Cluster Middleware  
e.g. Lustre, SLURM

Base OS  
Layer



Open Source

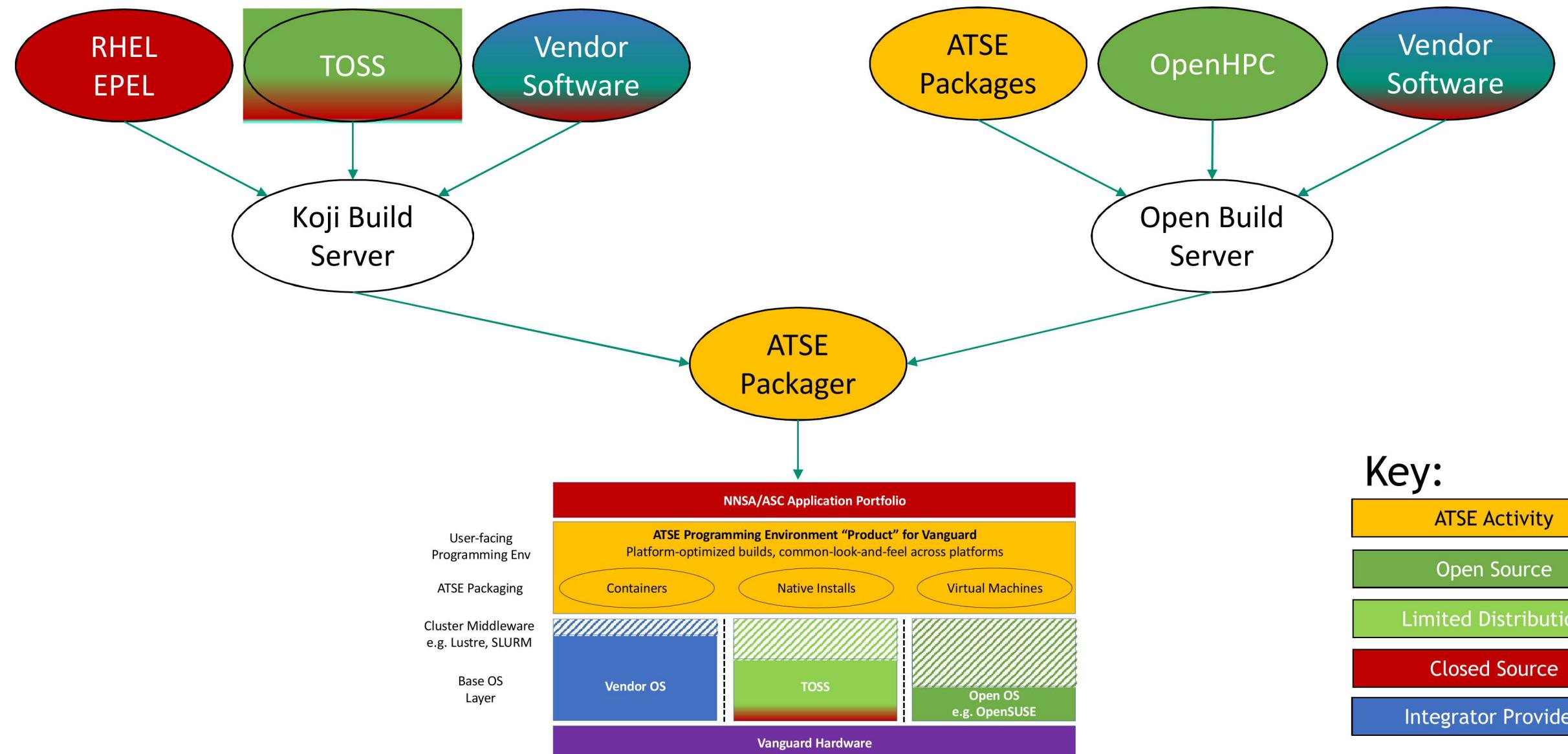
Limited Distribution

Closed Source

Integrator Provided

ATSE Activity

# Integrate Components from Many Sources



# Draft ATSE Timeline for 2018

## ✓ March

- ✓ Continue software stack explorations and gap analysis on testbeds
- ✓ Setup OpenBuild server and replicate OHPC package builds for aarch64

## ✓ April – May

- ✓ Develop ATSE Packager framework, ability to pull packages from TOSS, RHEL, OpenHPC OBS, vendor, and other sources
- ✓ Identify initial component list

## ✓ July

- ✓ Initial ATSE release 2018.0 on Mayer
  - ✓ Lab-distribution version: TOSS BaseOS + (ATSE-GCC | ATSE-ARM | ATSE-\*)
  - Open-distribution version: SUSE and/or CentOS BaseOS + ATSE-GCC

## ▪ Q3 2018

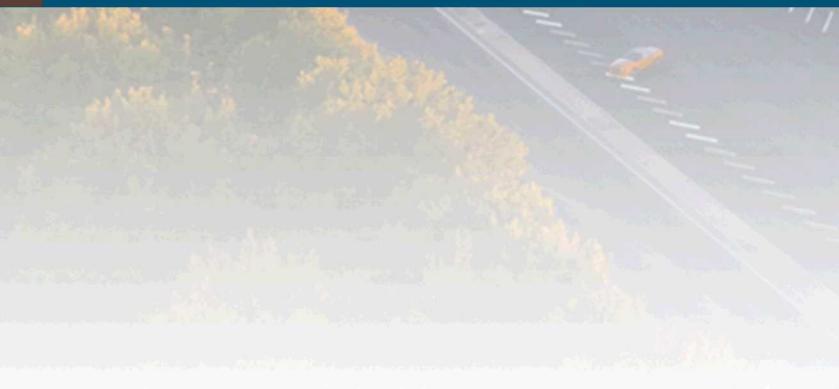
- Linux kernel optimization and HPC patches
- Basic VM & container support

## ▪ Q4 2018

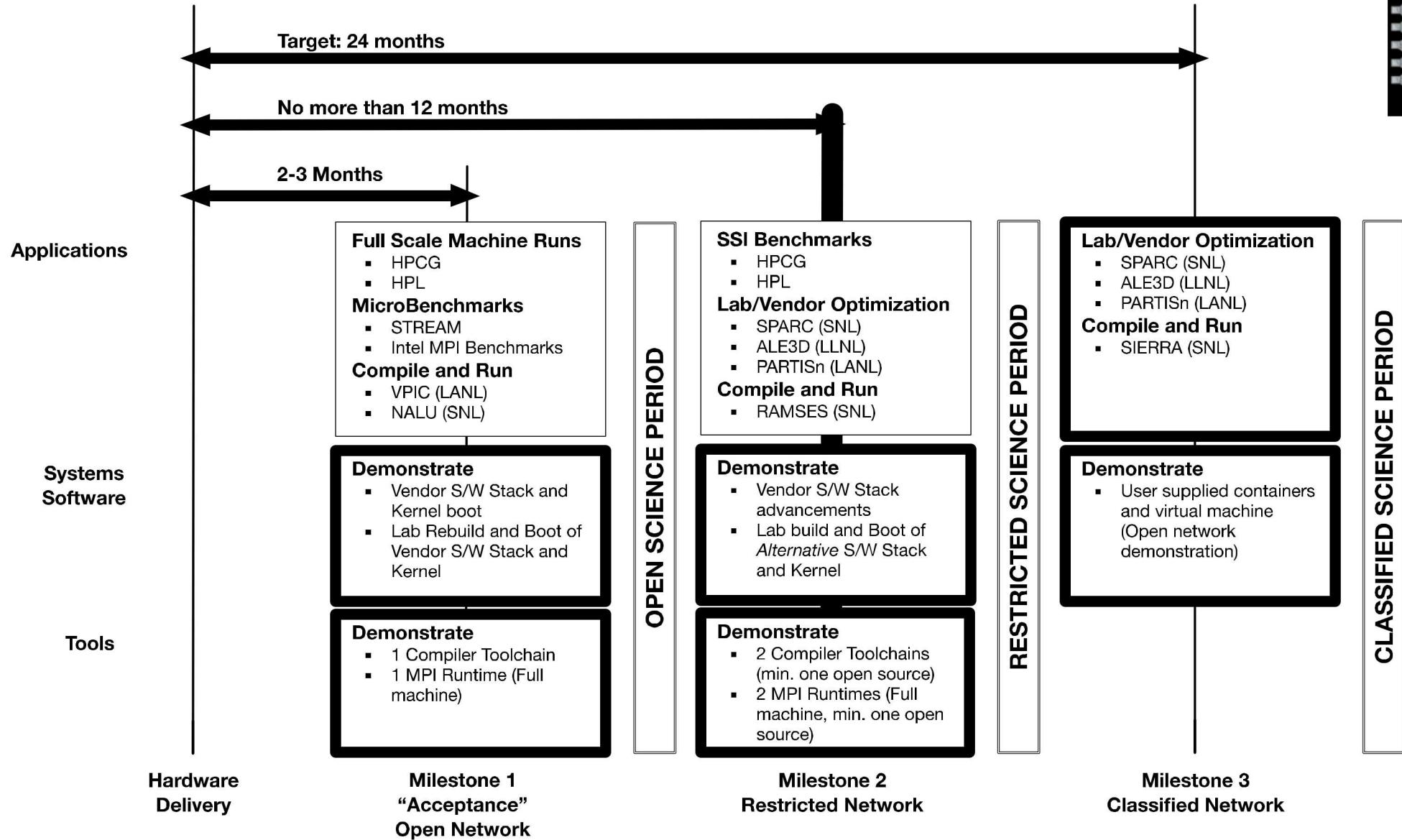
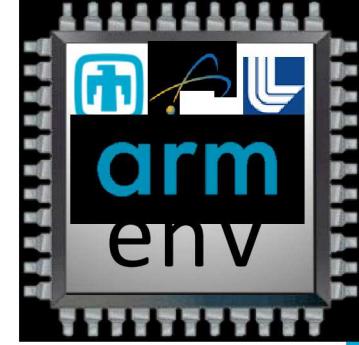
- ATSE 2018.1 release
- Initial upstream to OpenHPC push



## Astra Status and Research

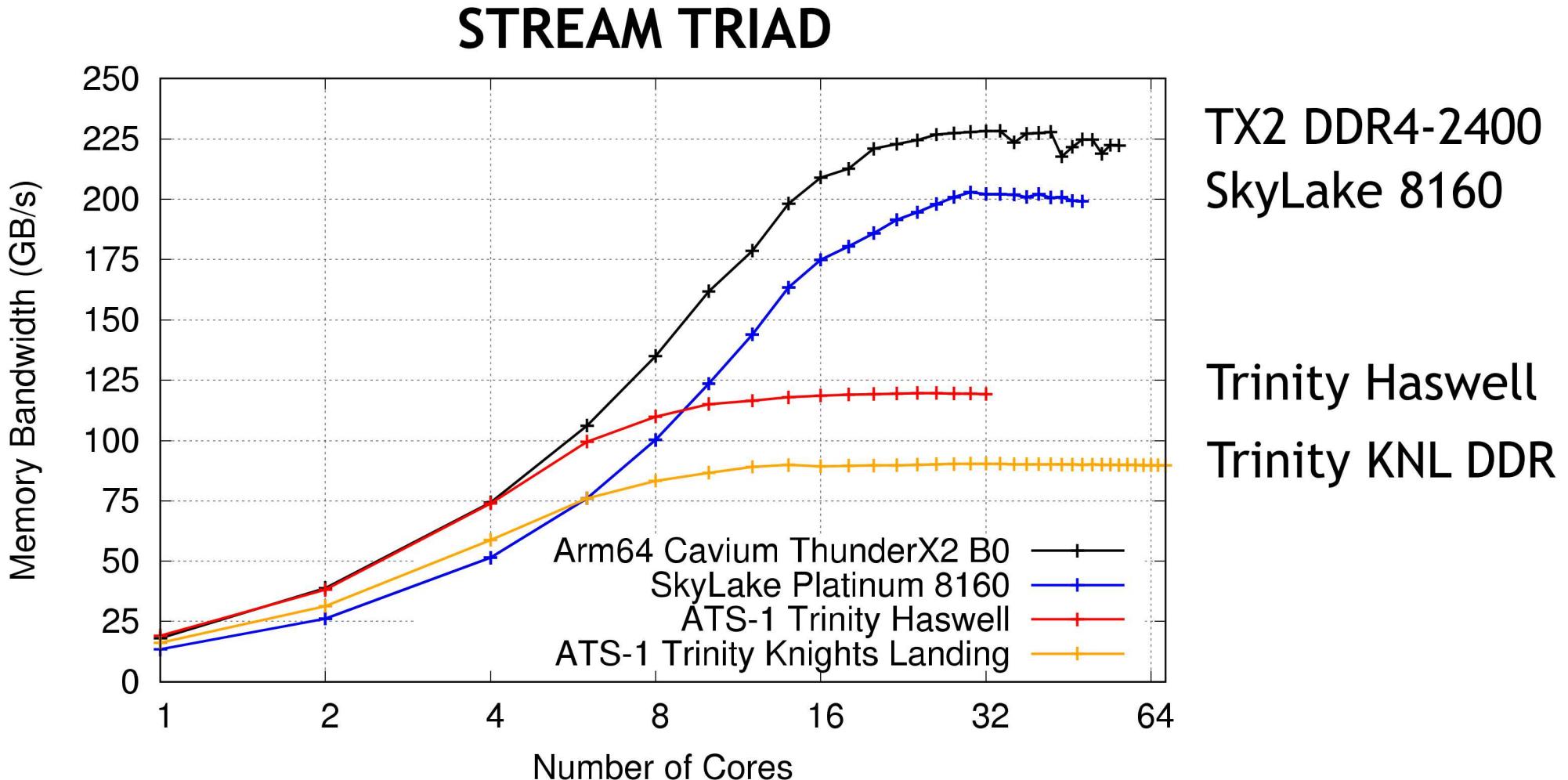


# Acceptance Plan – Maturing the Stack



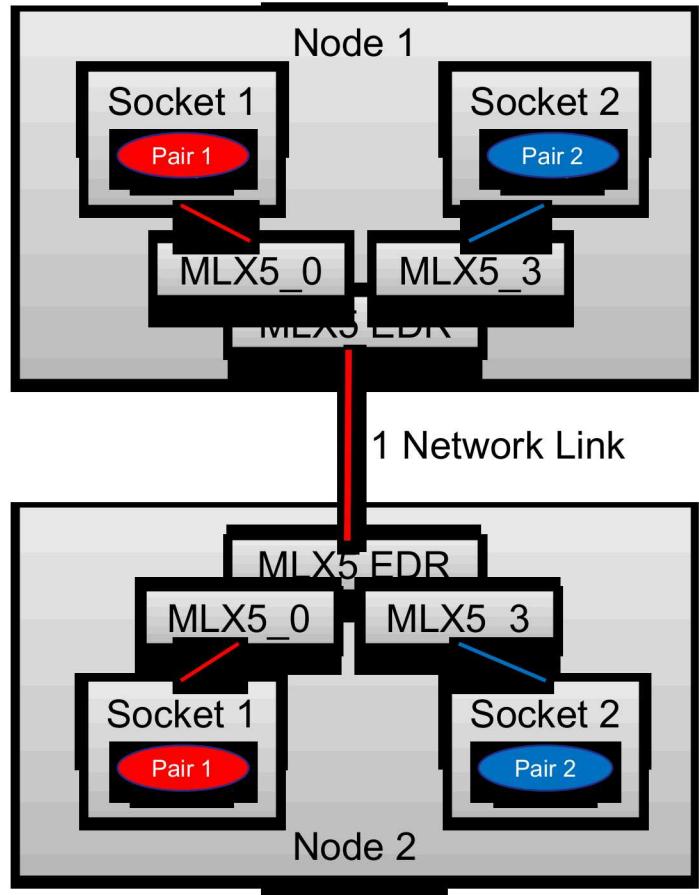
# Cavium Arm64 Providing Best-of-Class Memory Bandwidth

23

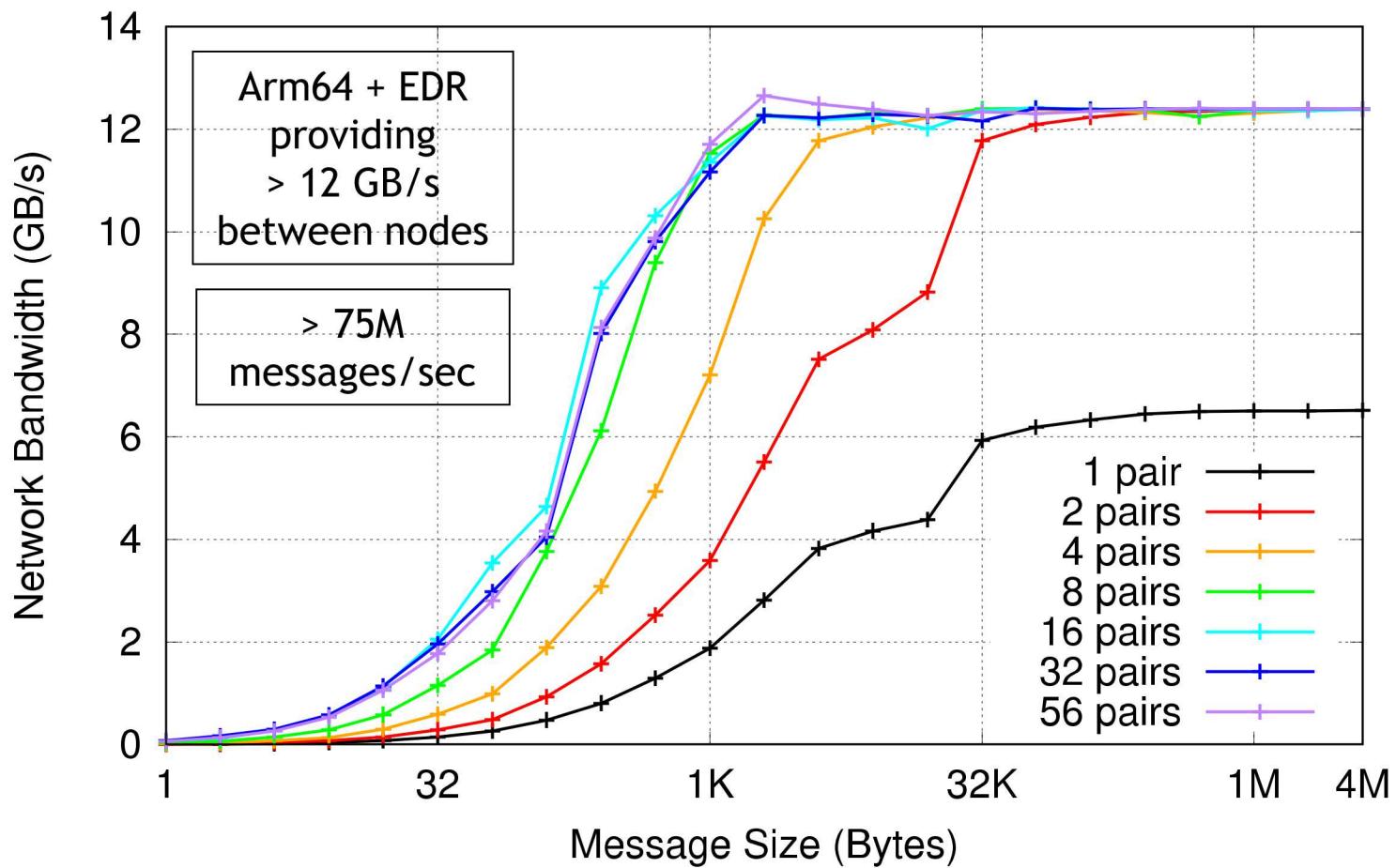


# Network Bandwidth on ThunderX2 + Mellanox MLX5 EDR with Socket Direct

Socket Direct - Each socket has dedicated path to the NIC

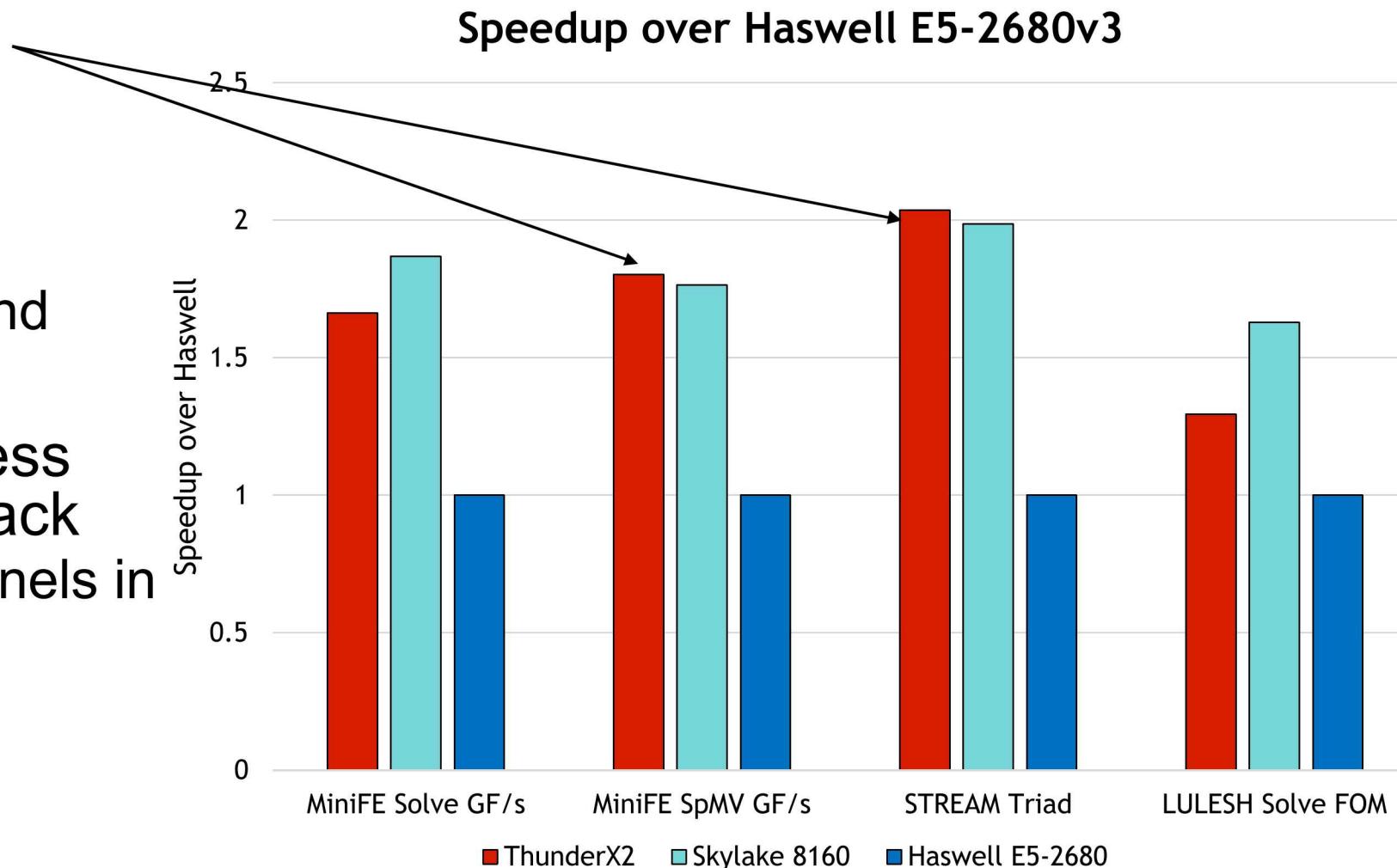


OSU MPI Multi-Network Bandwidth



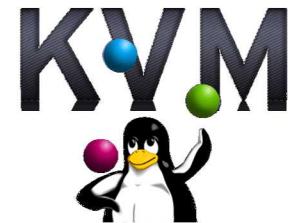
# Mini-App Performance on Cavium ThunderX2

- ThunderX2 providing high memory bandwidth
  - 6 channels (Skylake) vs. 8 in ThunderX2
  - See this in MiniFE SpMV and STREAM Triad
- Slower compute reflects less optimization in software stack
  - Examples – Non-SpMV kernels in MiniFE and LULESH
  - GCC and ARM versus Intel compiler



# R&D Areas

- Leverage containers and virtual machines
  - Support for machine learning frameworks
  - ARMv8.1 includes new virtualization extensions, SR-IOV
  - Working with Sylabs on full container solution
- Evaluating parallel filesystems + I/O systems @ scale
  - GlusterFS, Ceph, BeeGFS, Sandia Data Warehouse, ...
- Resilience studies over Astra lifetime
- Improved MPI thread support, matching acceleration
- OS optimizations for HPC @ scale
  - Exploring HPC-tuned Linux kernels to non-Linux lightweight kernels and multi-kernels
  - Arm-specific optimizations



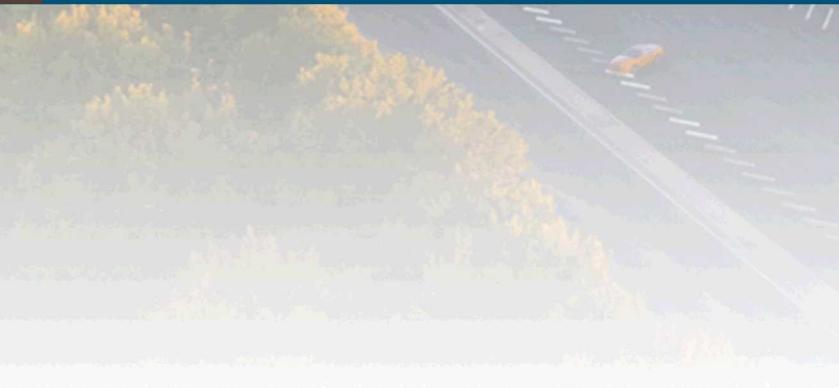
# Conclusion

- Vanguard allows the DOE to take necessary risks to ensure a healthy HPC ecosystem for future production mission platforms
  - Increase technology choices
  - Prove ability to run multi-physics production applications at scale
- Tri-lab software stack effort to mature ARM for ASC computing
  - Harden compilers, math libs, and tools
  - Optimize performance, verify expected results
  - Increase modularity and openness of software stack
  - Support traditional HPC and emerging AI + ML workloads
- Sandia now a member of Linaro HPC SIG!



Questions?

[ajyoung@sandia.gov](mailto:ajyoung@sandia.gov)



**VANGUARD**



- What opportunities and challenges do we face when moving from an x86 world to an ARM world?
  - Virtual Machines
    - Near-native HPC performance with VMs possible in x86
      - Type1 & Type2 hypervisors
      - Hobbes / Palacios VM
    - Avoid legacy issues with x86?
    - Anything new we can do with ARM?
  - Containers
    - How do I build containers on my x86 laptop that run on Astra?
    - Focus on ABI compatibility
  - Leverage industry/enterprise without losing HPC focus