This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

SAND2019-11875J

Multidimensional Thermal Analysis of an Ultrawide Bandgap AlGaN Channel High Electron Mobility Transistor

James Spencer Lundh[1], Bikramjit Chatterjee[1], Yiwen Song[1], Albert G. Baca[2], Robert J. Kaplar[2], Thomas E. Beechem[2], Andrew A. Allerman[2], Andrew M. Armstrong[2], Brianna A. Klein[2], Anushka Bansal[3], Disha Talreja[3], Alexej Pogrebnyakov[3], Eric Heller[4], Venkatraman Gopalan[3], Joan M. Redwing[3], Brian M. Foley[1], and Sukwon Choi[1,a)]

[1]Department of Mechanical Engineering, The Pennsylvania State University, University Park, Pennsylvania, 16802, USA
[2]Sandia National Laboratories, Albuquerque, New Mexico, 87185, USA
[3]Department of Materials Science and Engineering, The Pennsylvania State University, University Park, Pennsylvania 16802, USA
[4]Materials and Manufacturing Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, Ohio, 45433, USA

Abstract

Improvements in radio frequency (RF) and power electronics can potentially be realized through the incorporation of ultrawide bandgap (UWBG) materials such as aluminum gallium nitride ($Al_xGa_{1-x}N$). Multidimensional thermal characterization of an $Al_{0.30}Ga_{0.70}N$ channel high electron mobility transistor (HEMT) was done using Raman spectroscopy and thermoreflectance thermal imaging to experimentally determine the lateral and vertical steady-state operating temperature profiles under DC bias conditions. An electrothermal model of the $Al_{0.30}Ga_{0.70}N$ channel HEMT was developed to validate the experimental results and provide detailed spatial temperature profiles. The model was applied to investigate potential device-level thermal management solutions for $Al_xGa_{1-x}N$ channel HEMTs. While the low thermal conductivity of this III-N ternary alloy system results in more device self-heating at room temperature, the temperature insensitive thermal and electrical output characteristics of $Al_xGa_{1-x}N$ may open the door for extreme temperature applications.

Keywords: aluminum gallium nitride (AlGaN), electrothermal co-design, extreme environment electronics, high electron mobility transistor, Raman spectroscopy, thermal management, thermoreflectance thermal imaging, ultra-wide bandgap semiconductors.

[a)] Author to whom correspondence should be addressed: sukwon.choi@psu.edu

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Wide bandgap (WBG) gallium nitride (GaN) channel high electron mobility transistors (HEMTs) have matured significantly over decades of research and development, and commercial devices are available from multiple vendors. As such, researchers are investigating pathways for next generation devices through the adoption of ultrawide bandgap (UWBG) materials with bandgaps larger than that of GaN (~3.4 eV). $Al_xGa_{1-x}N$, whose bandgap energy increases with Al-composition ($0<x<1$), emerges as a natural choice due to the ability to pursue research and development based on the established GaN HEMT technology. Favorable characteristics of $Al_xGa_{1-x}N$ such as high breakdown field, high saturation velocity, and high temperature operation demonstrate the superior potential of $Al_xGa_{1-x}N$ channel HEMTs for high power switching and RF applications[1–3].

For high power switching applications, high breakdown voltages (V_B) and low specific on-resistances ($R_{on,sp}$) are required[4]. A lateral figure of merit (LFOM) has been formulated to compare the potential of material systems for power-switching[3]:

$$LFOM = \frac{V_B^2}{R_{on,sp}} = q\mu_{ch}n_sE_c^2$$

where q is the electronic charge constant, μ_{ch} is the channel mobility, n_s is the sheet carrier density, and E_c is the critical electric field. Since critical electric field scales with bandgap energy ($E_c \sim E_g^n$, $2<n<2.5$)[5], $Al_xGa_{1-x}N$ offers substantial LFOM improvements over GaN at high temperatures[3]. The channel mobility of $Al_xGa_{1-x}N$ devices is relatively low due to disordered alloy scattering[6], but research to improve μ_{ch} of the $Al_xGa_{1-x}N$ active layer is ongoing[7]. High specific on-resistance is another limiting factor, but recent studies show promise for improved ohmic contact technologies[8–10], especially at high temperatures[8].

For high power radio frequency (RF) applications, high breakdown voltages and high cutoff frequencies (f_T) are required[11]. The Johnson figure of merit (JFOM) is employed to assess material systems for high frequency operation[3]:

$$JFOM = V_Bf_T = \frac{E_cv_{sat}}{2\pi}$$

where v_{sat} is the electron saturation velocity. While theoretical studies show slight reductions in v_{sat} for $Al_xGa_{1-x}N$ with low/intermediate Al-compositions, the increased critical electric field at higher Al-compositions (allowing shorter channel devices) dominates and improves the JFOM over GaN[3].

$Al_xGa_{1-x}N$ channel HEMT technology has been advancing over the past few years through continued efforts to improve electrical performance such as lowering contact resistance[8–10]. However, excluding "high temperature testing" involving electrical characterization at elevated base temperatures[2,12], device-level thermal characterization has been absent. Because $Al_xGa_{1-x}N$ is promising for next generation power and RF electronics, the thermal characteristics and limits of this device technology need exploration.

Similar to GaN HEMTs, device self-heating is expected. Device self-heating was studied extensively in GaN HEMTs[13–16] and much research was focused on thermal management of these devices[16–21]. Likewise, experimental characterization of device self-heating in the $Al_xGa_{1-x}N$ technology is necessary to lay the groundwork for electrothermal co-design. Unfortunately, the self-heating behavior of $Al_xGa_{1-x}N$ HEMTs has been unexplored due to challenging experimental limitations. An electrothermal model which reproduces both electrical and thermal characteristics of a device can be used to design thermal management solutions and test the applicability of the new device technology for extreme environment applications. As such, thermal characterization and electrothermal simulation were performed on both $Al_{0.30}Ga_{0.70}N$ and GaN channel HEMTs for

comparison, and the thermal management of $Al_xGa_{1-x}N$ channel HEMTs for high temperature applications is briefly discussed.

The $Al_{0.30}Ga_{0.70}N$ channel HEMTs[12] (Fig. 1) were grown on 1.3 mm thick sapphire substrates using metal organic chemical vapor deposition (MOCVD). First, a 1.6 µm AlN transition layer was grown followed by a 3.9 µm and 0.25 µm $Al_{0.30}Ga_{0.70}N$ buffer and channel layer, respectively. The structure was capped with a 50 nm $Al_{0.45}Ga_{0.55}N$ barrier and SiN passivation. The ohmic contacts were formed using a Ti/Al/Ni/Au (25/100/15/50 nm) metal stack. The gate contact was formed using a Ni/Au Schottky metal stack with 1 µm field plate extensions over the SiN dielectric on the drain and source sides. For some test structures, the field plate was slightly misaligned to provide more direct access to the drain side edge of the gate contact for temperature measurement. This was done because this is the location of peak heat generation due to localized electric field concentration[22,23]. The HEMTs have a circular device structure with a gate length of 2 µm, gate-drain and gate-source spacings of 4 µm, and gate circumference of 330 µm. GaN HEMTs with similar circular device geometries were studied for comparison with the $Al_{0.30}Ga_{0.70}N$ channel HEMTs. The GaN HEMTs were grown on a 650 µm thick semi-insulating 6H-SiC substrate with a thin (~50 nm) AlN transition layer and a 4 µm thick GaN buffer. The GaN HEMTs have a gate length of 2 µm, gate-drain spacing of 6 µm, gate-source spacing of 2 µm, and gate circumference of 310 µm.

An electrothermal model[24] was developed that couples an electrical model (Synopsys Sentaurus) with a finite element thermal model (COMSOL Multiphysics). Material properties such as bandgap energy, electron mobility, and dielectric constant were adopted from the literature[1,3]. The contact and sheet resistances of both the $Al_{0.30}Ga_{0.70}N$ and GaN channel HEMTs were extracted using transmission line model (TLM) measurements and corrections were applied to account for the circular device geometries[25]. Four-point probing was used to reduce parasitic resistances from electrical connections. The temperature dependent thermal conductivity of the $Al_{0.30}Ga_{0.70}N$ channel/buffer layer was measured using frequency domain thermoreflectance (FDTR)[26], a laser-based optical pump-probe method. In this work, the pump laser (405 nm Coherent Obis) is directly modulated by the lock-in amplifier (Zurich Instruments HF2LI) to produce a square waveform, while the frequency-matched probe laser (532 nm Coherent Obis) is coaxially aligned with the pump to detect the magnitude and phase of the surface temperature relative to the pump laser heating event. By sweeping across a range of heating frequencies and measuring the frequency dependent phase difference between the heat flux and the surface temperature, the thermal properties of the $Al_{0.30}Ga_{0.70}N$ can be determined by fitting the data to a multilayer model and extracting unknown parameters of interest. Expected uncertainties in measured values are typically ≤10%, largely driven by uncertainties in model input parameters such as heat capacity and layer thickness, as well as error associated with scan-to-scan repeatability (laser spot focus, pump/probe beam overlap). The thermal conductivity of the $Al_{0.30}Ga_{0.70}N$ channel/buffer layer was measured to be 8.5 ± 0.85 W/(m*K) at room temperature and with a negligible temperature dependence up to 450 K. To account for potential spatial variations, five measurements were made at various locations on the sample for all temperatures tested.

Multidimensional thermal characterization was performed using both Raman thermometry and thermoreflectance thermal imaging. As demonstrated previously[27], thermoreflectance thermal imaging can be applied to acquire 2D thermal maps of device surfaces; the method is particularly effective for the measurement of highly reflective features such as metallization structures and was therefore used to determine the temperatures of the HEMT source, drain, and gate electrodes. Thermoreflectance thermal imaging was performed using a Microsanj NT-210A system equipped

with a 3-axis piezo-controlled stage and a 1626 x 1236 pixel charge coupled device (CCD) camera. A long working distance 50X objective (NA=0.45) was used, providing a spatial resolution of ~0.6 μm with 530 nm LED illumination. Using standard calibration procedures[28], point-by-point thermoreflectance coefficient maps of the $Al_{0.30}Ga_{0.70}N$ HEMT electrodes were obtained.

To probe the channel surface temperatures of the HEMTs, nanoparticle-assisted Raman thermometry[29] was used. In this technique, the temperature dependence of the Raman peak position of a particular phonon mode of the deposited nanoparticle is used to determine the device surface temperature since the nanoparticle is assumed to be in thermal equilibrium with the device surface. Since the nanoparticle can thermally expand freely, stress affecting the Raman peak position is assumed to be negligible. From a previous study the authors conducted[29], titanium dioxide (TiO_2) nanoparticles with 99.98% purity were selected due to excellent temperature sensitivity of the E_g phonon mode peak position and low measurement uncertainty. Nanoparticle-assisted Raman thermometry was performed using a Horiba LabRAM HR Evolution spectrometer with 532 nm excitation. Measurements were performed in a 180° backscattering configuration with a long working distance 50X objective (NA=0.45) where the spatial resolution is determined by the size of the sub-micrometer nanoparticles. To reduce systematic error in peak position shifts resulting from sources such as room temperature fluctuations, a reference mercury emission line at ~546 nm in the Raman spectra was used. The dependence of the TiO_2 E_g Raman peak position on incident laser power was investigated to determine the threshold for laser-induced heating of the nanoparticles in order to select a suitable laser power (~1 mW).

To investigate the vertical temperature distribution in these devices, confocal Raman thermometry was used. Using the experimental setup described above, these measurements offered a spatial resolution of ~1 μm and a depth of field of ~10 μm[30]. For the GaN HEMTs, it was possible to probe the average temperatures of the GaN channel/buffer layers and the top ~6 μm of the SiC substrate. The temperature of the AlN transition layer could not be probed due to low intensity and signal-to-noise ratio resulting from the small layer thickness. For the AlGaN HEMTs, it was possible to probe the average temperatures of the $Al_{0.30}Ga_{0.70}N$ channel/buffer layers, AlN transition layer, and the top ~5 μm of the sapphire substrate. To determine the temperature of the GaN layer, a multi-spectral analysis method[31] was used. For the remaining layers, Raman temperature calibrations were performed to determine the temperature dependence of the peak positions and linewidths of several phonon modes; the temperature calibrations consisted of measuring the peak position and linewidth at zero power dissipation through the stage temperature range of 25°C and 175°C in 10°C intervals. Based on the sensitivity and linearity of the temperature dependence, the following Raman phonon modes and their respective spectral features were monitored: $Al_{0.30}Ga_{0.70}N$ A_1 (LO) peak position[32], AlN A_1 (LO) peak position[32], sapphire A_{1g} peak position, and SiC E_2 (TO) peak position. To minimize stress effects on the peak position shift[33] for $Al_{0.30}Ga_{0.70}N$ and AlN, the A_1 (LO) peak position was monitored because it has been shown to be less sensitive to thermoelastic stress effects as compared to the E_2 (high) peak position[32,34]. Due to larger probing volumes and smaller temperature gradients in the sapphire and SiC substrates, stress effects were assumed not to significantly impact the measured temperature results.

The dependence of bias conditions (for fixed power dissipation) on the heat generation profile and the resulting channel temperature distribution was also investigated since the channel peak temperature rise was shown to directly impact the device lifetime[23]. The gate bias conditions were determined from the transfer characteristics of the $Al_{0.30}Ga_{0.70}N$ HEMT (Fig. 2(a)). The pinched-off channel condition was defined as the gate voltage which resulted in ~15% of the saturation

drain current (V_{GS}=1V); the open channel condition was defined as the gate voltage which resulted in ~90% of the saturation drain current (V_{GS}=4V). For the GaN HEMTs, the open channel condition utilized the same requirement which resulted in V_{GS}=2V. The measured output characteristics of the $Al_{0.30}Ga_{0.70}N$ channel HEMT show good agreement with simulation results, establishing confidence in the model (Fig. 2(b)).

Comparison of the vertical temperature distributions of the $Al_{0.30}Ga_{0.70}N$ and GaN channel HEMTs shown in Fig. 3 highlights the magnification of self-heating in the $Al_{0.30}Ga_{0.70}N$ channel HEMT due to the increased thermal resistance resulting from the lower thermal conductivity of the $Al_{0.30}Ga_{0.70}N$ system. Under open channel conditions, the $Al_{0.30}Ga_{0.70}N$ HEMT (V_{DS}=9V, $P_{density}$=0.76 W/mm) has a peak temperature approximately three times greater than for the GaN HEMT (V_{DS}=20V, $P_{density}$=1.61 W/mm) while operating at less than half the power density. However, this is expected due to the high thermal resistance of the $Al_xGa_{1-x}N$-on-sapphire system ($k_{Al0.3Ga0.7N}$~8.5 W/(m*K))[35] as compared to GaN-on-SiC (k_{GaN}~130 W/(m*K))[36,37]. Additionally, the magnitude of the temperature gradient in the $Al_{0.30}Ga_{0.70}N$ channel/buffer is greater than that in the GaN channel/buffer suggesting greater resultant thermal stress gradients in the former.

Under pinched-off conditions (V_{DS}=31V, $P_{density}$=0.76 W/mm), the heat generation in the $Al_{0.30}Ga_{0.70}N$ HEMT becomes more localized under the drain-side corner of the gate whereas for open channel conditions the heat generation is more evenly distributed across the channel length[23,38] (Fig. 4(a)). The peak heat generation of the $Al_{0.30}Ga_{0.70}N$ HEMT under open channel conditions only reaches ~60% of that under pinched-off conditions for an identical power dissipation level. Extending the dimensionality of the thermal analysis to probe both the lateral and vertical temperature distributions, the normalized magnitude and distribution of the heat generation profile of the $Al_{0.30}Ga_{0.70}N$ HEMT under these two different bias conditions is reflected in the resulting measured and simulated temperature profiles (Fig. 4(b) and 4(c)). The magnitude of the vertical temperature gradient in the $Al_{0.30}Ga_{0.70}N$ at the drain-side edge of the gate increases substantially as the device channel becomes more pinched-off (Fig. 4(c)). This can be understood as a marked increase in the local heat flux in the active region of the device because the heat generation becomes more localized in accordance with the electric field concentration at the drain-side edge of the gate.

The electrothermal model was applied to evaluate the effectiveness of thermal management solutions developed for III-V device technologies, including both bottom-side (high thermal conductivity substrate integration[39,40]) and top-side (flip-chip integration[41]) approaches. As shown in Fig. 5(a), bottom-side approaches (Case 2) such as selecting a high thermal conductivity substrate like diamond[39,40] and thinning the buffer layer reduce the device thermal resistance by 67%. Top-side thermal management realized through flip-chip integration to a carrier substrate[41] using gold bumps (Cases 3 and 4) showed more promising results as reductions in thermal resistance up to 78% were achieved. This is because flip-chip integration enables heat sinking within closer proximity to the heat generation in the device. While thermal management of the $Al_{0.30}Ga_{0.70}N$ channel HEMT was very effective at reducing thermal resistance, the thermal performance was not comparable to the reference GaN HEMT (Case 5) at room temperature base conditions. However, the model may not be optimized for the final packaging or application. For example, the model imposes an isothermal bottom-side boundary condition of 25°C which can be unrealistic. Because the AlGaN thermal conductivity is a much weaker function of temperature than for GaN, the choice of 25°C was very conservative in that the thermal benefits of GaN over AlGaN observed here will diminish at higher temperature boundary conditions more relevant to many applications especially high temperature and extreme environment electronics[42].

Accordingly, the effect of base temperature on thermal resistance in the $Al_{0.30}Ga_{0.70}N$ and GaN channel HEMTs were investigated and compared (Fig. 5(b)). For all thermal management schemes, the $Al_{0.30}Ga_{0.70}N$ HEMT showed potential for better thermal performance than the GaN HEMT at high temperatures due to significant increases in the thermal resistance of the GaN system with temperature[37]. For example, for the $Al_{0.30}Ga_{0.70}N$ HEMT on a sapphire substrate flip chip integrated to a diamond carrier (Case 4), the thermal resistance becomes less than that for the reference GaN HEMT (Case 5) for base temperatures beyond 250°C. In contrast to GaN, the combination of the ultrawide bandgap, thermal conductivity with negligible temperature dependence[43], and relatively temperature insensitive electrical output characteristics[2,8,44] make AlGaN suitable for high temperature electronics that require stable operation[45]. These results highlight the significant advantages that thermally-optimized $Al_xGa_{1-x}N$ devices can have over GaN in extreme temperature environments[46,47].

However, thermal management solutions can negatively affect electrical performance and electrothermal co-design is required. While diamond is the most effective substrate/carrier for thermal management (Fig. 5(a)) due to its high thermal conductivity, AlN could be more promising from economical and electrical standpoints due to lower cost and increased mobility resulting from reduced threading dislocation densities and higher crystalline quality of the $Al_xGa_{1-x}N$ buffer layer[7]. Top-side thermal management approaches such as flip chip integration inherently increase parasitic capacitances in the devices[48], lowering the cutoff and maximum operational frequencies for RF applications[49]. Efforts to minimize these parasitic capacitances by increasing the stand-off distance between the RF chip and sub-mount through the use of thicker bonding pads would increase the thermal resistance between the transistor channel and thermal ground, negating the benefits of flip-chip integration. This example highlights the interdependent nature of the problem and the need to consider the electrical and thermal performance simultaneously. Additionally, more realistic device designs such as multi-finger devices need to be considered as the benefits of the flip-chip integration used here diminishes for these devices since the contact pads are much farther from the active area of the device. However, previous studies[50,51] have demonstrated successful electrothermal co-design of power devices which enabled multi-finger AlGaN/GaN HFETs with significantly reduced areal footprints while improving both the electrical and thermal device performance.

In conclusion, thermal analysis of an $Al_{0.30}Ga_{0.70}N$ channel HEMT was undertaken through multidimensional thermal characterization and electrothermal simulation. Increased room temperature thermal resistance due to the lower thermal conductivity of the $Al_xGa_{1-x}N$ system results in aggravated device self-heating and large temperature gradients through the thickness of the $Al_{0.30}Ga_{0.70}N$ layer. Applying thermal management solutions established for III-V device technologies, the thermal performance of the $Al_{0.30}Ga_{0.70}N$ channel HEMT can improve significantly. Although relatively inferior at room temperature, the thermal performance of thermally-optimized $Al_{0.30}Ga_{0.70}N$ channel HEMTs can become comparable or superior to standard GaN channel HEMTs at high ambient temperature conditions. Combined with benefits from the ultra-wide bandgap and temperature insensitive electrical output characteristics, the $Al_xGa_{1-x}N$ device technology has potential to enable applications that require extended operation at high temperatures (350°C-1000°C) where active cooling is not feasible, including combustion chambers, exhaust systems of automotive/aviation engines, down-hole environments in deep-well drilling, industrial processing plants, re-entry vehicles, and satellites.

Acknowledgment

Funding for efforts by the Pennsylvania State University was provided by the AFOSR Young Investigator Program (Grant No. FA9550-17-1-0141, Program Officers: Dr. Brett Pokines and Dr. Michael Kendra, also monitored by Dr. Kenneth Goretta). Additional funding (Anushka Bansal and Joan M. Redwing) was provided by NSF (DMR-1808900). Disha Talreja, Alexej Pogrebnyakov, and Venkatraman Gopalan acknowledge support from the Penn State NSF-MRSEC Center for Nanoscale Science Grant number DMR 1420620. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

References

[1] T. Nanjo, A. Imai, Y. Suzuki, Y. Abe, T. Oishi, M. Suita, E. Yagyu, and Y. Tokuda, IEEE Trans. Electron Devices **60**, 1046 (2013).
[2] P.H. Carey IV, F. Ren, A.G. Baca, B.A. Klein, A.A. Allerman, A.M. Armstrong, E.A. Douglas, R.J. Kaplar, P.G. Kotula, and S.J. Pearton, IEEE J. Electron Devices Soc. **7**, 444 (2019).
[3] M.E. Coltrin, A.G. Baca, and R.J. Kaplar, ECS J. Solid State Sci. Technol. **6**, S3114 (2017).
[4] A. Raman, S. Dasgupta, R. Siddharth, J.S. Speck, and M.K. Umesh, Jpn. J. Appl. Phys. **47**, 3359 (2008).
[5] R.J. Kaplar, J.C. Neely, D.L. Huber, and L.J. Rashkin, IEEE Power Electron. Mag. **4**, 36 (2017).
[6] R.J. Kaplar, A.A. Allerman, A.M. Armstrong, M.H. Crawford, J.R. Dickerson, A.J. Fischer, A.G. Baca, and E.A. Douglas, ECS J. Solid State Sci. Technol. **6**, Q3061 (2016).
[7] S. Hashimoto, K. Akita, T. Tanabe, H. Nakahata, K. Takeda, and H. Amano, Phys. Status Solidi Curr. Top. Solid State Phys. **7**, 1938 (2010).
[8] B.A. Klein, A.G. Baca, A.M. Armstrong, A.A. Allerman, C.A. Sanchez, E.A. Douglas, M.H. Crawford, M.A. Miller, P.G. Kotula, T.R. Fortune, and V.M. Abate, ECS J. Solid State Sci. Technol. **6**, S3067 (2017).
[9] S. Bajaj, F. Akyol, S. Krishnamoorthy, Y. Zhang, and S. Rajan, Appl. Phys. Lett. **109**, 133508 (2016).
[10] E.A. Douglas, S. Reza, C. Sanchez, D. Koleske, A. Allerman, B. Klein, A.M. Armstrong, R.J. Kaplar, and A.G. Baca, Phys. Status Solidi Appl. Mater. Sci. **214**, 1600842 (2017).
[11] T. Razzak, H. Xue, Z. Xia, S. Hwang, A. Khan, W. Lu, and S. Rajan, in *2018 IMWS-AMP* (IEEE, 2018).
[12] A.G. Baca, A.M. Armstrong, A.A. Allerman, B.A. Klein, E.A. Douglas, C.A. Sanchez, and T.R. Fortune, ECS J. Solid State Sci. Technol. **6**, S3010 (2017).
[13] X.D. Wang, W. Da Hu, X.S. Chen, and W. Lu, IEEE Trans. Electron Devices **59**, 1393 (2012).
[14] A. Venkatachalam, W.T. James, and S. Graham, Semicond. Sci. Technol. **26**, 085027 (2011).
[15] A. Sarua, H. Ji, M. Kuball, M.J. Uren, T. Martin, K.P. Hilton, and R.S. Balmer, IEEE Trans. Electron Devices **53**, 2438 (2006).
[16] A. Christensen, W.A. Doolittle, and S. Graham, IEEE Trans. Electron Devices **52**, 1683

(2005).
[17] H.C. Nochetto, N.R. Jankowski, and A. Bar-Cohen, in *IMECE2011* (ASME, 2011), pp. 241–249.
[18] G.J. Riedel, J.W. Pomeroy, K.P. Hilton, J.O. Maclean, D.J. Wallis, M.J. Uren, T. Martin, U. Forsberg, A. Lundskog, A. Kakanakova-Georgieva, G. Pozina, E. Janzén, R. Lossy, R. Pazirandeh, F. Brunner, J. Würfl, and M. Kuball, IEEE Electron Device Lett. **30**, 103 (2009).
[19] T.J. Anderson, K.D. Hobart, M.J. Tadjer, A.D. Koehler, E.A. Imhoff, J.K. Hite, T.I. Feygelson, B.B. Pate, C.R. Eddy, and F.J. Kub, ECS J. Solid State Sci. Technol. **6**, Q3036 (2016).
[20] X. Chen, F.N. Donmezer, S. Kumar, and S. Graham, IEEE Trans. Electron Devices **61**, 4056 (2014).
[21] Y. Won, J. Cho, D. Agonafer, M. Asheghi, and K.E. Goodson, IEEE Trans. Components, Packag. Manuf. Technol. **5**, 737 (2015).
[22] S. Karmalkar and U.K. Mishra, IEEE Trans. Electron Devices **48**, 1515 (2001).
[23] S. Choi, E.R. Heller, D. Dorsey, R. Vetury, and S. Graham, IEEE Trans. Electron Devices **60**, 159 (2013).
[24] B. Chatterjee, J.S. Lundh, J. Dallas, H. Kim, and S. Choi, in *2017 ITherm* (IEEE, 2017), pp. 1247–1252.
[25] D.K. Schroder, *Semiconductor Material and Device Characterization* (John Wiley & Sons, 2006).
[26] A.J. Schmidt, R. Cheaito, and M. Chiesa, Rev. Sci. Instrum. **80**, 094901 (2009).
[27] D. Kendig, A. Tay, and A. Shakouri, in *2016 THERMINIC* (IEEE, 2016), pp. 115–120.
[28] A. Shakouri, A. Ziabari, D. Kendig, J.-H. Bahk, Y. Xuan, D.Y. Peide, K. Yazawa, and A. Shakouri, in *2016 SEMI-THERM* (IEEE, 2016), pp. 128–132.
[29] J. Dallas, G. Pavlidis, B. Chatterjee, J.S. Lundh, M. Ji, J. Kim, T. Kao, T. Detchprohm, R.D. Dupuis, S. Shen, S. Graham, and S. Choi, Appl. Phys. Lett. **112**, 073503 (2018).
[30] N.J. Everall, Appl. Spectrosc. **63**, 245A (2009).
[31] S. Choi, E.R. Heller, D. Dorsey, R. Vetury, and S. Graham, IEEE Trans. Electron Devices **60**, 1898 (2013).
[32] M. Kuball, Surf. Interface Anal. **31**, 987 (2001).
[33] T. Beechem, A. Christensen, S. Graham, and D. Green, J. Appl. Phys. **103**, 124501 (2008).
[34] T. Batten, J.W. Pomeroy, M.J. Uren, T. Martin, and M. Kuball, J. Appl. Phys. **106**, 094509 (2009).
[35] B.C. Daly, H.J. Maris, A. V. Nurmikko, M. Kuball, and J. Han, J. Appl. Phys. **92**, 3820 (2002).
[36] T.E. Beechem, A.E. McDonald, E.J. Fuller, A.A. Talin, C.M. Rost, J.-P. Maria, J.T. Gaskins, P.E. Hopkins, and A.A. Allerman, J. Appl. Phys. **120**, 095104 (2016).
[37] E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, and A.J. Schmidt, Appl. Phys. Lett. **110**, 031903 (2017).
[38] E. Heller, S. Choi, D. Dorsey, R. Vetury, and S. Graham, Microelectron. Reliab. **53**, 872 (2013).
[39] D.C. Dumka, T.M. Chou, J.L. Jimenez, D.M. Fanning, D. Francis, F. Faili, F. Ejeckam, M. Bernardoni, J.W. Pomeroy, and M. Kuball, in *2013 CSICS* (IEEE, 2013), pp. 1–4.
[40] H.C. Nochetto, N.R. Jankowski, and A. Bar-Cohen, in *2012 CSICS* (IEEE, 2012), pp. 1–4.
[41] S. Choi, G.M. Peake, G.A. Keeler, K.M. Geib, R.D. Briggs, T.E. Beechem, R.A. Shaffer, J. Clevenger, G.A. Patrizi, and J.F. Klem, IEEE Trans. Components, Packag. Manuf. Technol. **6**,

740 (2016).
[42] M.A. Huque, S.A. Eliza, T. Rahman, H.F. Huq, and S.K. Islam, Solid. State. Electron. **53**, 341 (2009).
[43] W. Liu and A.A. Balandin, J. Appl. Phys. **97**, 073710 (2005).
[44] H. Tokuda, M. Hatano, N. Yafune, S. Hashimoto, K. Akita, Y. Yamamoto, and M. Kuzuhara, Appl. Phys. Express **3**, 121003 (2010).
[45] E.R. Heller, IEEE Trans. Electron Devices **55**, 2554 (2008).
[46] J.D. Cressler and H.A. Mantooth, *Extreme Environment Electronics* (CRC Press, 2017).
[47] K. Son, A. Liao, G. Lung, M. Gallegos, T. Hatake, R.D. Harris, L.Z. Scheick, and W.D. Smythe, Nanosci. Nanotechnol. Lett. **2**, 89 (2010).
[48] D.M. Pozar, *Microwave Engineering* (John Wiley & Sons, 2009).
[49] W. Lu, V. Kumar, R. Schwindt, E. Piner, and I. Adesida, Solid. State. Electron. **46**, 1441 (2002).
[50] S.K. Oh, T. Jang, Y.J. Jo, H.Y. Ko, and J.S. Kwak, IEEE Trans. Electron Devices **63**, 620 (2016).
[51] S.K. Oh, T. Jang, S. Pouladi, Y.J. Jo, H.-Y. Ko, J.-H. Ryou, and J.S. Kwak, Appl. Phys. Express **10**, 16502 (2016).

Figure Captions

Fig. 1. (a) Cross-sectional schematic of the $Al_{0.30}Ga_{0.70}N$ channel HEMT[12] device structure. Field plate structures are denoted by F.P.

Fig. 2. (a) Measured transfer characteristics of the $Al_{0.30}Ga_{0.70}N$ channel HEMT. The dashed lines indicate the gate bias conditions that denote "open channel" (normalized I_{DS}~0.15) and "pinched-off" (normalized I_{DS}~0.9) conditions according to the nomenclature used here. (b) Measured and simulated output characteristics of the $Al_{0.30}Ga_{0.70}N$ channel HEMT under open channel (V_{GS} = 4V) and pinched-off (V_{GS} = 1V) conditions.

Fig. 3. Depth temperature distributions of the $Al_{0.30}Ga_{0.70}N$ and GaN channel HEMTs under open channel conditions with power densities of 0.76 W/mm and 1.61 W/mm, respectively. The depth temperature distributions were measured (meas.) and simulated (sim.) at the drain-side edge of the gate.

Fig. 4. (a) Heat generation profiles for the $Al_{0.30}Ga_{0.70}N$ channel HEMT under open channel and pinched-off conditions normalized with respect to the pinched-off condition for identical power densities (0.76 W/mm). (b) Lateral temperature distributions of the $Al_{0.30}Ga_{0.70}N$ channel HEMT under open channel and pinched-off conditions for identical power densities. (c) Depth temperature distributions of the $Al_{0.30}Ga_{0.70}N$ channel HEMTs under open channel and pinched-off conditions for identical power densities. The depth temperature distributions were measured and simulated at the drain-side edge of the gate.

Fig. 5. (a) Thermal management solutions for the $Al_{0.30}Ga_{0.70}N$ channel HEMT: Case 1 – AlGaN (4 μm buffer) on sapphire (1300 μm); Case 2 – AlGaN (0.5 μm buffer) on diamond (1300 μm); Case 3 – AlGaN (4 μm buffer) on sapphire (1300 μm) flip chip integrated to an AlN carrier; Case 4 – AlGaN (4 μm buffer) on sapphire (1300 μm) flip chip integrated to a diamond carrier. A baseline case (Case 5, not shown) for reference is GaN (4 μm) on SiC (650 μm). (b) Comparison of the thermal resistance for the various thermal management solutions at room temperature (25 °C) base conditions. The HEMT operating power density was 6 W/mm for all cases. (c) The effect of base temperature on the thermal resistance of the $Al_{0.30}Ga_{0.70}N$ channel HEMTs and GaN channel HEMT reference.

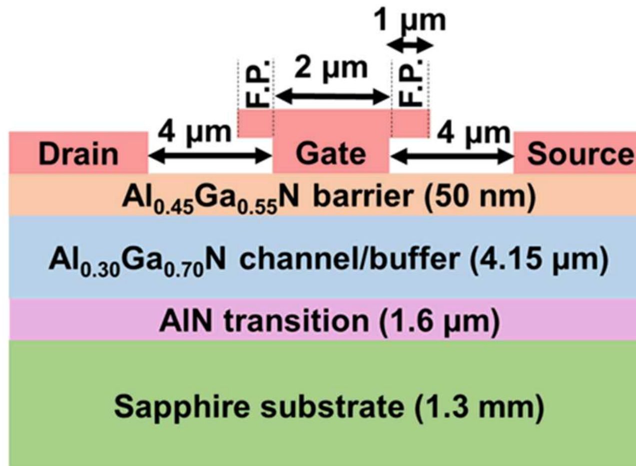

Fig. 1. (a) Cross-sectional schematic of the $Al_{0.30}Ga_{0.70}N$ channel HEMT[12] device structure. Field plate structures are denoted by F.P.

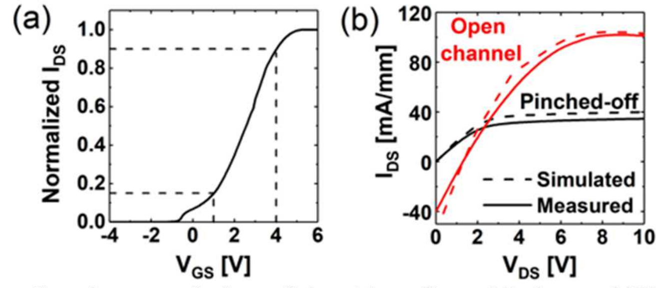

Fig. 2. (a) Measured transfer characteristics of the $Al_{0.30}Ga_{0.70}N$ channel HEMT. The dashed lines indicate the gate bias conditions that denote "open channel" (normalized I_{DS}~0.15) and "pinched-off" (normalized I_{DS}~0.9) conditions according to the nomenclature used here. (b) Measured and simulated output characteristics of the $Al_{0.30}Ga_{0.70}N$ channel HEMT under open channel (V_{GS} = 4V) and pinched-off (V_{GS} = 1V) conditions.

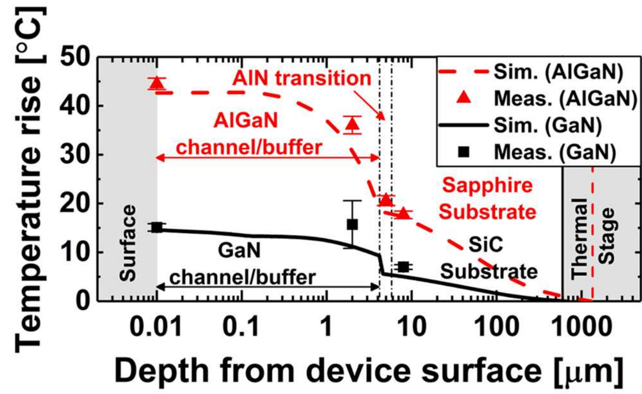

Fig. 3. Depth temperature distributions of the $Al_{0.30}Ga_{0.70}N$ and GaN channel HEMTs under open channel conditions with power densities of 0.76 W/mm and 1.61 W/mm, respectively. The depth temperature distributions were measured (meas.) and simulated (sim.) at the drain-side edge of the gate.

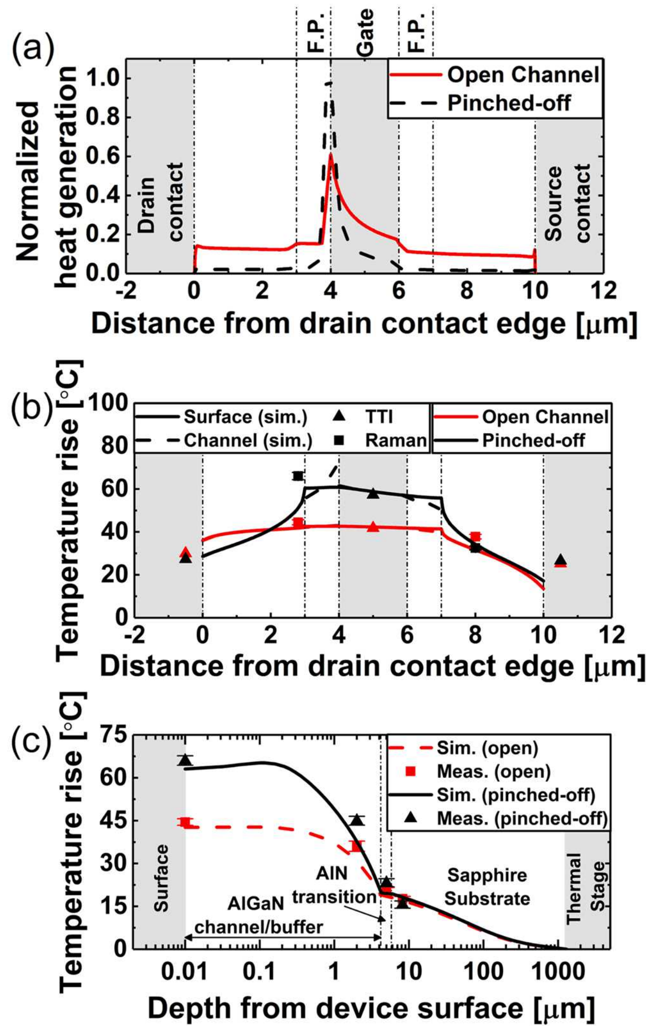

Fig. 4. (a) Heat generation profiles for the $Al_{0.30}Ga_{0.70}N$ channel HEMT under open channel and pinched-off conditions normalized with respect to the pinched-off condition for identical power densities (0.76 W/mm). (b) Lateral temperature distributions of the $Al_{0.30}Ga_{0.70}N$ channel HEMT under open channel and pinched-off conditions for identical power densities. (c) Depth temperature distributions of the $Al_{0.30}Ga_{0.70}N$ channel HEMTs under open channel and pinched-off conditions for identical power densities. The depth temperature distributions were measured and simulated at the drain-side edge of the gate.

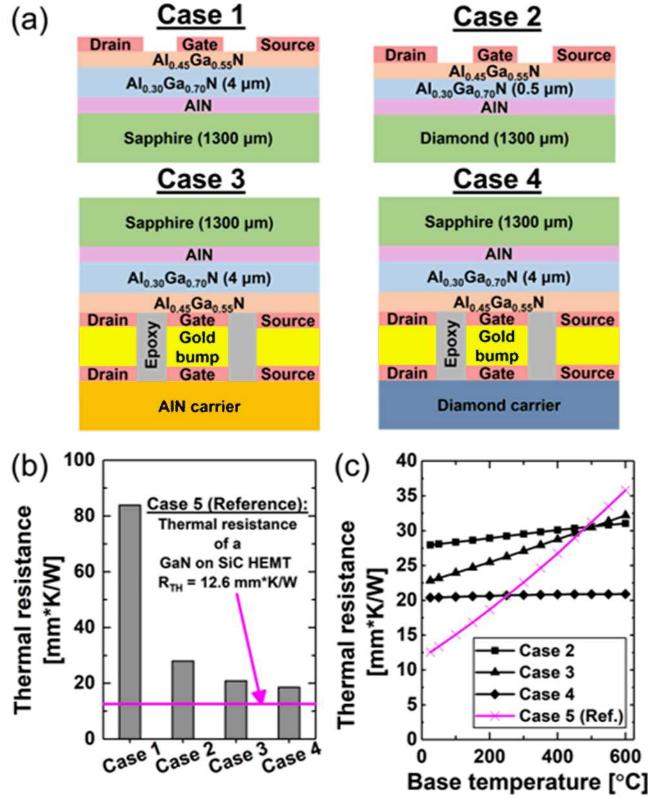

Fig. 5. (a) Thermal management solutions for the $Al_{0.30}Ga_{0.70}N$ channel HEMT: Case 1 – AlGaN (4 µm buffer) on sapphire (1300 µm); Case 2 – AlGaN (0.5 µm buffer) on diamond (1300 µm); Case 3 – AlGaN (4 µm buffer) on sapphire (1300 µm) flip chip integrated to an AlN carrier; Case 4 – AlGaN (4 µm buffer) on sapphire (1300 µm) flip chip integrated to a diamond carrier. A baseline case (Case 5, not shown) for reference is GaN (4 µm) on SiC (650 µm). (b) Comparison of the thermal resistance for the various thermal management solutions at room temperature (25 °C) base conditions. The HEMT operating power density was 6 W/mm for all cases. (c) The effect of base temperature on the thermal resistance of the $Al_{0.30}Ga_{0.70}N$ channel HEMTs and GaN channel HEMT reference.