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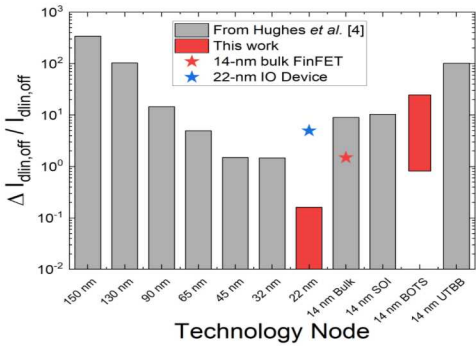

TID-Induced Leakage and Drive Characteristics of Planar 22-nm PDSOI and 14-nm Bulk and Quasi-SOI FinFET Devices

M. P. King, J. G. Massey, A. Silva, E. H. Cannon, M. R. Shaneyfelt, T. D. Loveless, J. Ballast, M. Cabanas-Holmen, S. DiGregorio, W. C. Rice, B. L. Draper, P. Oldgies, K. Rodbell

U.S. DEPARTMENT OF ENERGY

National Nuclear Security Administration

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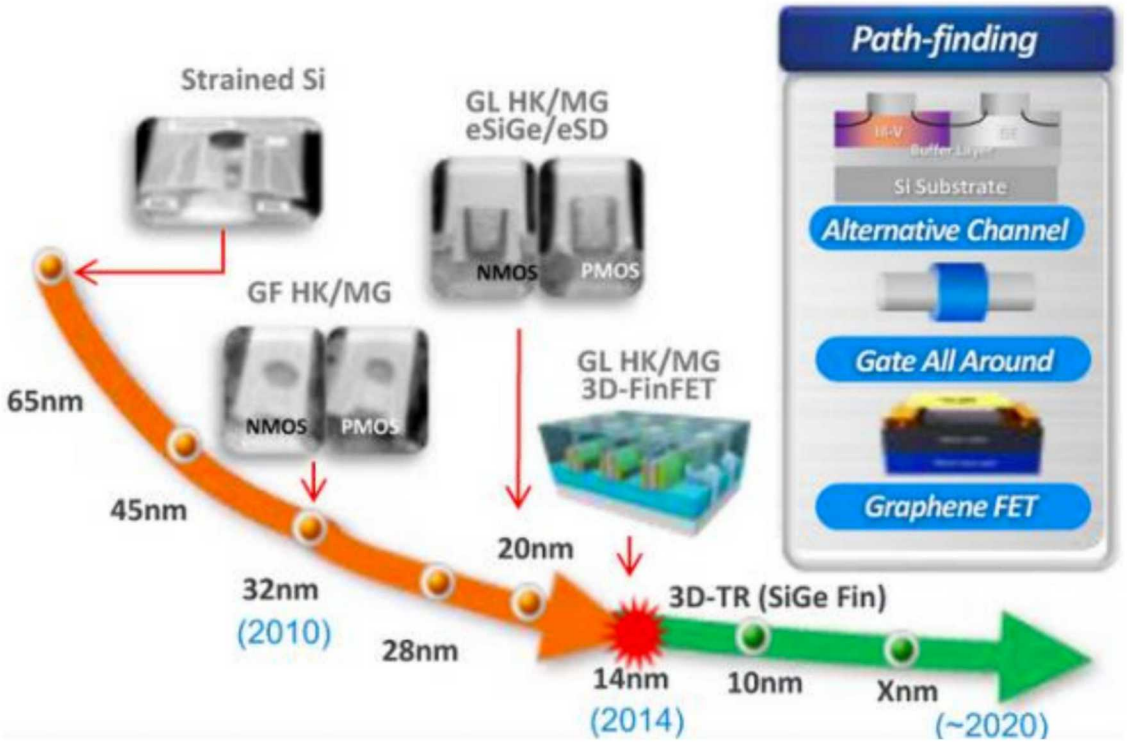
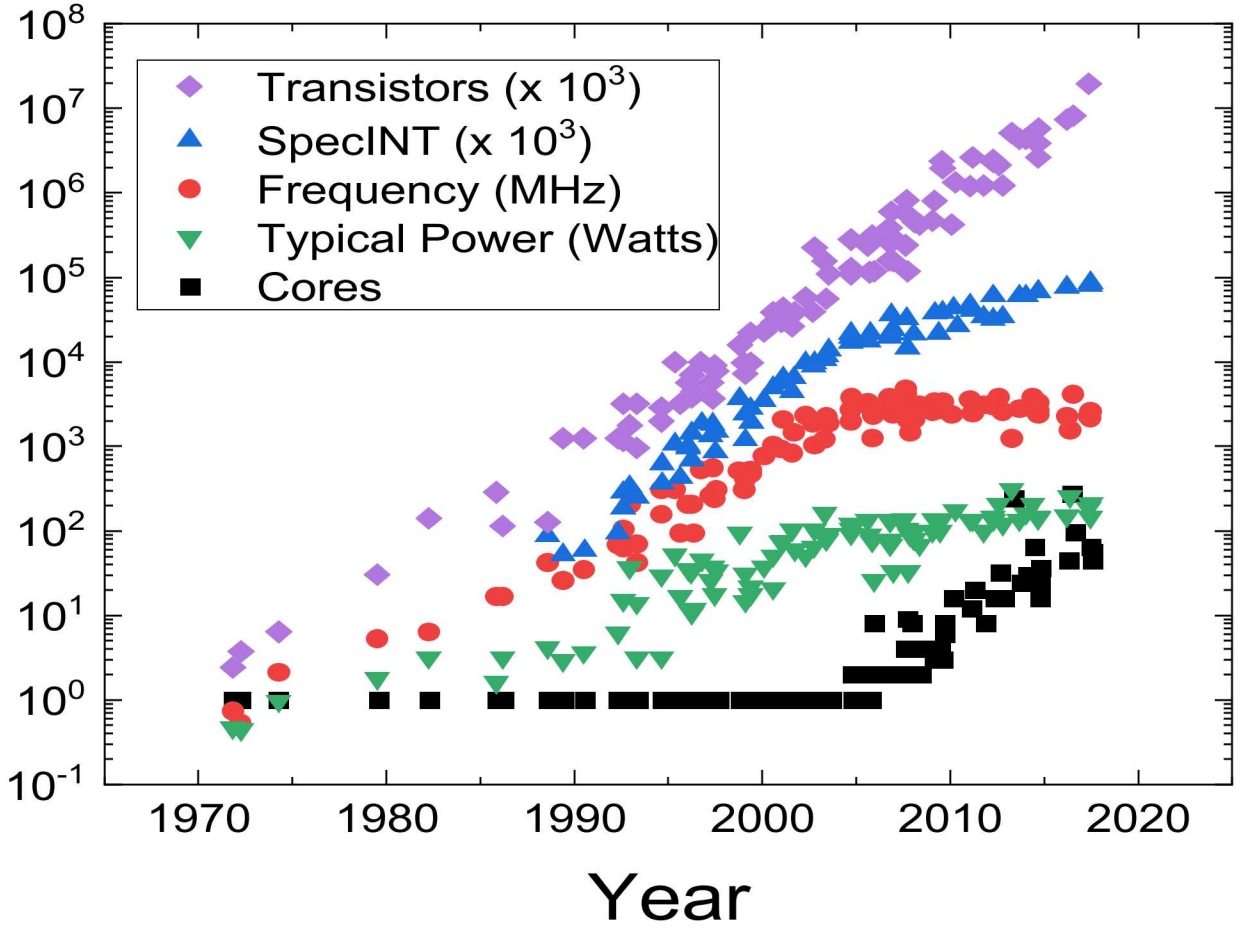
Technology Scaling Trends

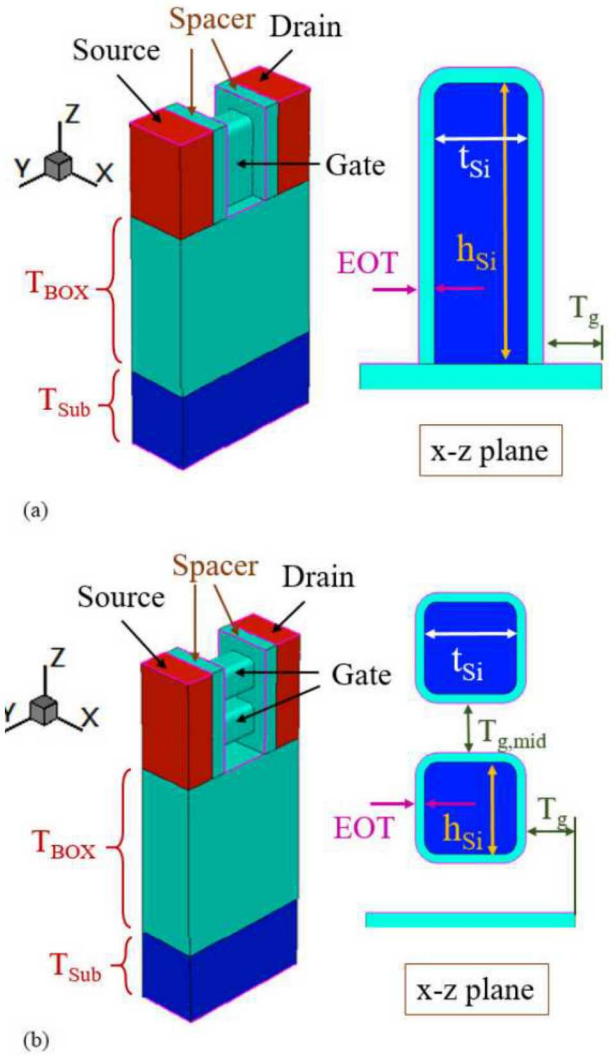




1995	1997	1999	2001	2004	2006	2008	2010	2012	2014
350 nm	250 nm	180 nm	130 nm	90 nm	65 nm	45 nm	32 nm	22 nm	14 nm

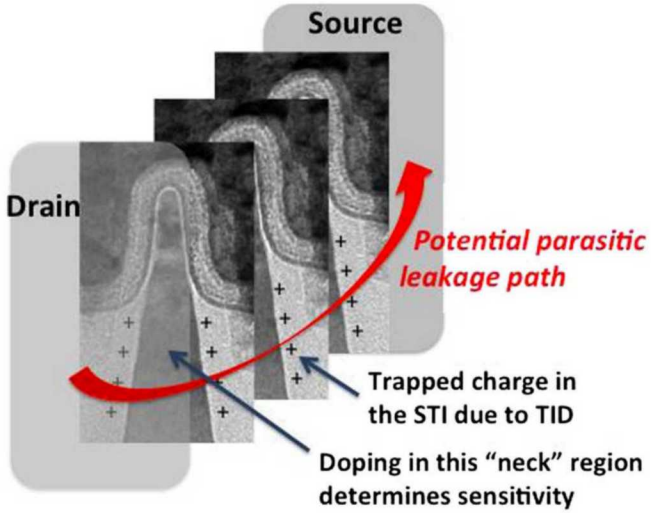
Motivation

- State of the art semiconductor processes have created high performance and low power consumption technologies
- There is a drive to use these technologies for commercial space, defense, and infrastructure
  - Need to understand radiation effects in leading technology nodes



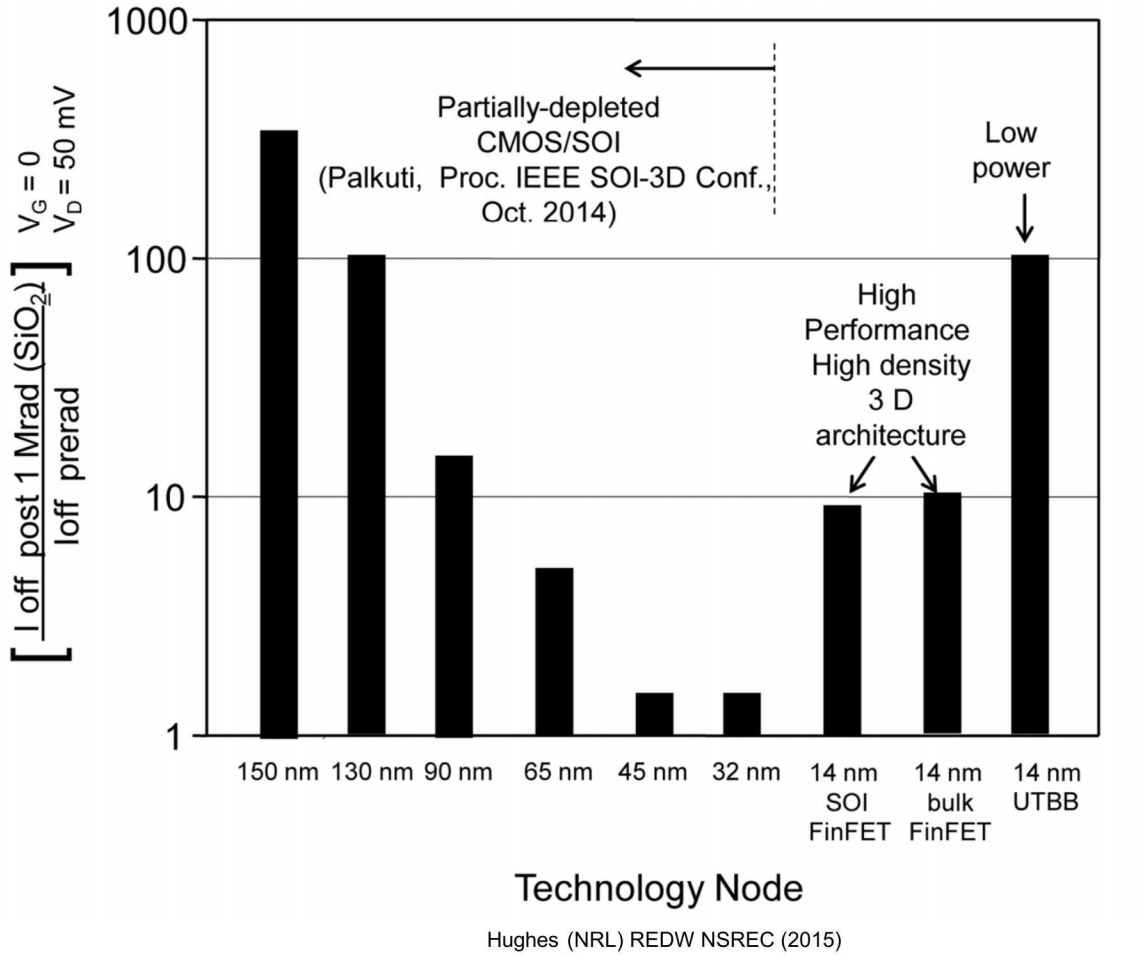
Total Ionizing Dose (TID) Degradation Mechanisms

- Gate degradation from interface traps and positive charge trapping in oxide bulk
  - Mobility ($\mu_{n,p}$) degradation
  - Threshold voltage (V_{th}) shifts
  - Drive current ($I_{ds,on}$) drifts
- Leakage current ($I_{ds,off}$) from charge trapping in shallow trench isolation (and buried oxide in SOI)



Chatterjee, *IEEE TNS*, 2013.

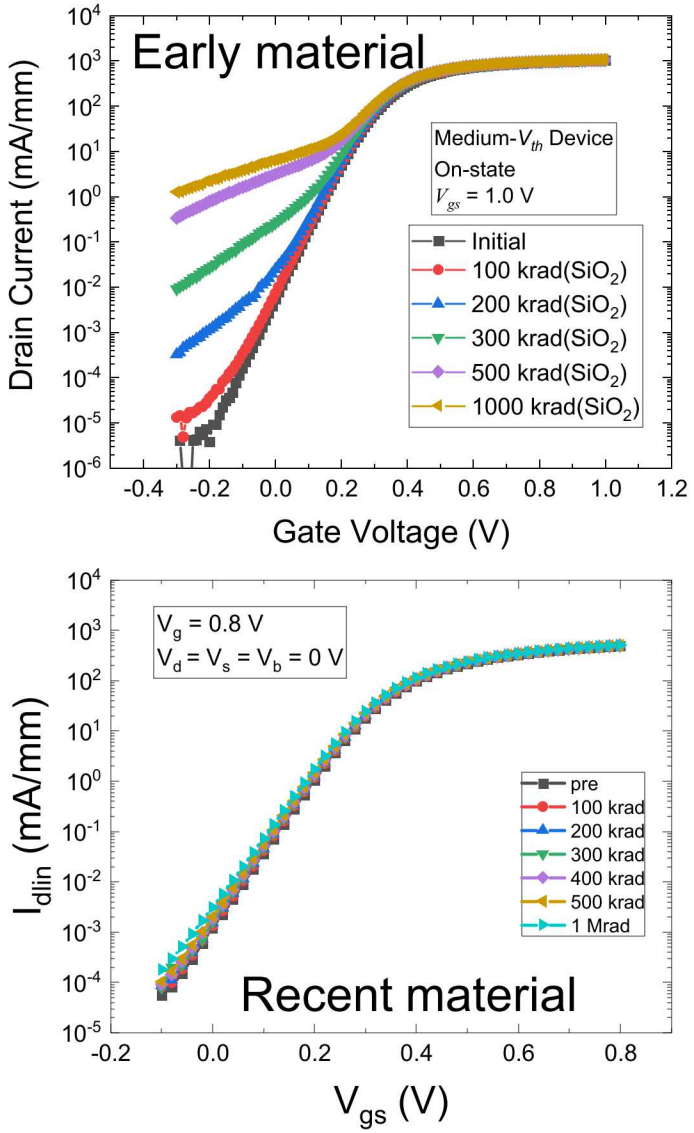
TID vs Technology Scaling



Hughes (NRL) REDW NSREC (2015)

- Scaling trends of off-state leakage vs technology node
- PDSOI exhibits very low leakage for 45- and 32-nm at 1 Mrad
- Migration to FinFETs resulted in a dramatic increase in post-irradiation leakage (early look)
- FDSOI shows leakage comparable to older technologies

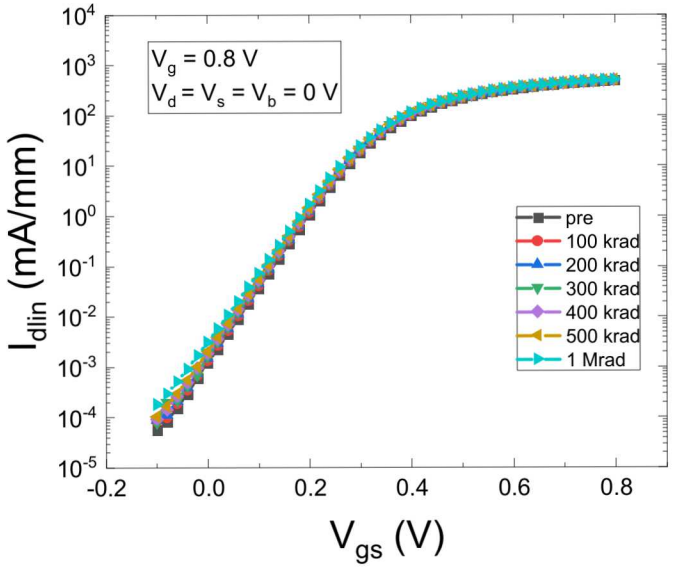
A Tale of Two Commercial Processes

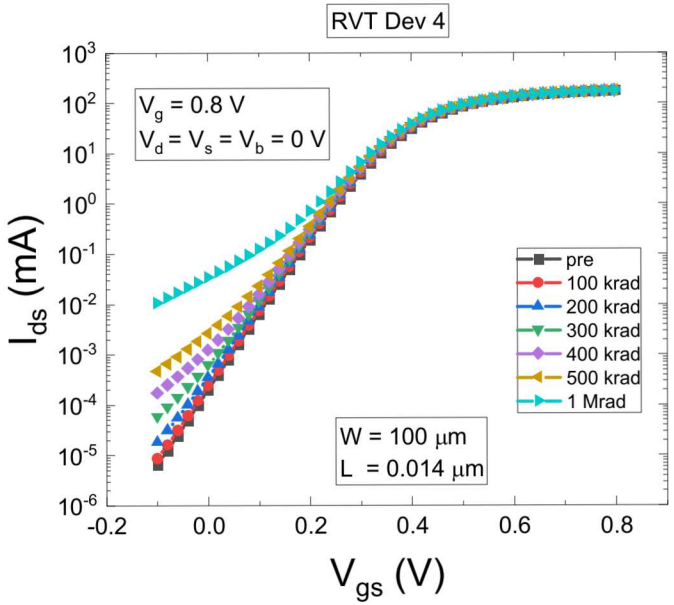


- Typically comes about when they fix a leakage problem
- Radiation-induced leakage is observed above 1 Mrad(SiO_2)
- Impossible to say if TID resilience remains a permanent feature of the technology going forward

Two snapshots of GF 14-nm FinFET technology show *very* different TID results

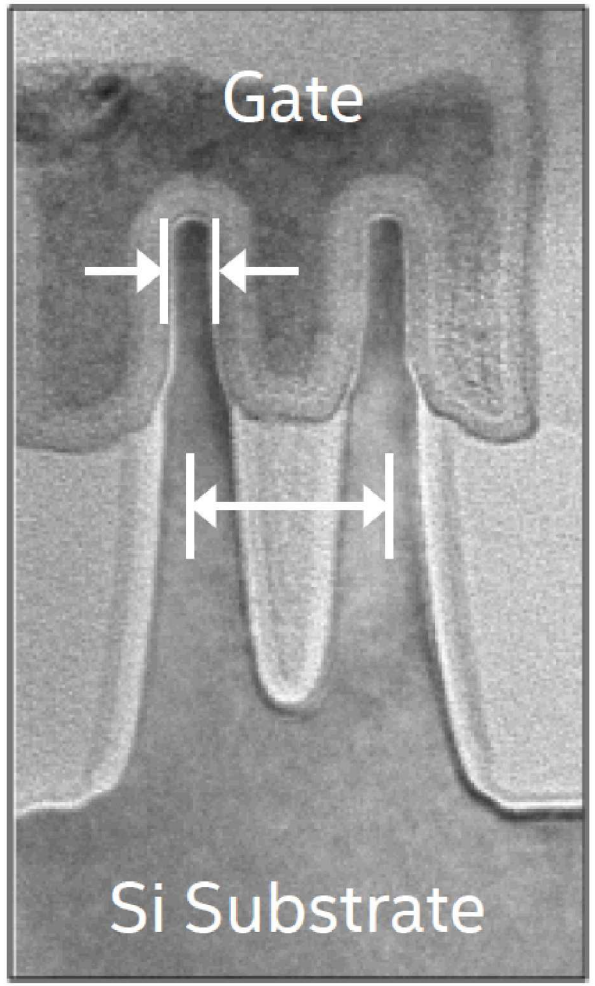
Device Geometry effects





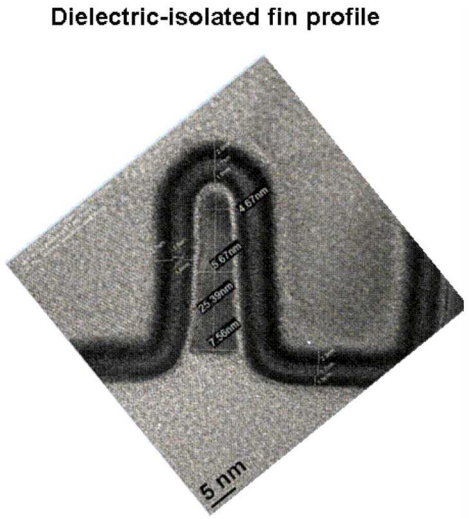
- Interesting device width dependence in many fingered transistors
- Acceptable leakage currents become unacceptable – depending on device V_{th} and geometry
- Actual leakage path is still under investigation – field oxide perimeter is a likely suspect

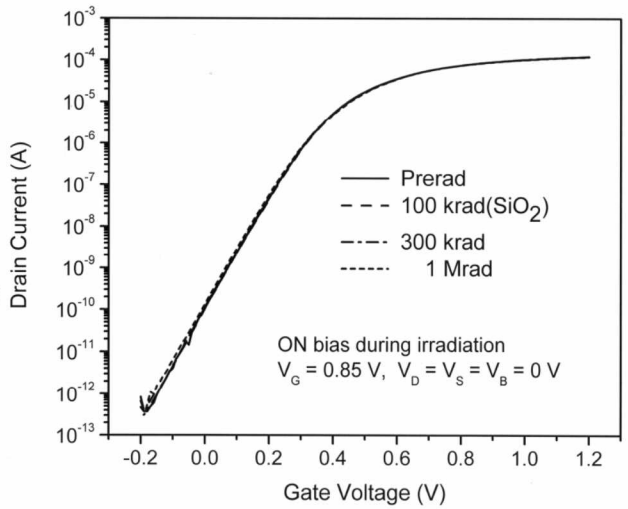
Understanding Isolation Oxides in FinFETs

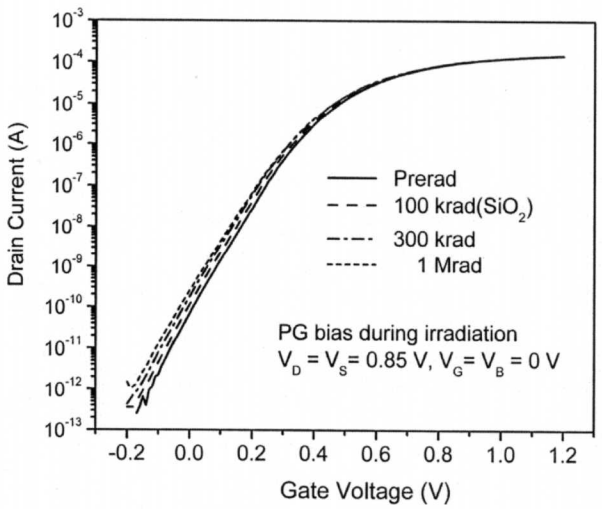


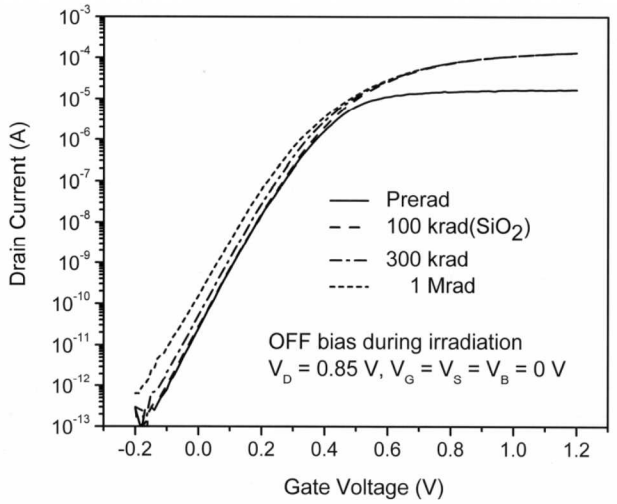
- Flowable oxides sometimes used for dielectric fill step for good coverage of high aspect ratio profile between channels
- A flowable oxide alone would have a poor quality interface and present electrical problems – and TID problems
- Treating the sub-fin / isolation oxide interface more like the gate means *different* materials than were used in any previous process technology and higher quality interface

Return of the SOI FinFETs?





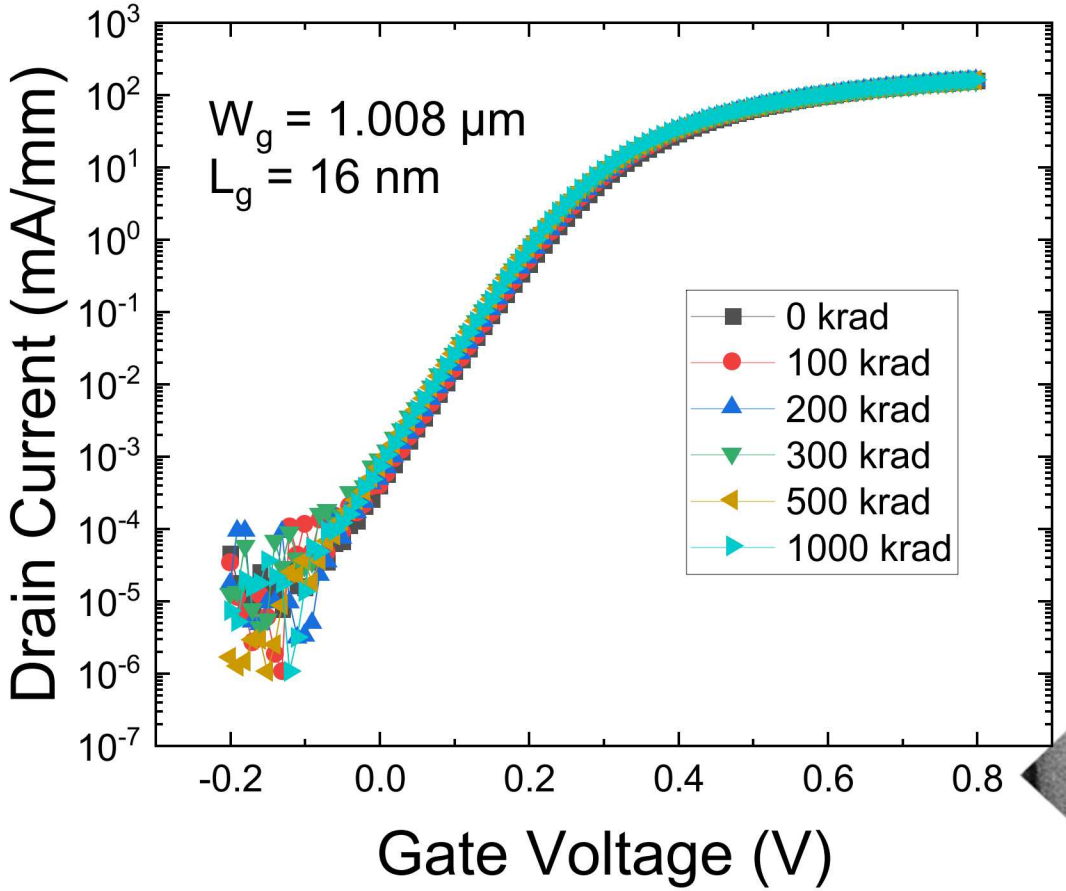




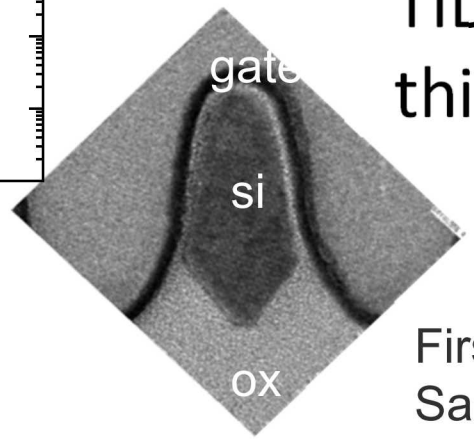
- No commercial source (IBM tech)
- Latchup a non-issue
- TID can be addressed through RHBP
- Possibly a high DRU threshold
  - Good: Reduced charge collection volume
  - Bad: Increased parasitics and floating body

TID Response of BOTS-FinFETs

Quasi-SOI Technology - Experimental



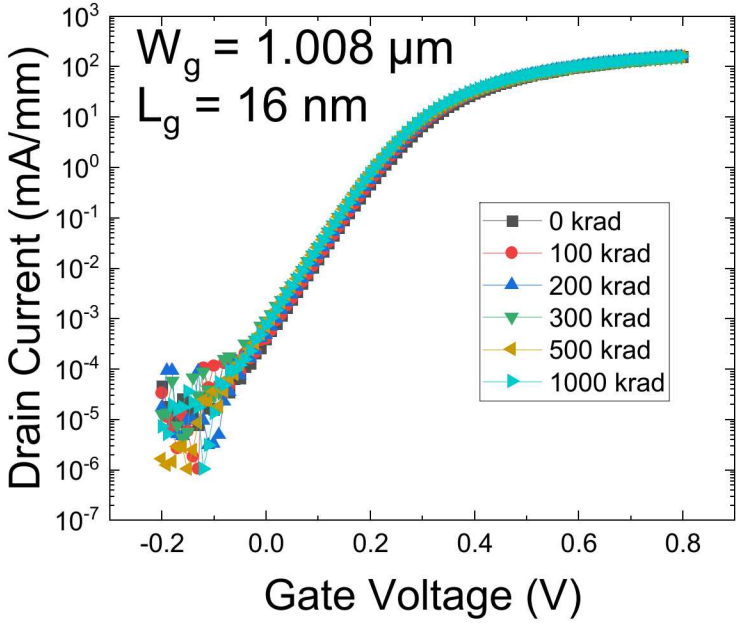
Electrically isolated FinFET on bulk eliminates latch up structures and reduces SEU cross section

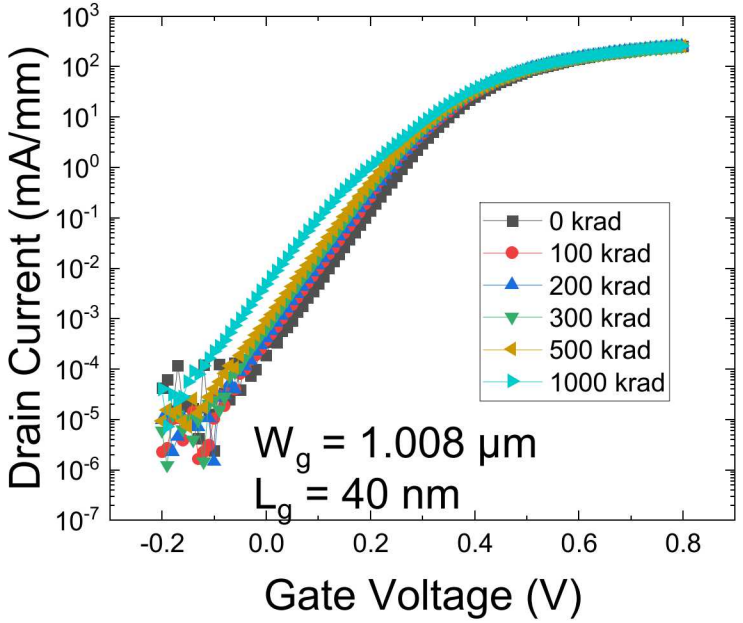


- Dielectrically isolated devices remove latchup and dose rate upset structures limiting current technology
- Initial results show promise for TID – the expected Achilles heel of this technology

First demonstrated by IBM, GF, and Samsung publication in VLSI 2014

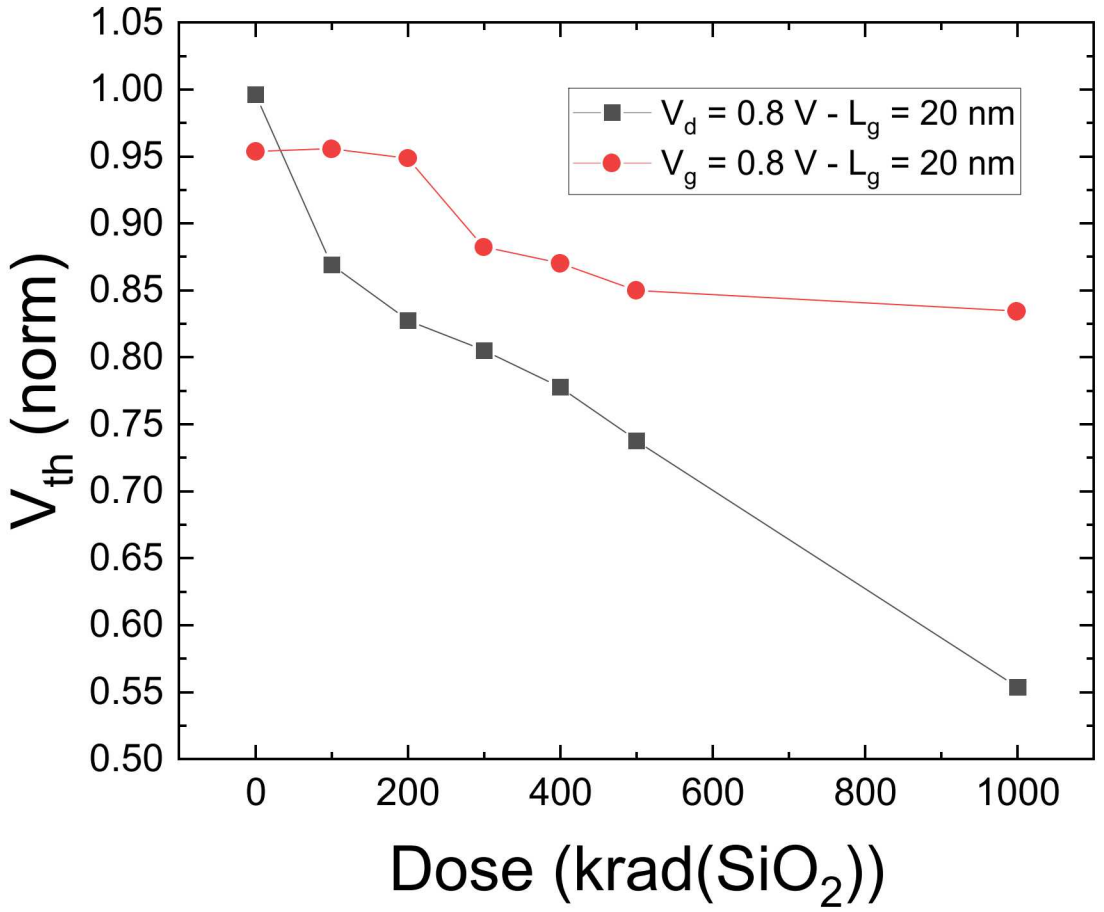
Transistor Length Dependence





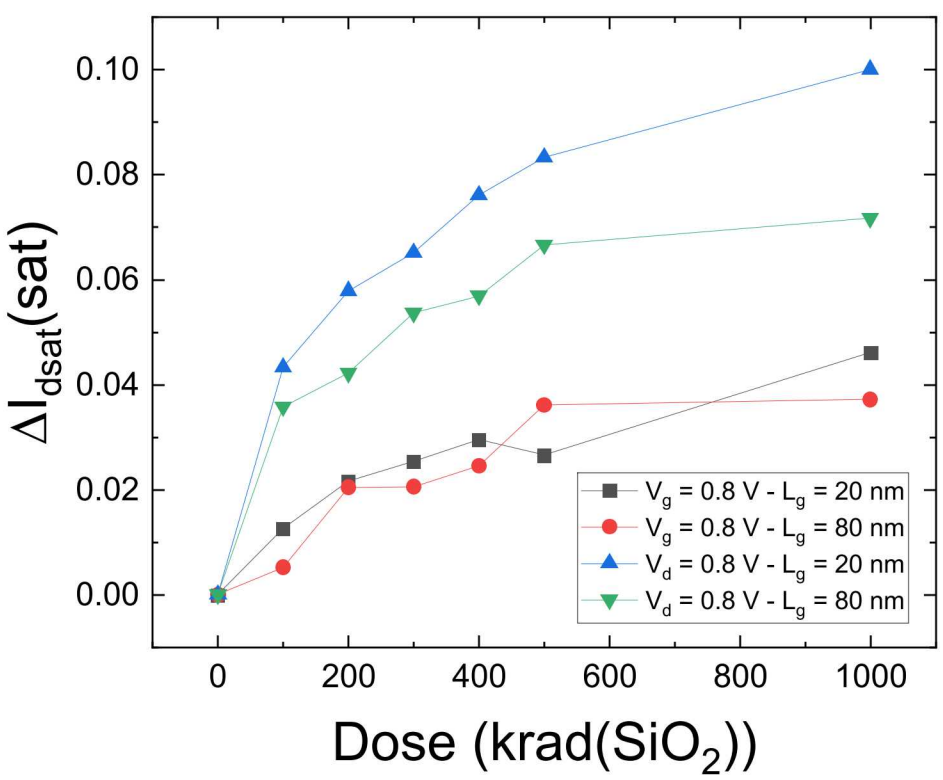
- Device length leads to interesting trends for threshold voltage and leakage current
- Parasitic leakage current does not scale as W/L like normal FET -> alternative leakage path and parasitic transistor definition

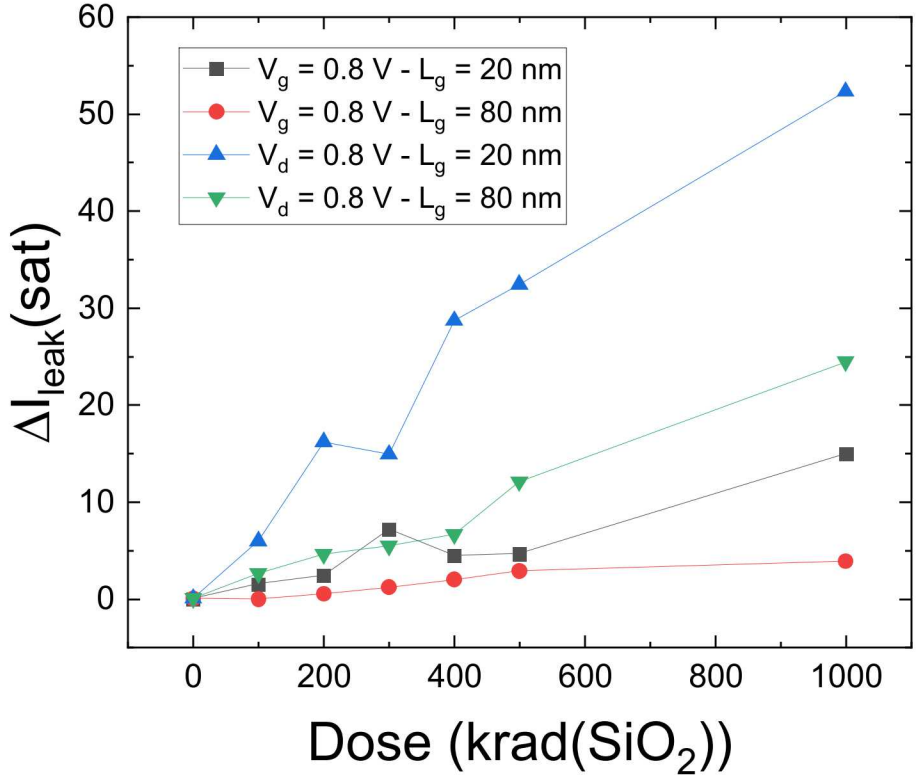
Threshold Voltage Influenced by Buried Oxide Trapped Charge



- Devices irradiated in the off-state (V_d = 800 mV, V_g = V_s = 0 V) exhibit substantially stronger ΔV_{th} than devices irradiated in the on-state (V_g = 800 mV, V_d = V_s = 0 V)
- TCAD simulations show electric field penetration of the “BOX” for the off-state irradiation
- Leads to greater charge yield and larger impact on device V_{th} and I_{leak}(sat)

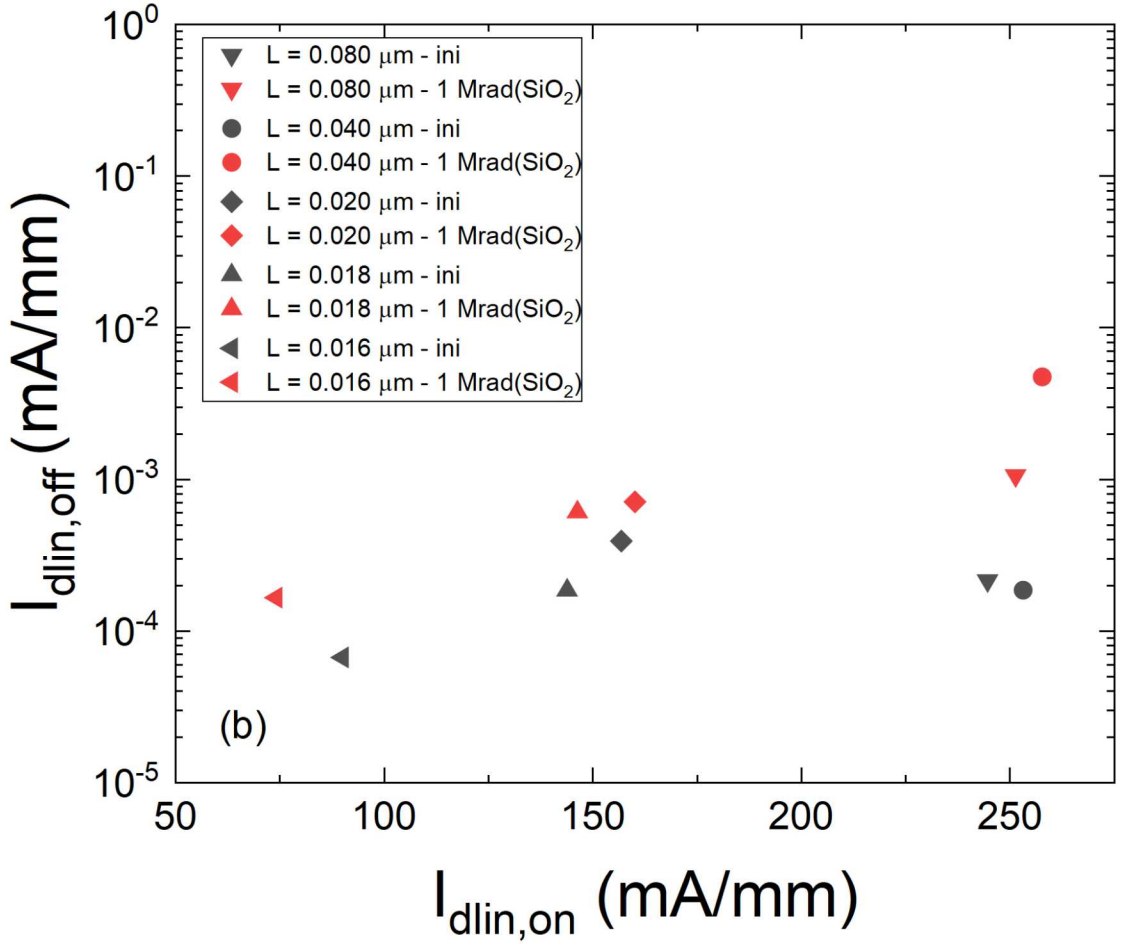
Saturation Response – Long vs Short Channel Devices





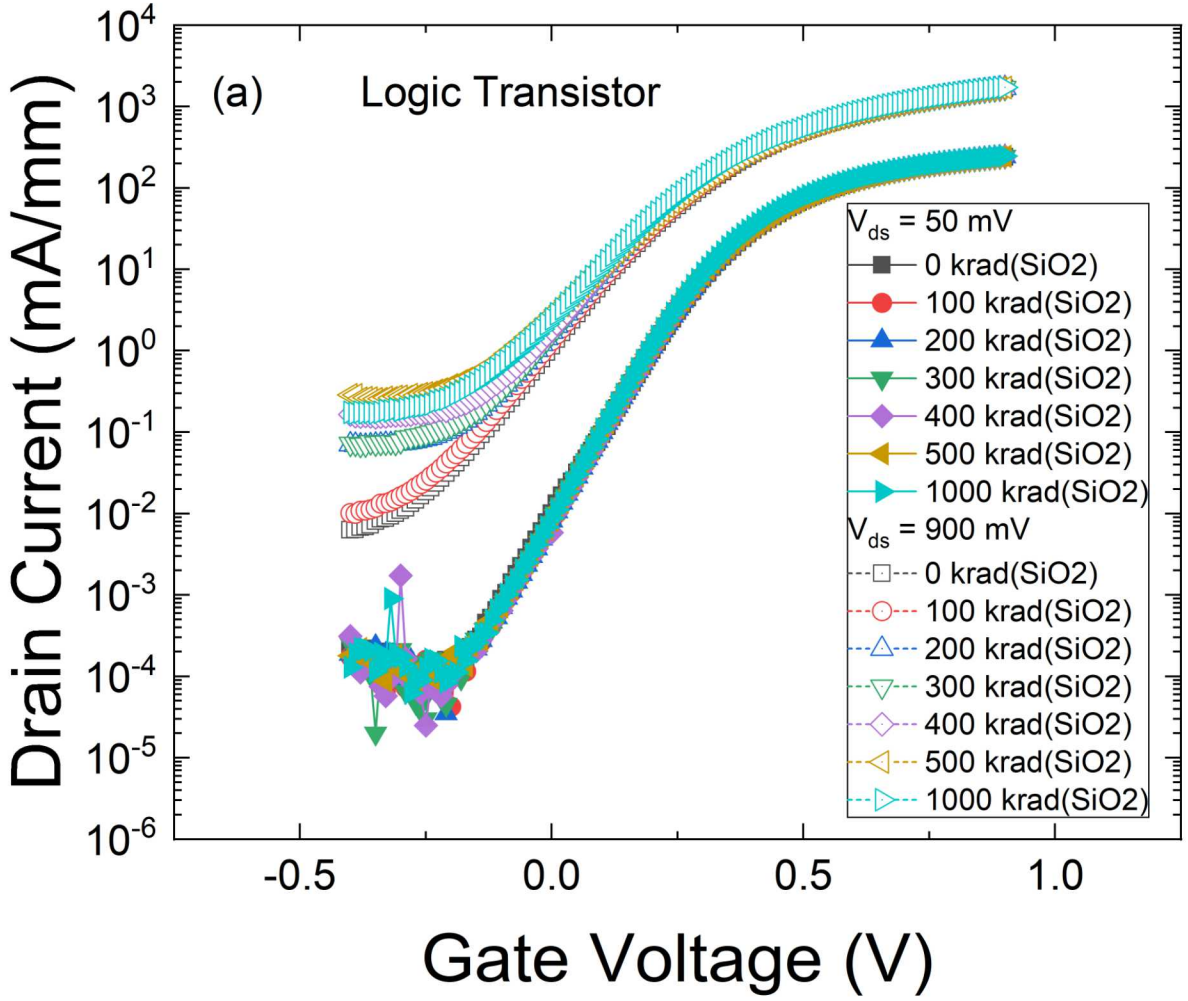
- Irradiation condition has more impact on post-irradiation drive current than channel length with the worst case ΔV_{th} in the *off-state*
- Leakage is highest in the off-state as well – geometry dependence ~ $1/L_g$

Parametric Extraction – BOTS-FinFET

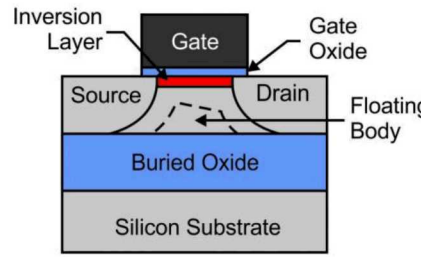


- Dependence on the effective channel length
  - Interesting transistor geometry effects
  - Current analysis is limited by available geometries
- Response to TID behaves more like reports of TID FDSOI than bulk devices

TID Response – IBM 22-nm PDSOI



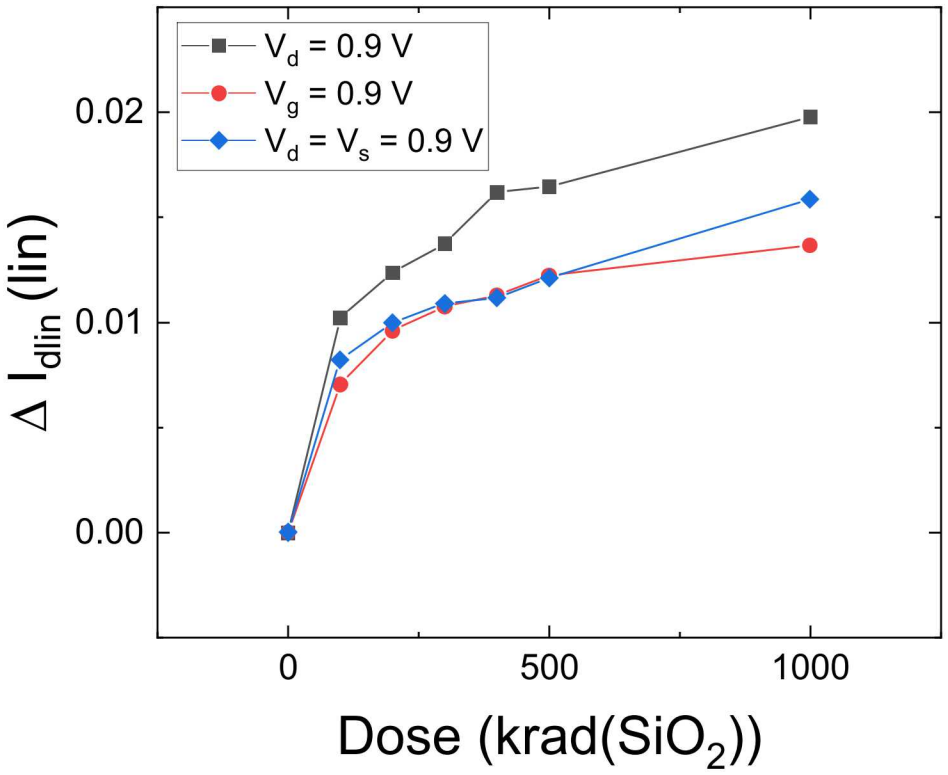
- PDSOI has traditionally shown the most promise for radiation hardness
- First, and only, public look at IBM 22-nm PDSOI shows very good linear response, saturation shows more shift
- High V_{ds} *I-V* characteristics show front-back gate coupling

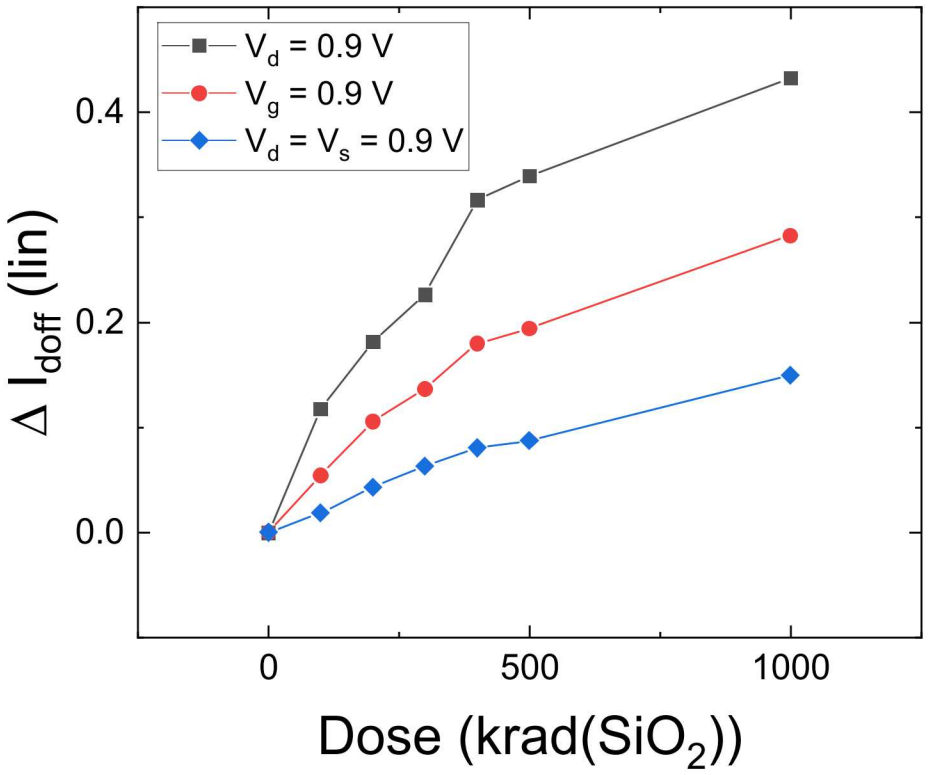


Floating body voltage influences the inversion layer - not fully depeleted

PDSOI

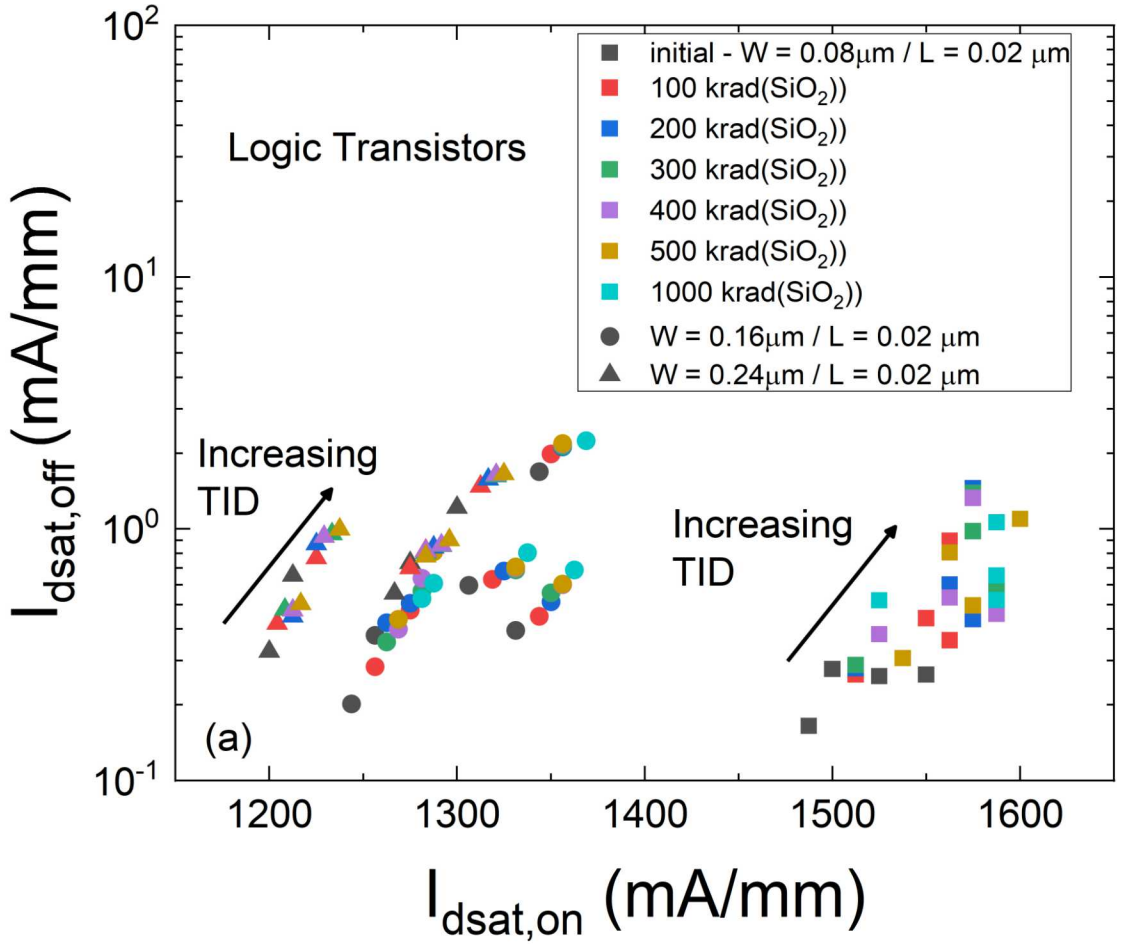
Worst Case – Linear Device Operation





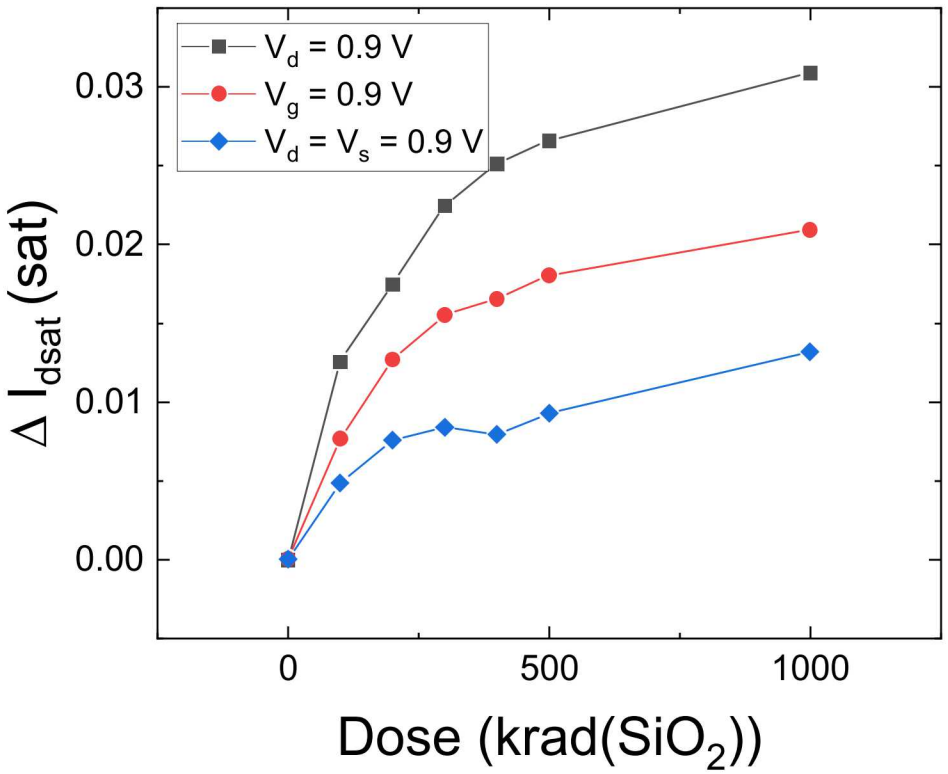
- Devices are shown to have a worst case leakage (I_{doff}) and drive (I_{dlin}) for the off-state irradiation condition
- Neither drive current or leakage are significantly effected at 1 Mrad(SiO_2)

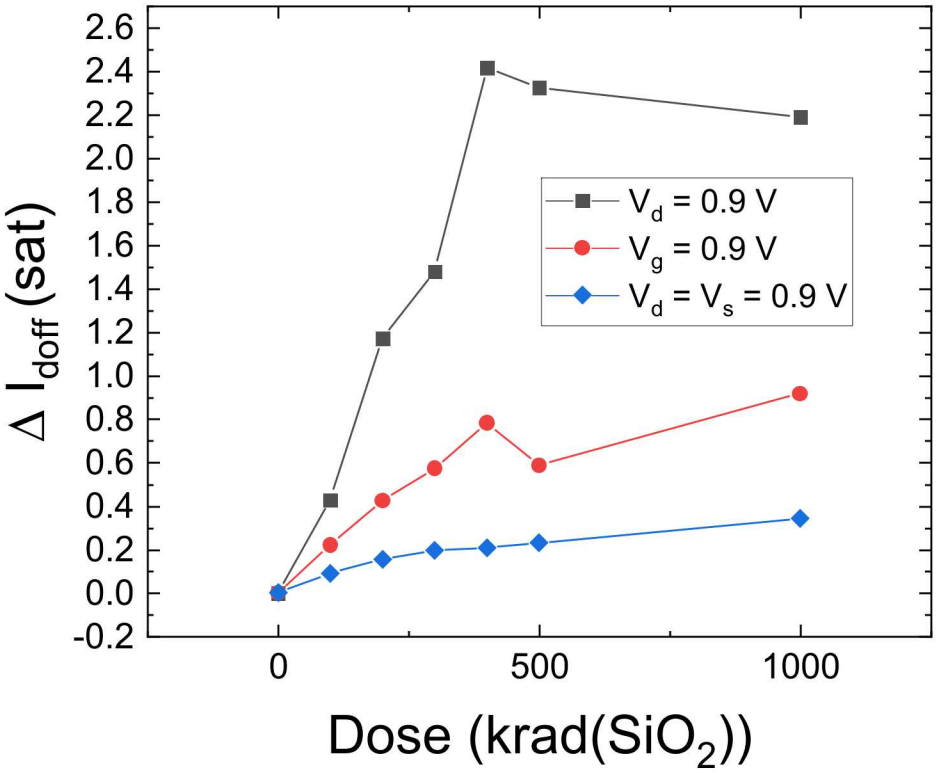
Parameter Extraction – 22 nm PDSOI



- Devices show excellent post-irradiation leakage current
- Observed V_{th} is small ~ 10-20 mV consistent with observed changes in I_{dsat}
- Post-irradiation leakage only significant in saturation mode – linear mode experiences only a small ΔV_{th}

Saturation Response – Sidewall and Backgate Coupling





- Drive current in saturation is again minimally effected at 1Mrad(SiO_2)
- Leakage current *does* increase up to 240% in the off-state condition
- Leakage only shown to be significant under high drain bias implying coupling of the sidewall and/or backgate in the transfer curve

Conclusions

- Logic and IO devices for planar 22-nm PDSOI technology show order of magnitude reduction of TID-induced leakage over the previous two generations of this technology
- Reduction in TID-induced leakage in bulk 14-nm FinFET from GF making it comparable in post-irradiation performance to 45- and 32-nm PDSOI technologies
- Design width and length dependences observed in *bulk* and *quasi-SOI transistors* – leakage paths still under investigation
- Results from an experimental quasi-SOI FinFET technology also show promise for reliable operation in radiation environments