Design, Analyses and Validation of Sliding Mode Control for a DAB DC-DC Converter

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***Abstract*— In this paper, a comprehensive voltage control loop design for a dual active bridge (DAB) DC-DC converter is proposed using the sliding mode control (SMC), where the coefficients are formed to ensure both small signal and large signal stability of the system. The major objectives of the proposed SMC are to enhance the converter dynamics and attain a tight output voltage regulation under fast load fluctuations or during start-up. In addition, dynamic performance of the system is examined considering the steady state error and overshoot. The proposed control method is capable of achieving soft-switching operation by determining the effective duty phase displacement range. To verify the proposed method, a hardware prototype of a DAB converter is developed and evaluated, and the effectiveness of the loop design is validated by the experiment. It is observed that overshoot is eliminated in the start-up test and the fast settling time is achieved.**

***Index Terms*—Sliding mode control, DAB, DC-DC converter, robustness.**

I. INTRODUCTION

In recent years, the DAB DC-DC converter [1], [2] has drawn much attention for high power applications, i.e. electric vehicle charger, energy storage system. It has the advantages of galvanic isolation, high efficiency and wide range output voltage. Moreover, the power inductor of the DAB converter can be integrated as the leakage inductor in the transformer [3], which leads to the reduction in cost and volume.

Many researches have been conducted in the DAB converter, including the topological variations, control and system optimization [4]–[9]. Aiming at the optimization of the minimum conduction loss and copper loss, a set of closed-form expressions for the optimal control parameters are derived and implemented in [4] to facilitate the direct application to a given DAB converter. The paper further presents the properties of the proposed modulation scheme with respect to the switching loss. Moreover, a comprehensive triple-phase-shift control method is proposed in [9] to reduce the current stress and achieve soft-switching, where all effective switching modes are investigated. In terms of the DAB converter control, it is fundamentally examined using different methods and models, to achieve the minimum conduction loss, low transformer ringing, low component current/voltage stress, extended soft-switching range and efficiency optimization over wide input/output voltage range [4], [9]–[12]. However, most of them are mainly focused on the power flow management and steady state performance of the DAB converter, which may have limited dynamic response performance. In most cases, PI compensators are adopted [13] as the controllers. However, they fail to achieve the desired performance under large parameter variations and load disturbances [14]. Another choice is to implement the sliding mode controllers on DAB converter for better dynamic performance. In [15], a SMC based control technique is proposed for modular DAB converters, which is aimed to balance and regulate the output voltage. However, it does not cover the details of synthesizing procedure among the control and power stages, and the system stability is not clear.

To resolve the aforementioned concerns, a comprehensive SMC based control loop scheme is proposed in this manuscript, including the proper modelling to capture the dynamics, stability and robustness analyses. The major objectives of the proposed SMC are to improve the converter dynamics and ensure a tight output voltage regulation under load disturbances or during start-up. Furthermore, the essence of surface coefficients and their selection criterion are comprehensively disclosed. Explicitly, a phase-shifted regulation function is formulated to supervise the system dynamics while maintaining the asymptotical stability over a wide range of operating conditions. In addition, dynamic performance of the system is examined considering the steady state error and overshoot. The proposed control method is capable of achieving soft-switching operation by determining the effective duty phase displacement range.

II. THE PROPOSED SLIDING MODE CONTROL SCHEME FOR A DAB DC-DC CONVERTER

Fig.1 shows a simplified circuit of the DAB DC-DC converter consisting two full bridges and a magnetic tank, where L_s denotes the power inductor to satisfy the maximum power transfer requirement. Note that the power inductor at each side can be obtained through the leakage inductance of the transformer. $Q_{1\sim8}$ are the active MOSFETs.

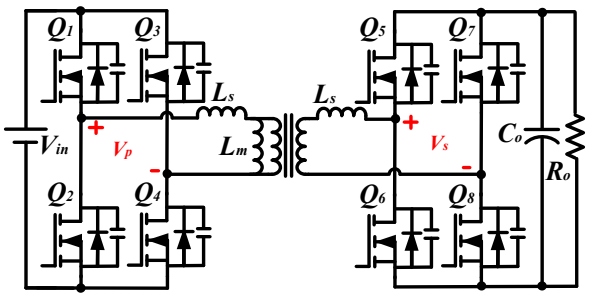


Fig. 1. The topology of a DAB DC-DC converter.

In this work, single phase-shifted modulation (SPS) is implemented to simplify the analyses. D denotes the phase-shifted ratio and DT is defined as the phase difference time between primary voltage V_p and secondary voltage V_s, where T is the switching period and $T = \frac{1}{f}$. Typical operating waveforms are shown in Fig. 2.

A. Sliding Surface Design with a Sampled-data Based Model

Theoretically speaking, accurate modelling is essential for the sliding surface and control loop design of DAB converter. Considering the conventional state-space averaging method has the limitation of predicting the inductor current and system dynamics, a modeling technique based on data sampling is developed in [16] to precisely retain the steady state and dynamic characteristics of a DAB converter. There are several assumptions to be mentioned as follows,

- Turns ratio is designed to be 1:1. Due to the symmetric structure, the primary leakage inductance in the transformer is approximately equal to the secondary one.
- The equivalent series resistance of the conducting path, R_c, including the ON-resistance of switches and parasitic resistance of the transformer, is considered in this model.
- The parasitic inductance and capacitance are ignored.

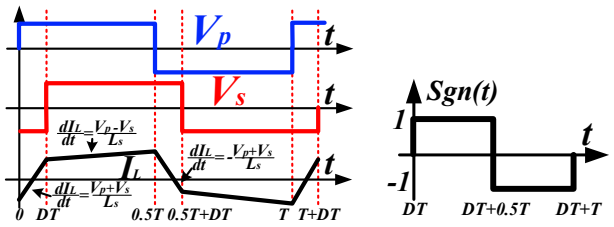
The state variables of the system are the primary inductor current I_L, and the output voltage V_o. Based on [16], the revised sampled-data model can be transformed into the state space representation considering the identical primary and secondary inductors,

$$\begin{cases} \frac{dX}{dt} = AX + BU \\ Y = CX \end{cases} \tag{1}$$

where, X is the state variable matrix of the system, $X = [\, I_L(t) \quad V_o(t)]^T$, U is the input matrix, Y is the output matrix, and A, B, C are the parameter matrices as follows,

$$A = \begin{bmatrix} \frac{-R_C}{2L_S} & \frac{-Sgn(t)}{2L_S} \\ \frac{Sgn(t)}{C_o} & \frac{1}{-C_o R_o} \end{bmatrix}, B = \begin{bmatrix} \frac{(-2D+1)Sgn(t)}{2L_S} \\ \frac{D(1-D)}{4fC_o L_S} \end{bmatrix},$$
$$C = [0\ 1], Y = [V_o], U = [V_{in}] \tag{2}$$

Therefore, the eigenvalues of matrix A are observed to be in the left-half-plane, making the system stable with respect to the large signal model. In Fig. 2, the waveforms of inductor current over each half duty cycle are identical, regardless of the phase difference. As a result, the modelling can be established for either one of half duty cycles without loss of generality, i.e. from DT to $DT + 0.5T$. To further simplify the analyses, the first half duty cycle operation is considered, where $Sgn(t)$ is taken as +1.



(a) (b)

Fig. 2. SPS-based modulation: (a) Operating waveforms; (b) Waveform of $Sgn(t)$.

The predetermined sliding mode surface S is fundamentally defined by the error combination between the output voltage and its reference value V_o^* in Eq. (3) and independent with the initial conditions,

$$S = \alpha_1(V_o^* - V_o) + \alpha_2 \int_0^t (V_o^* - V_o)dt \tag{3}$$
$$\frac{dS}{dt} = -\alpha_1 \frac{dV_o}{dt} + \alpha_2(V_o^* - V_o) \tag{4}$$

where α_1 and α_2 are the sliding surface coefficients. The surface is chosen due to: (i) at the steady state, $\dot{S} = 0$ always hold; (ii) the existence of both proportional and integral coefficients gives a flexibility to adjust the loop bandwidth [17]. Moreover, to satisfy the existence condition of SMC, both S and $\dot{S}$ need to be zero in steady state. The unified constraint [18] to ensure the existence condition of the sliding mode is expressed as,

$$S \cdot \dot{S} < 0 \tag{5}$$

The discrete values of the control variable can be obtained as,

$$u = \begin{cases} 1, & S > 0 \\ 0, & S \le 0 \end{cases} \tag{6}$$

Therefore, he proposed sliding mode control diagram can be constructed using the defined sliding mode surface, as shown in Fig. 3.

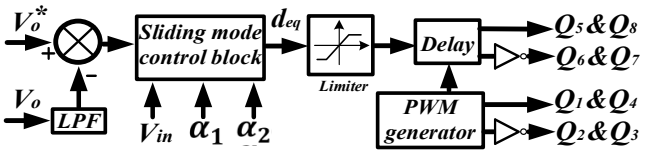


Fig. 3. The proposed sliding mode control structure of DAB converter.

The phase-shifted control is presented in Eq. (6), which generates the signal 'u' depending on the polarity of S. For a positive value of S when V_o is less than V_o^*, the phase-shifted ratio D is increased by a step size of 0.001 in the

implementation, which is defined by $u = 1$. Likewise, when V_o is higher than V_o^*, D is decreased by 0.001. At the equilibrium point, $\dot{S} = 0$,

$$\dot{S} = -\alpha_1 \dot{V}_o + \alpha_2 (V_o^* - V_o) = 0 \tag{7}$$

Recall Eq. (1), at the equilibrium point the state variables can be computed as,

$$\begin{cases} I_L = \frac{(-2D+1)V_{in} - V_o}{2R_c} \\ \dot{V}_o = \frac{I_L}{C_o} - \frac{V_o}{C_o R_o} + \frac{D(1-D)V_{in}}{4fC_o L_s} \end{cases} \tag{8}$$

where $\dot{V}_o$ contains the ripple information in SMC and is not zero. The equilibrium phase-shifted ratio D_{eq} is achieved by plugging Eq. (8) into Eq. (7), where the following quadratic equation with respect to D_{eq} is shown as,

$$D_{eq}{}^2 + \left(\frac{4fL_s}{R_o} - 1\right) D_{eq} + 2fL_s \left[-\frac{1}{R_o} + \frac{3V_o}{V_{in}R_o} + \frac{2C_o}{V_{in}}\frac{\alpha_2}{\alpha_1}(V_o^* - V_o)\right] = 0 \tag{9}$$

$$D_{eq} = \frac{1 - \frac{4fL_s}{R_o} + \sqrt{\left(\frac{4fL_s}{R_o} - 1\right)^2 - 8fL_s\left[-\frac{1}{R_o} + \frac{3V_o}{V_{in}R_o} + \frac{2C_o\alpha_2}{V_{in}\alpha_1}(V_o^* - V_o)\right]}}{2} \tag{10}$$

and the other solution is negative which is not relevant for the discussion. The equilibrium phase-shifted ratio D_{eq} must be kept among the boundaries considering the monotonicity of the gain function: $0 < D_{eq} < 0.5$, which defines the constraints of sliding surface coefficients α_1 and α_2.

Moreover, the existence condition of real roots needs to be satisfied,

$$\left(\frac{4fL_s}{R_o} - 1\right)^2 - 8fL_s\left[-\frac{1}{R_o} + \frac{3V_o}{V_{in}R_o} + \frac{2C_o}{V_{in}}\frac{\alpha_2}{\alpha_1}(V_o^* - V_o)\right] > 0 \tag{11}$$

B. Stability Analyses of the Proposed SMC Loop

1) Sliding Motion Equation

The stability of the sliding motion equation can be investigated using Lyapunov function,

$$\bar{V}(S) = \frac{1}{2}S^2(x,t) \tag{12}$$

where, $\bar{V}(S) > 0$ for $S(x,t) > 0$. x denotes the state variable vector. Furthermore, an efficient condition for the asymptotic stability of the system can be derived as follows,

$$\frac{d\bar{V}(s)}{dt} = \frac{1}{2}\frac{d}{dt}\left(S^2(x,t)\right) \le -\varepsilon|S(x,t)| \tag{13}$$

where, ε is a strictly positive real constant, which determinates the convergence rate of the trajectory to the sliding surface. This inequality refers that all trajectories are forced to move towards the sliding surface, which confirms the stability and reachability of the sliding surface motion. Another important condition to be verified is whether it meets surface motion requirement from Eq. (5). Applying the error expression $e(t) = V_o^* - V_o$ and its derivative $\dot{e} = -\dot{V}_o = -\frac{I_L}{C_o} + \frac{V_o}{C_o R_o} - \frac{D(1-D)V_{in}}{4fC_o L_s}$, a range of these coefficients for the sliding motion existence condition is achieved. Since this inequality cannot confirm the small signal stability with the same set of parameters, the analyses on the small signal stability are performed in the following subsection.

2) Small Signal Model

Taking the advantages of the sampled-data based model, the small signal modeling can be accurate in terms of setting the phase and gain margin, and the loop bandwidth, which are the governing factors for the loop stability under a perturbation in any state variable [19], [20]. Consequently, based on the state space equations, the state variable $V_o(s)$ can be derived as,

$$V_o(s) = \frac{V_i\left[\frac{-2D+1}{2L_sC_o} + \frac{D(1-D)\left(s+\frac{R_C}{2L_s}\right)}{4fL_sC_o}\right]}{s^2 + s\left(\frac{R_C}{2L_s} + \frac{1}{R_oC_o}\right) + \frac{R_C}{2L_sR_oC_o}}, \Delta V_o(s) = \frac{\partial V_o(s)}{\partial D}\Delta D \tag{14}$$

where, $\Delta V_o(s)$ represents the disturbance of the state variable using the partial derivative at certain constant D. Thus, the plant transfer function $T_p(s)$ of the SMC system can be expressed as,

$$T_p(s) = \frac{\partial V_o(s)}{\partial D} = \frac{V_i\left[\frac{-2}{2L_sC_o} + \frac{(1-2D)\left(s+\frac{R_C}{2L_s}\right)}{4fL_sC_o}\right]}{s^2 + s\left(\frac{R_C}{2L_s} + \frac{1}{R_oC_o}\right) + \frac{R_C}{2L_sR_oC_o}} \tag{15}$$

where, $C(s)$ denotes the transfer function of the sliding mode controller. $C(s) = -(\alpha_1 + \frac{\alpha_2}{s})$. Therefore, Eq. (15) can be utilized for the loop design and comparative study with other compensators.

C. Dynamic Behavior

1) Error dynamics

Considering the surface and the error expression, the dynamic can be obtained as follows,

$$e(t) = E_o e^{-\frac{\alpha_2}{\alpha_1}t} \tag{16}$$

where, E_o denotes the initial steady state error for the output voltage. Note that the error dynamic would converge to zero fundamentally at the steady state, regardless of its initial value. In addition, the settling time can be tuned based on the selection of the sliding surface coefficients. For example, to achieve 4% settling of the output voltage, the selection of the sliding surface coefficients α_1 and α_2 should be subjected to the condition below, assuming C_o is fully discharged for the initial state,

$$E_o e^{-\frac{\alpha_2}{\alpha_1}t} < 0.04V_o^*, \quad \frac{\alpha_2}{\alpha_1} > \frac{\ln(25)}{t_s} \tag{17}$$

where, t_s represents the desired settling time of the system.

It is worthwhile to note that the stability constraints for the sliding surface must hold while selecting the sliding surface coefficients. Furthermore, the asymptotic stability of the error dynamic needs to be ensured such that the error dynamics converge to zero, which describes the tracking performance of the state variable V_o. In this regard, the stability of Lyapunov function $\tilde{V}(e)$ based on the energy function can be examined as,

$$\dot{\tilde{V}}(t) = -\frac{\alpha_2}{\alpha_1} C_o {E_o}^2 e^{-\frac{2\alpha_2}{\alpha_1}t} < 0 \tag{18}$$

From Eq. (18), the derivative of the Lyapunov function is monotonically negative definite regardless of the coefficients since $\dot{\tilde{V}}(t_s) < 0$ holds with the defined settling time t_s. Therefore, the asymptotic stability of error dynamic is confirmed.

2) Trajectory Condition

Taken the boundary of the sliding mode surface into consideration, the transverse variation of the sliding surface from its nominal condition is proportional to the overshoot of output voltage under load transient. Therefore, the trajectory of confining the value of 'S' within the boundaries, i.e. $S + \Delta S$ and $S - \Delta S$, respectively, is shown in Fig. 4, where the overshoot can be controlled.

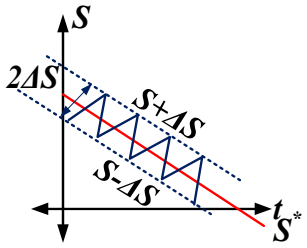


Fig. 4. The variation of sliding surface with respect to time.

The variation of $2\Delta S$ happens during ON and OFF intervals, where ON intervals imply the rising slope ($\dot{S} > 0$) and OFF intervals imply the decreasing slope ($\dot{S} < 0$). Note that the ON and OFF periods are determined by the phase difference adjustment between the primary and secondary gate signals. $|\dot{S}|$ can be expressed in terms of traversal period,

$$|\dot{S}| = \left|\frac{dS}{dt}\right| = \left|-\alpha_1 \frac{dV_o}{dt} + \alpha_2 (V_o^* - V_o)\right| < \frac{2\Delta S}{\frac{1}{2f}} = 4\Delta S f \tag{19}$$

If ΔS is kept infinitesimally small as time interval goes to zero, the weighted sum of V_o and $\frac{dV_o}{dt}$ from their individual references needs to obey the following inequality, which is described in Fig. 4.

$$|\alpha_1 \Delta V_o + \frac{2\alpha_2 V_o}{f}| < \frac{\alpha_2 V_o^*}{2f} \tag{20}$$

In order to establish the boundary limit for ΔV_o, it is required to replace V_o with ΔV_o, which can be computed by utilizing the state-space equation. Recalling from Eq. (8), the following relationship is yielded,

$$\Delta V_o = \frac{I_L}{fC_o} - \frac{V_o}{fC_o R_o} + \frac{D(1-D)V_{in}}{4f^2 C_o L_s} \tag{21}$$

Since Eq. (21) implies an upper bound for an averaged ΔV_o over one switching period, it could be transformed into inequality and expressed in Eq. (22), which confines the state variables within a certain band of variation under load disturbances.

$$|\Delta V_o| < \frac{\frac{\alpha_2 V_o^*}{2} - 2\alpha_2 R_o \left[I_L + \frac{D(1-D)V_{in}}{4fL_s}\right]}{f(\alpha_1 - 2\alpha_2 C_o R_o)} \tag{22}$$

By means of proper selection of the sliding mode coefficients without violating other stability constraints, the variation ΔV_o can be minimized.

D. Soft Switching Constraints

Soft switching of primary and secondary side MOSFETs can be achieved with proper value of phase difference time. Note that the inductor current needs to be large enough to fully charge or discharge the MOSFET junction capacitor during the phase difference time,

$$\frac{1}{2} 2L_s \Delta I_L^2 > C_j \cdot \max(V_{in}, V_o)^2 \tag{23}$$

where, C_j is the MOSFET junction capacitance. From the Fig. 2 (a), the following equations are obtained,

$$\begin{cases} I_L(0) = -\left[I_L(DT) + \frac{V_{in}-V_o}{2L_s}\frac{T(1-D)}{2}\right] \\ I_L(DT) = I_L(0) + \frac{V_{in}+V_o}{2L_s}\frac{DT}{2} \end{cases} \tag{24}$$

Therefore, ΔI_L can be derived as,

$$\Delta I_L = I_L(DT) - I_L(0) = \frac{DT(V_{in}+V_o)}{2L_s} \tag{25}$$

Based on Eq. (23) and Eq. (25), soft switching constraints are obtained and the effective range of D is determined.

E. Comparison with PI Compensator

PI controllers can be implemented for the voltage regulation of DAB converter. Although a higher phase margin might improve the dynamic performance, it effectively increases the closed loop bandwidth, which in turn amplifies the high frequency components arising from switching and parasitic resonance in the circuit.

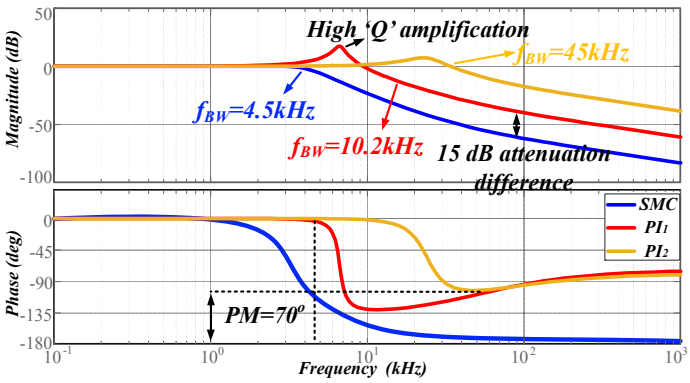


Fig. 5. Bode plot of system response with SMC and two different PI compensator combinations using parameters in Table I.

TABLE I. CIRCUIT PARAMETERS AND SPECIFICATIONS

Items	Specifications
V_{in} / V_o^*	$400V$ / $395V$
f	$50kHz$
L_s	$9.8\mu H$
C_o	$1.8mF$
R_o / R_c	31.2Ω / 0.1Ω

As shown in Fig. 5, the phase margin (70^o) between SMC and PI_2 compensator is set to be the nearly same, which inherently implies different bandwidths. It is observed that high frequency components receive higher attenuation in case of SMC than PI compensation with the same phase margin. On the other hand, maintaining a similar high frequency attenuation, phase margin of SMC will be higher as the phase response is much flatter for SMC in comparison to PI compensators. Therefore, SMC gives better performance than PI either in terms of high frequency attenuation level or phase margin.

III. EXPERIMENTAL RESULTS

As the verification for the proposed control methodology, the prototype of a DAB converter is designed and built, as shown in Fig. 6, where the control algorithm is implemented in a digital signal processor (TMS320F28335) [21]. It is worth mentioning that the newly released IXYS SiC MOSFET IXFN70N120SK with SOT-227-4 package is utilized here to minimize the dead-time effect and maximum power transfer capability [22]. The integrated voltage and current sensors along with the isolated gate drivers are equipped in the daughter board, attaching close to the power board to reduce the parasitics and EMI noise. It is worth mentioning that this design is of modularity and flexibility and brings the convenience if one module fails down. Each full bridge is rated at 2.5 kW with an isolated planar transformer operating at 50 kHz. Due to the page limitation, only a set of experimental results regarding the start-up transient and steady state operation are disclosed.

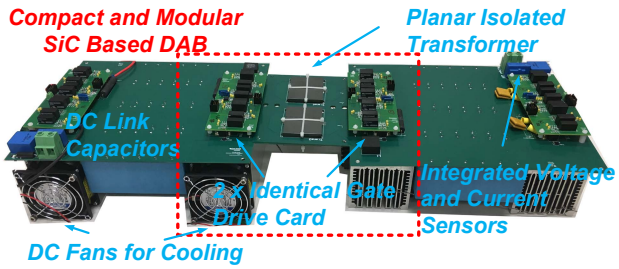


Fig. 6. The showcase of the compact and modular SiC based DAB converter built in authors' lab.

It is observed in Fig. 7 that (i) fast settling time is achieved with 100ms; (ii) output voltage ripple is eliminated, which demonstrates ample phase margin and implies good system stability.

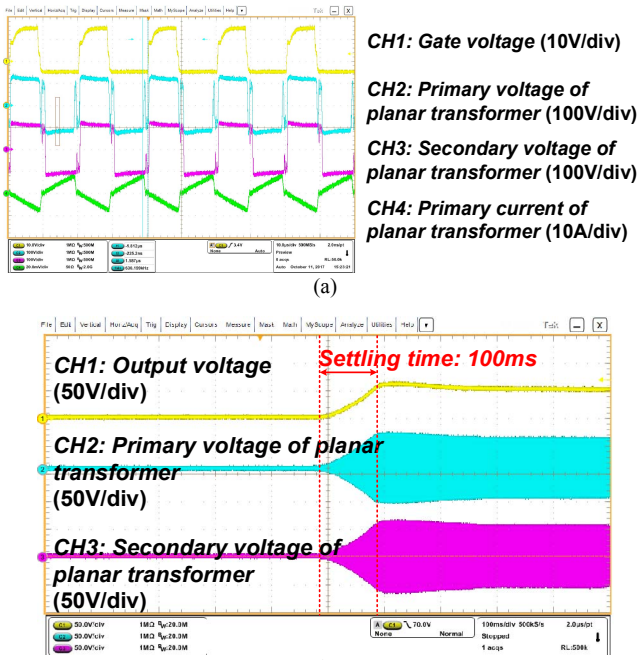


Fig. 7. Experimental results: (a) steady state waveforms with 0.2 phase-shifted ratio at 600 W; (b) experimental start-up waveforms of output voltage V_o with settling time 100 ms.

IV. CONCLUSIONS AND FUTURE WORK

In this work, a detailed output voltage control loop design procedure for a dual active bridge (DAB) DC-DC converter is proposed using sliding mode control (SMC) technique. The sliding mode coefficients are investigated to guarantee both small signal and large signal stability for the robustness consideration. In addition, dynamic performance of the system is examined considering the steady state error and overshoot. The proposed control method is capable of achieving soft-switching operation by determining the effective duty phase displacement range. As the verification of proof-of-concept, a hardware prototype of a DAB converter is built and evaluated, and the effectiveness of the loop design is validated by the start-up transient tests. It is observed that overshoot is eliminated in the start-up test and the fast settling time is achieved.

For the future work, the prototype will be tested up to full power. To validate the improved dynamics of the proposed control over PI compensator, load transients with respect to SMC and PI compensator will both be conducted.

V. ACKNOWLEDGEMENT

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