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Using MRED to Screen Multiple Node Charge Collection Mitigated SOI Layouts

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Abstract

Multiple node charge collection robust SOI latch designs and layouts are simulated and tested. MRED is used to identify potential single-event susceptibilities associated with different layouts prior to fabrication and to bound potential single-event testing responses.

Background – Single Node Charge Collection Mitigated Designs

- Dual Interlocked Cell (DICE)

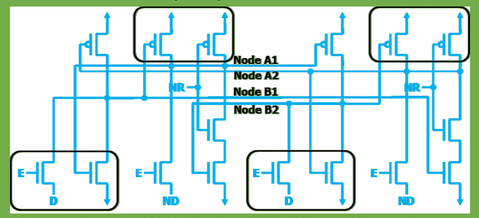

Fig. 1. Circuit schematic of DICE latch with black boxes showing transistors that should be maximally separated in the circuit layout. No boxed transistors should also be maximally separated.

- Transient Immune Composite Logic (TICT) or Stacked

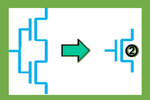

Fig. 2. TICT or double stacked transistor circuit (left side) with simplified schematic representation (right side). Storage transistors in latches are replaced with TICT for SEU mitigation and all transistors are replaces with TICT for SEU/SET mitigation.

- Triple Modular Redundancy (TMR) – Triplicate sequential circuits and vote out errors

All above are susceptible to co-incident charge collection events in two circuit nodes.

Multiple Node Charge Collection Mitigated Designs/Layouts

- Triple Stacked Transistor Latch

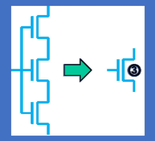

Fig. 3. Triple stacked transistor (left side) circuit with simplified schematic representation (right side).

- Triple stacked transistor islands should not be colinear in layout. Right triangle layout in Fig. 4.
- Requires sufficient charge collection in all 3 transistors in a stack to potentially cause upset.

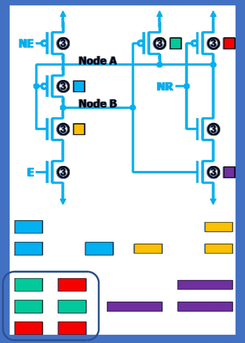

Fig. 4. Triple stacked transistor latch showing layout of susceptible circuit nodes.

- Stacked DICE Latch

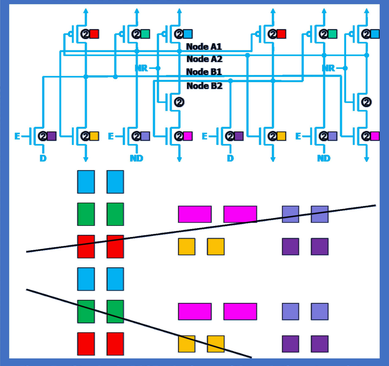

Fig. 5. Stacked DICE design with relative transistor placement.

- Vertical DICE Redundancy
- Horizontal Stacking Redundancy
- Requires sufficient charge collection in 4 specific transistors to potentially cause upset

MRED Simulation

TABLE I. MRED Simulation Results for Normally Incident Ions, Minimum 0.0001 fC.

Latch Type	45 MeV He		178 MeV Ni		531 MeV Ar		785 MeV Cu		1032 MeV Kr	
	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count
Standard	159	N/A	174,013	N/A	174,111	N/A	175,505	N/A	175,437	N/A
DICE	403	7	444,209	22	446,906	29	445,760	23	446,328	18
Triple Stacked	1,233	0	1,352,175	0	1,259,216	0	1,355,856	0	1,358,271	0
Stacked DICE	737	0	888,719	0	891,480	0	891,156	1	891,545	0

TABLE II. MRED Simulation Results for Isotopically Incident Ions, Minimum 0.0001 fC.

Latch Type	45 MeV He		178 MeV Ni		531 MeV Ar		785 MeV Cu		1032 MeV Kr	
	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count
Standard	283	N/A	111,815	N/A	151.282	N/A	157,445	N/A	158,036	N/A
DICE	747	7	284,410	814	389,401	868	403,165	946	405,494	874
Triple Stacked	1,698	0	798,883	0	990,497	0	1,013,661	4	1,019,973	0
Stacked DICE	1,378	2	553,376	114	752,736	154	778,702	166	783,126	160

MRED Simulation Parameters

- 100 Million Monte Carlo samples per data point.
- Multiple Node Event Count is 2 for DICE, 3 for Triple Stacked, and 4 for Stacked DICE and in specific node combinations.

- DICE
  - Simple circuit simulation of multiple node events reduces all but 1 event with Cu and 2 events with Kr at normal incidence, but MRED shows potential SEUs. Example MRED graphical result shown in Fig. 6.
  - Most multiple node events remained with isotropic incidence, which shows limit of DICE reliability.

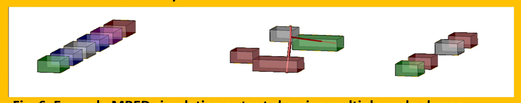

Fig. 6. Example MRED simulation output showing multiple node charge collection in DICE latch, 2 PMOSFETs.

- Triple Stacked
  - Review of 4 isotropic Cu events show at least one transistors receives less than 1 fC, which was limit for DICE upsets
  - Multiple node events observed in lower left sets of transistors
- Stacked DICE
  - Layout shown to be vulnerable in isotropic case. Fig. 5 shows a couple paths that traverse through 4 transistors.
  - MRED shows need for improved layout.

SEU Test Results

- Test Structures
  - Two 2k shift registers with common inputs and clocks and error flagging between outputs, for each latch type.
  - Error circuitry design with triple stacked latches for all cases.
- Test Campaign
  - Input is static (all 0s) with slow clocking. Error flag counts measured in oscilloscope.
  - Testing at Texas A&M Cyclotron with 15 MeV/U beam and ions listed in Tables I & II at normal incidence.
- Results
  - Standard latch was the only one to upset, results shown in Fig. 7.
  - MRED simulation results coupled with simple circuit simulation produces upper bounds for standard and DICE latches, also shown in Fig. 7.
  - MRED shows that >1x10^{11} particles/cm^2 fluence would be needed to see statistically significant DICE upsets.

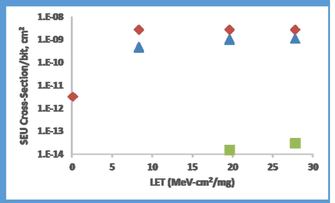

Fig. 7. SEU test results for the standard latch (blue triangles). Also shown are normal incident cross-sections from MRED simulation for the standard latch (red diamonds) and DICE latch (green squares).

Conclusions

- Two new robust latches introduced showing mitigation of co-incident charge collection at 2 circuit nodes.
- MRED capability to assess circuit designs/layouts to predict SEU test results or to determine if layouts actually accomplish design goals.

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