MW-Class Cryogenically-Cooled Inverter for Electric-Aircraft Applications

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High power inverters will be a key enabler for future aircraft based on hybrid electric or turbo-electric propulsion as envisioned by NASA and Boeing. Cooling a power electronics converter to low temperature, e.g. using cryogenic cooling, can significantly improve the efficiency and power density of a power conversion system. This paper presents the design of a MW cryogenically-cooled power inverter for electric aircraft applications. The power semiconductor and magnetic component characterization, inverter topology and power stage design, modulation and control, EMI noise reduction and filters design, and cooling system design are illustrated. A MW-level inverter prototype has been assembled and tested. The experimental results verify the functionality of the inverter.

I. Introduction

High power inverters will be a key enabler for future aircraft based on hybrid electric or turbo-electric propulsion as envisioned by NASA and Boeing. A technological hurdle exists however, in that the components for power generation, distribution, and transformation are not currently available in the high-power ranges with the necessary efficiency and power density required for transport-class aircraft [1].

Power generation and distribution using superconducting systems with extremely low power loss offer intriguing propulsion-system benefits. However, many of the necessary power electronics to control and protect a cryogenic system are not yet available. There are not many reports about power converter designs at cryogenic temperatures. According to recent literature [2-9], the maximum reported power level of a cryogenically cooled converter prototype was 2.5 kW. Moreover, there is no specific detailed cooling system design provided that would be suitable for high power electronics applications.

This paper presents the design of a MW-class cryogenically cooled inverter for aircraft application. The inverter is DC-fed from $\pm$ 500 V bus, and is capable of three-phase output up to a fundamental frequency of 3 kHz. Fig. 1 shows the inverter system architecture, which includes dc link, power stage, input/output filter, gate drive, protection, inverter control, and thermal interface with a cryogenic cooling system. The characterization of critical components at cryogenic temperatures, including power devices and magnetics, is introduced first as the basis for power converter design and optimization. Then, the detailed inverter system design including inverter topology, gate drive, busbar, modulation, control, EMI noise reduction and filter design, and cryogenic cooling system are presented. A 1 MW prototype has been assembled and the functionality of the inverter has been experimentally verified.

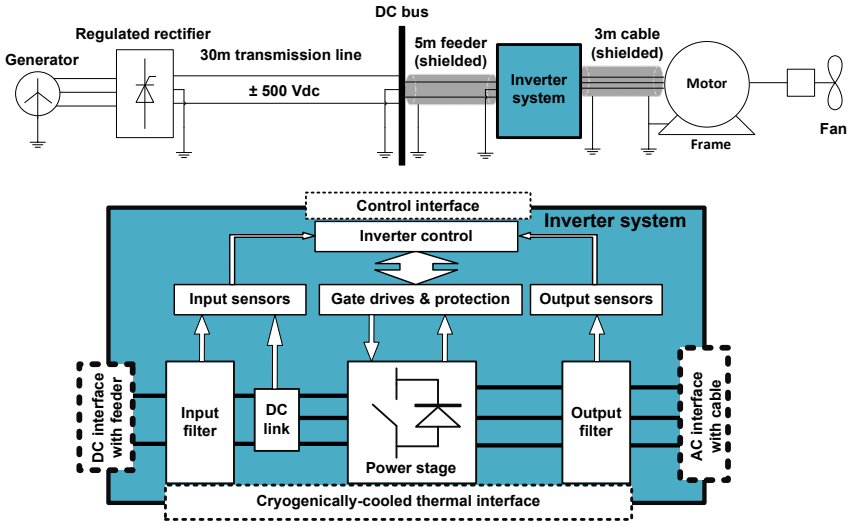

Fig. 1. Inverter system architecture.

II. MW-Class Cryogenically Cooled Inverter System Design

A. Characterization of Components at Cryogenic Temperatures

Power device characterization at cryogenic temperatures was presented in [12]-[14]. Fig. 2 shows the behavior of specific on-resistances and breakdown voltages of some sample devices. It is observed that at room temperature, SiC MOSFET has the lowest specific on-resistance. As temperature decreases to cryogenic region, GaN HEMT shows the lowest specific on-resistance. However, the dynamic on-resistance of GaN HEMT may be an issue at low temperatures [19]. SiC MOSFET and GaN HEMT both show stable breakdown voltages throughout the whole temperature range, while the breakdown voltage of Si MOSFET trends down with the temperature drop. As a result of performance evaluation and design requirement, the SiC MOSFET was selected due primarily to the availability of high-current power modules and the stable breakdown voltage. However, the SiC die temperature should be controlled in a certain range to avoid high conduction loss.

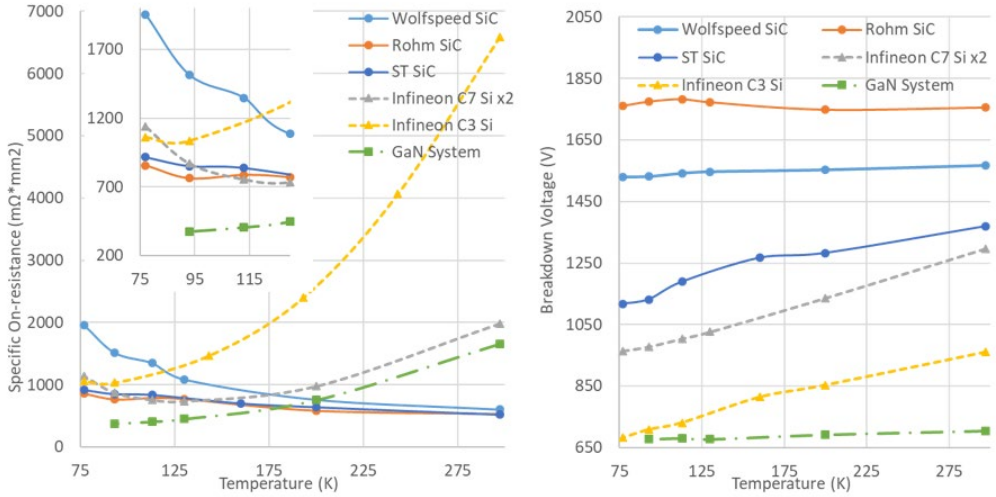

Fig. 2. Static performance of Si, SiC and GaN MOSFETs and their comparison.

Characterization of magnetics at cryogenic temperatures was presented in [11]. The widely used magnetic material for EMI inductor –nanocrystalline, is characterized at low temperatures and summarized as shown in Fig. 3. Compared to the room temperature values, the core loss increases to about 1.5-2.5 times, the permeability decreases to 60% and flux density increases 8% at cryogenic temperatures. Although the nanocrystalline core performance degrades at cryogenic temperatures, low temperature cooling can still benefit the inductor design due to the significant reduction

of inductor winding loss. In addition, the low-temperature environment allows a higher range of temperature rise for inductor design, therefore a less degree of thermal limitation for core selection.

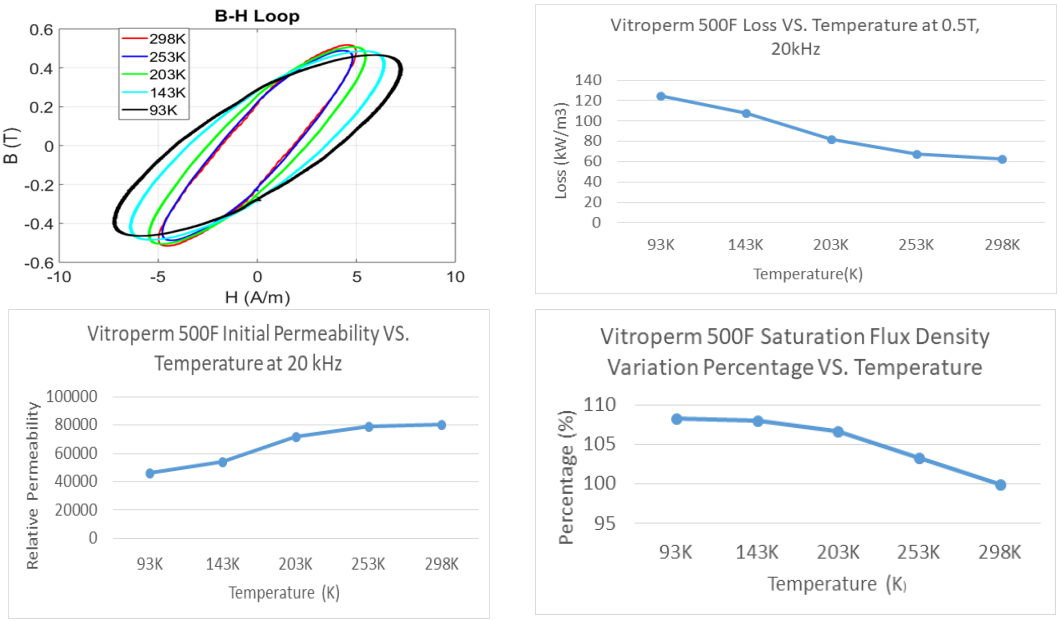

Fig. 3. Nanocrystalline magnetic core characteristics at low temperature.

B. Power Module and Inverter Topology Selection

Power modules with high current capability are preferred to achieve MW power delivery. Table I lists the parameters of the selected SiC MOSFET module. Based on the static and double pulse test, it can match the requirement of the loss budget. The active neutral-point-clamped (ANPC) converter shown in Fig. 4 is a promising and popular candidate for high-power medium-voltage (kilo-volts level) applications. All the switches in the converter can be actively controlled to achieve bidirectional power flow, better thermal balance and higher efficiency [15]. Therefore, it was adopted as the topology. Two inverters are paralleled and interleaved to achieve 1 MW power while reducing harmonic ripples.

Table I. Specs of power module

Manufacturer	Wolfspeed
Die Technology	3nd GEN
Voltage Rating	900 V
Current Rating	800 A
Weight	179 g

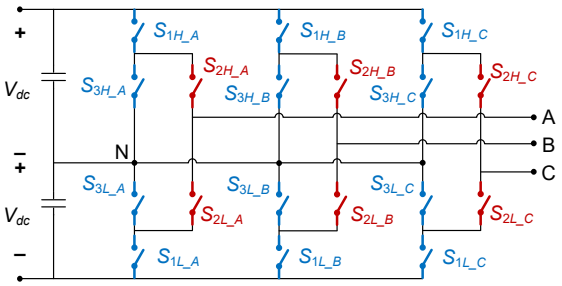

Fig. 4. Topology of 3L-ANPC converter.

C. Power Stage Design

The electric design of the power stage includes the coordinated design of converter layout, busbar, gate drive and auxiliary circuits. A laminated busbar structure was designed to minimize the parasitic inductance in switching loops. Fig. 5 shows the busbar for one phase leg. A loop inductance of less than 20 nH was achieved. The gate drive board with de-saturation and over-temperature protection is shown in Fig. 6. The interface board with isolated power supplies and communication interface is shown in Fig. 7.

The power stage is cooled by cryogenic gaseous nitrogen to avoid freezing of the dielectric gel of the power modules. Tapered fins are used in the cold plate channel to provide a uniform temperature distribution of all of the dies on an individual module. From an inlet manifold, the gas flows in 18 parallel channels, where each channel has a pressure adjustment valve at the channel exit to regulate the flow and maintain uniform temperatures among all of the modules.

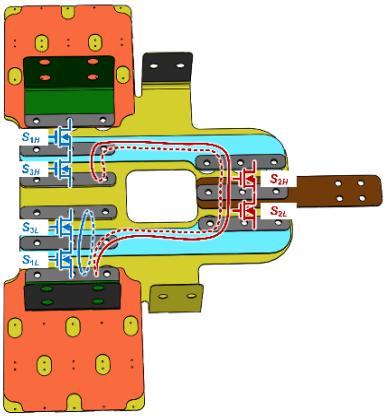

Fig. 5. Designed busbar.

Fig. 6. Designed gate drive.

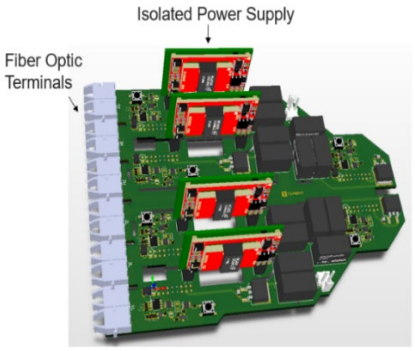

Fig. 7. Designed interface board.

D. Modulation and Control

For a three-level inverter, there exist redundant switching states. Multi-control objectives such as balancing neutral point voltage, reducing switching loss and CMV can be achieved by selecting the redundant space vectors [16]. Popular space vector modulation (SVM) schemes such as nearest three space vector (NTSV) [22], common-mode reduction (CMR) [23] and common-mode elimination (CME) [24] have been developed. For three-level ANPC topology, over-voltage issue on non-active devices induced by multi-commutation loops and nonlinear output capacitance of the power semiconductors have been discussed in [15, 17].

Paralleling and interleaving inverters provides increased power level and reduced output harmonics. However, circulating current exists when the paralleled inverters have common dc and ac sides. The circulating current distorts the current, increases loss and degrades the inverter system performance. To suppress high-frequency circulating current, coupled inductors are inserted into the circulating loop. The low-frequency circulating current can be suppressed by implementing a closed-loop controller to actively adjust the dwell time of the redundant small vectors in three-level modulation.

TI TMS320C6748 and Xilinx FPGA Spartan 6 were selected as central controllers for the design of control system. The communication between DSP and FPGA is based on Universal Parallel Port protocol. The synchronization among switching signals is crucial to control paralleled inverters. Especially, the synchronization also enables precise interleaving angle control between paralleled inverters. The software architecture of DSP and FPGA, as well as the hardware configuration, is illustrated in [18].

E. EMI Noise and EMI Filter

In aircraft applications, both the inverter dc input side and ac output side need to meet DO-160 standards [10], and thus EMI filters are needed for both sides. EMI filters are usually a main weight contributor for motor drive in aircraft applications.

EMI filter corner frequency is an indicator of EMI filter weight, and a higher EMI filter corner frequency usually indicates a lighter EMI filter. When the switching frequency is below 150 kHz, it has a non-monotonous relationship with EMI filter corner frequency as shown in Fig. 8. Some optimal switching frequency (such as 70 kHz, 140 kHz) exists, and can be selected to optimize the EMI filter.

For a paralleled inverter system, interleaving can be utilized to reduce the harmonics. In [20]-[21], analytical models for harmonic calculation of the three-level NPC inverter with space vector modulation are developed. Then, the optimal interleaving angle ranges to reduce the dc side, ac side and EMI harmonics consider multiple impact factors are derived. Fig. 9 and Fig. 10 show the calculation results of the CM and DM filter corner frequency as a function of modulation index and interleaving angle, assuming a 70 kHz switching frequency. It can be observed that, the CM filter corner frequency peak is achieved when interleaving angle is around 180°, and the second optimal interleaving angle range is 30°~90°. The DM filter corner frequency peak is obtained when interleaving angle is around 30°~60°, and the second optimal interleaving angle range is around 120°~180°.

Nanocrystalline material is selected for both the coupled inductors and CM chokes in the system due to its superior performance to achieve high power density. The leakage inductance of the coupled inductor and CM choke is utilized to suppress the DM noise. Cryogenic cooling benefits the inductor due to a significant reduction in copper resistivity, allowing a decrease in weight and an increase in efficiency. A unique feature of the filter inductors is the use of 3-D printed thermoplastic housing that accommodates liquid nitrogen cooling for the larger inductors and reduces the

housing weight. The losses of the core material are higher at colder temperatures, so the cooling of the inductor is tailored so that the windings are kept cold, while the core is at the highest possible temperature of the inductor.

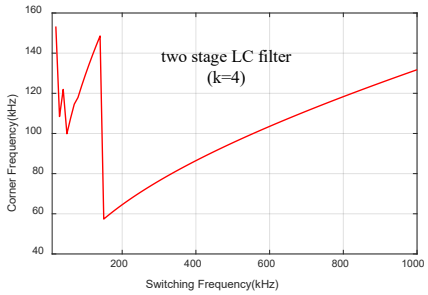

Fig. 8. EMI filter corner frequency versus switching frequency.

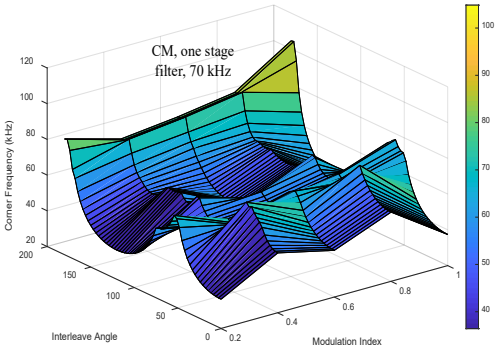

Fig. 9. CM Filter corner frequency versus interleaving angle at different modulation indexes.

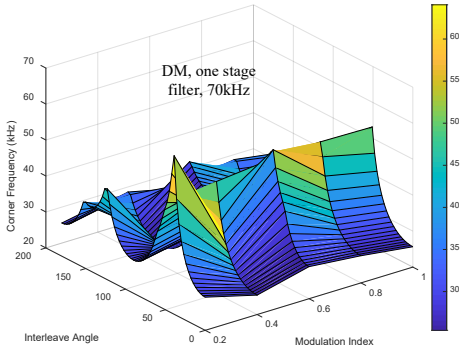

Fig. 10. DM Filter corner frequency versus interleaving angle at different modulation indexes.

F. System Integration

With the design of all the subsystems, Fig. 11 shows the inverter system integration including the power stages, EMI filters, controllers and sensors, gas nitrogen and liquid nitrogen cooling system.

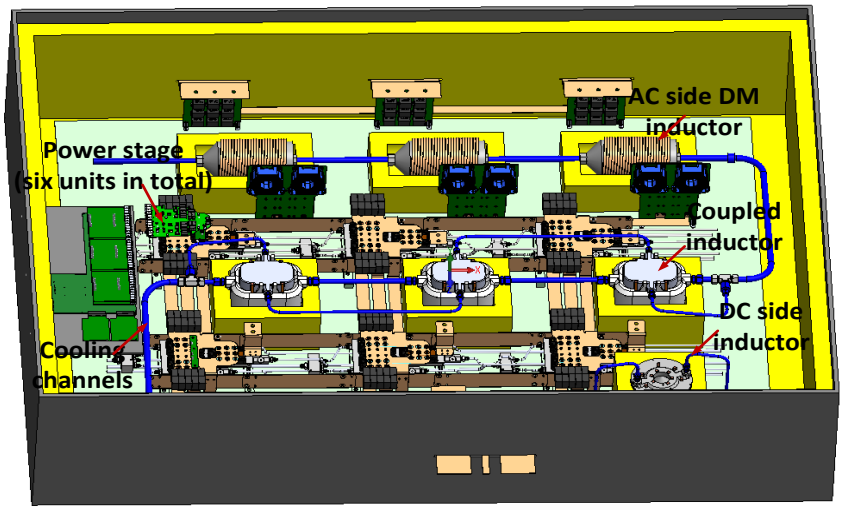

Fig. 11. Inverter system integration.

III. Prototype and Experimental Results

Fig. 12 shows the setup of testing the cooling performance of the cold plate. Three groups of resistor heaters as well as the attached thin aluminum plates are mounted on top of the cold plate. Power loss based on the estimated

converter loss are generated from the heaters to mimic the operation of the converter. Fig. 13 plots the measured temperature with the loss corresponding to inverter full load condition. The maximum heater case temperature is slightly higher than 60 °C, which indicates that the cooling performance is good enough for full load operation.

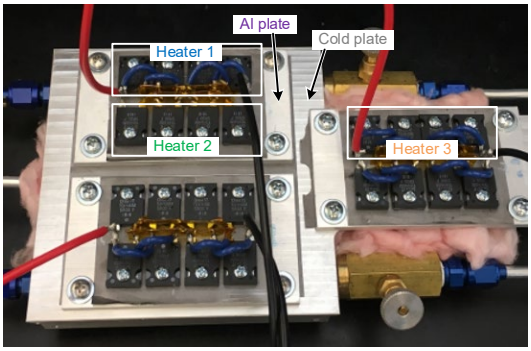

Fig. 12. Cold plate testing setup with resistor heaters.

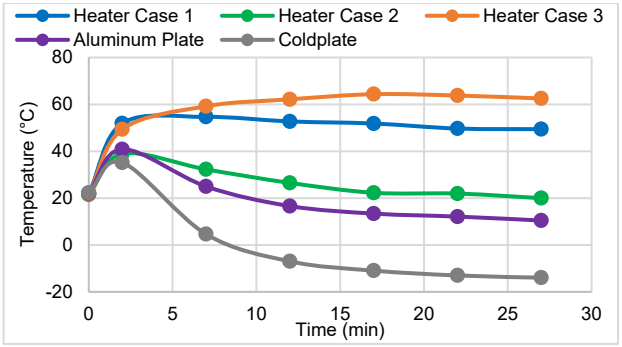

Fig. 13. Cold plate testing result under full load condition.

Fig. 14 shows the assembled coupled inductor with 3-D printed housing for the 1 MW inverter system. The housing is specially designed to accommodate liquid nitrogen cooling and the inductor heat dissipation requirement.

(a) (b)

Fig. 14. Coupled inductor with 3-D printed housing (one phase), (a) bottom of the housing with core set and winding, (b) top of the housing.

Fig. 15 shows one single-phase prototype of the converter and Fig.16 shows the testing platform of the inverter at room temperature. Fig. 14 and Fig. 15 show the pulse test waveforms at rated voltage and current level. The peak current in Fig. 17 is 650 A, which corresponds to peak current at full output power. In Fig. 18, the peak voltage across the SiC MOSFET is less than 600 V, which verifies the performance of the busbar and the proposed control. Fig. 19 shows the continuous power test waveforms at room temperature.

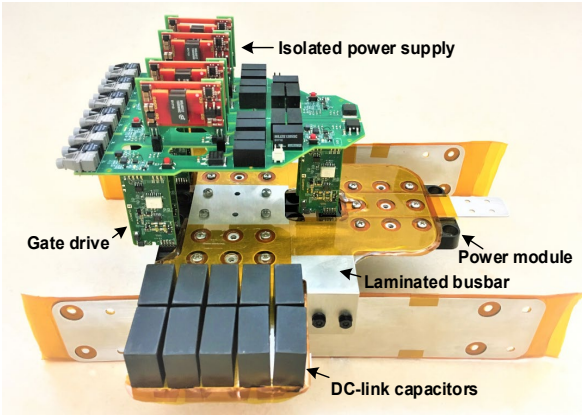

Fig. 15. Prototype of 3L-ANPC converter (single phase).

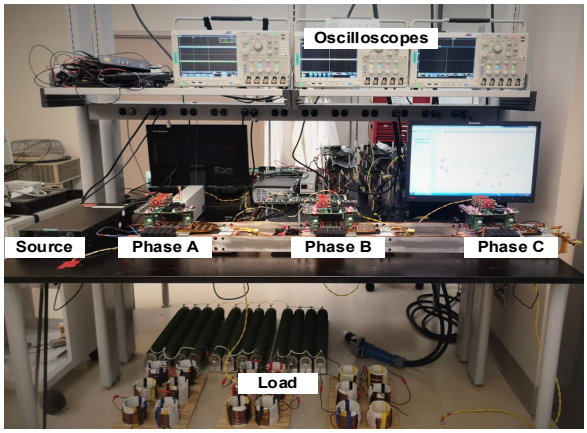

Fig. 16. Testing platform of 3L-ANPC converter.

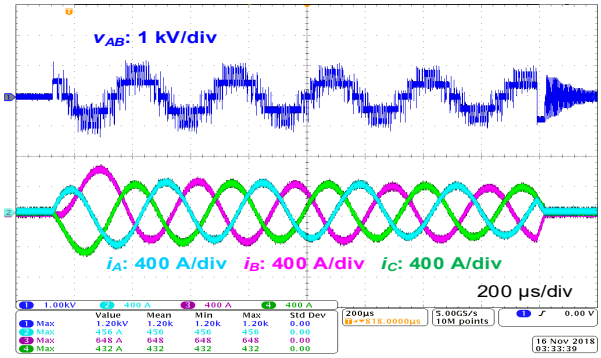

Fig. 17. Tested output voltage and current waveforms.

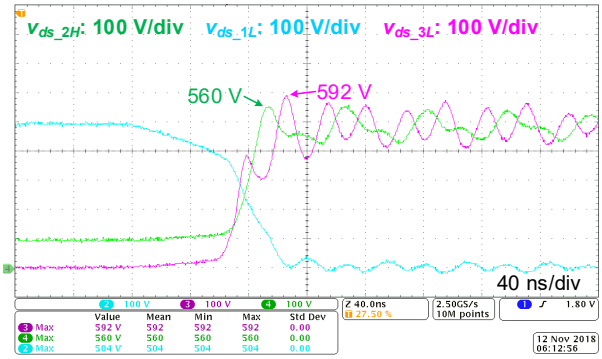

Fig. 18. Tested switching transient waveforms.

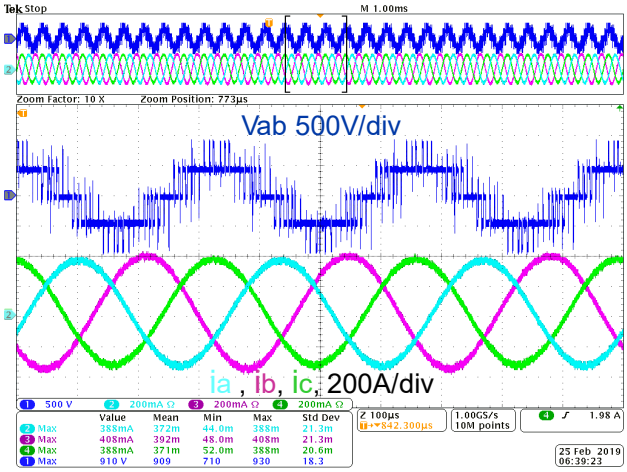

Fig. 19. Line voltage and phase output currents waveforms.

Fig. 20 shows the tested voltage and current waveforms of two paralleled inverters with 1 kV dc voltage input and a couple of amps current. Signals are well synchronized and current among the inverters well balanced. Fig. 21 shows the voltage waveforms for two interleaved inverters with 60° interleaving angle, and Fig. 22 shows the EMI noise current comparison. The 60° interleaving angle results in significantly reduced 3rd and 4th order harmonics when compared to a 0° interleaving angle.

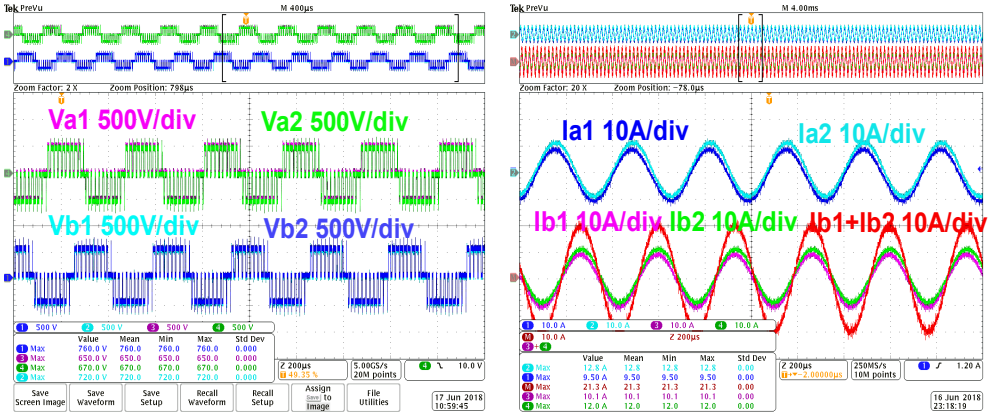

Fig. 20. Phase output voltage and currents of two paralleled inverters.

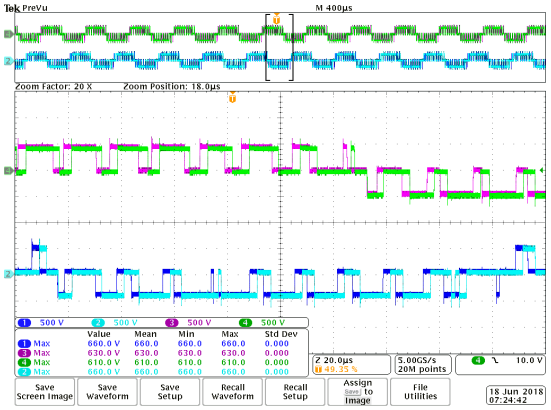

Fig. 21. Phase output voltage of two 60°interleaved inverters.

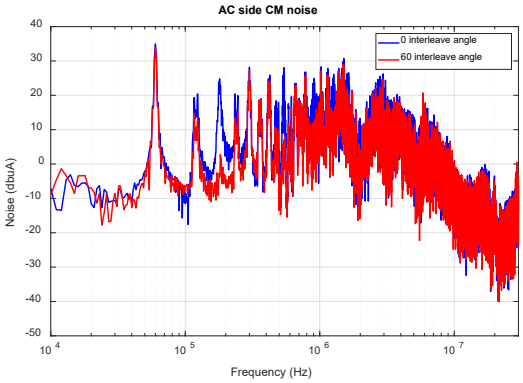

Fig. 22. EMI noise current comparison with 0° and 60° interleaving angle.

IV. Conclusion

This paper presents the design of a MW-level cryogenically cooled inverter for electric aircraft applications. Two 500 kW three-level ANPC inverters are paralleled to achieve 1 MW power delivery. The subsystems design to fit cryogenic cooling and achieve high power density are illustrated. Experiment results are demonstrated and verify the functionality of the inverter. For future work, the 1 MW inverter system will be tested at full load condition with cryogenic cooling.

Acknowledgment

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References

[1] Amendment no. 3 to the NASA Research Announcement (NRA), "Research opportunities in aeronautics – 2015 (ROA-2015)," NNH14ZEA001N, 2015.

[2] A. Forsyth, C. Jia, D. Wu, C. Tan, S. Dimler, Y. Yang, and W. Bailey, "Cryogenic converter for superconducting coil control," *IET Power Electron.*, vol. 5, no. 6, pp. 739-746, 2012.

[3] J. Garrett, R. Schupbach, H. A. Mantooth, and A. B. Lostetter, "Development of an Extreme Environment DC Motor Drive Full Bridge Power Stage Using Commercial-Off-The-Shelf Components," in *Proc. Int. Pleanet. Probe Workshop*, 2006.

[4] J. Bourne, R. Schupbach, B. Hollosi, J. Di, A. Lostetter, and H. A. Mantooth, "Ultra-Wide Temperature (-230° C to 130° C) DC-Motor Drive with SiGe Asynchronous Controller," in *Proc. IEEE Aerosp. Conf.*, 2008, pp. 1-15.

[5] C. Barth, J. Colmenares, T. Foulkes, K. Coulson, J. Sotelo, T. Modeer, N. Miljkovic, and R. C. Pilawa-Podgurski, "Experimental evaluation of a 1 kW, single-phase, 3-level gallium nitride inverter in extreme cold environment," in *Proc. IEEE Appl. Power Electron. Conf.*, 2017, pp. 717-723.

[6] O. Mueller and K. Herd, "Ultra-high efficiency power conversion using cryogenic MOSFETs and HT-superconductors," in *Proc. IEEE Power Electron. Special. Conf.*, 1993, pp. 772-778.

[7] C. Gold and O. M. Mueller, "Cryogenically-cooled switching circuit," U. S. Patent US6172550B1, Jan. 9, 2001.

[8] B. Ray, S. S. Gerber, R. L. Patterson, and I. T. Myers, "Liquid nitrogen temperature operation of a switching power converter," NASA-TM-106867, 1995.

[9] B. Ray, S. S. Gerber, R. L. Patterson, and I. T. Myers, "77 K operation of a multi-resonant power converter," in *Proc. IEEE Power Electron. Special. Conf.*, 1995, vol. 1, pp. 55-60.

[10] RTCA DO-160G, Environmental Conditions and Test Procedures for Airborne Equipment, December 8, 2010.

[11] R. Chen, Z. Dong, Z. Zhang, H. Gui, J. Niu, R. Ren, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Core characterization and inductor design investigation at low temperature," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018.

[12] Z. Zhang, C. Timms, J. Tang, R. Chen, J. Sangid, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Characterization of high-voltage high-speed switching power semiconductors for high frequency cryogenically-cooled application," in *Proc. IEEE Appl. Power Electron. Conf.*, 2017, pp. 1964-1969.

[13] H. Gui, R. Ren, Z. Zhang, R. Chen, J. Niu, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Characterization of 1.2 kV SiC power MOSFETs at cryogenic temperatures," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 7010-7015.

[14] R. Ren, H. Gui, Z. Zhang, R. Chen, J. Niu, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Characterization of 650 V enhancement GaN HEMT at cryogenic temperatures," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 891-897.

[15] H. Gui, Z. Zhang, R. Chen, R. Ren, J. Niu, B. Liu, H. Li, Z. Dong, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "A simple control to reduce device over-voltage caused by non-active switch loop in three-level ANPC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2019.

[16] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization of a high power high frequency three-level active neutral point clamped phase leg," IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3255-3266, 2014.

[17] R. Ren, Z. Zhang, B. Liu, R. Chen, H. Gui, J. Niu, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Multi-commutation loop induced over-voltage issue on non-active switches in fast switching speed three-level active neutral point clamped phase leg," in Proc. IEEE Energy Convers. Congr. Expo., 2018.

[18] J. Niu, R. Chen, Z. Zhang, H. Gui, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Design of a Single Controller for Multiple Paralleled Converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2019.

[19] R. Cuerdo, Y. Pei, Z. Chen, S. Keller, S. DenBaars, F. Calle *et al.*, "The kink effect at cryogenic temperatures in deep submicron AlGaN/GaN HEMTs," *IEEE Electron Device Lett.,* vol. 30, no. 3, pp. 209-212, 2009.

[20] R. Chen, J. Niu, H. Gui, Z. Zhang, F. Wang, Leon M. Tolbert, B. J. Blalock, D. J. Costinett and B. B. Choi, "Analytical analysis of AC and DC side harmonics of three-level active neutral point clamped inverter with space vector modulation," *IEEE Applied Power Electronics Conference and Exposition (APEC*), 2019.

[21] R. Chen, J. Niu, H. Gui, Z. Zhang, F. Wang, Leon M. Tolbert, B. J. Blalock, D. J. Costinett and B. B. Choi, "Coupled inductor design for interleaved three-level active neutral point clamped inverters considering EMI noise reduction," *IEEE Applied Power Electronics Conference and Exposition (APEC*), 2019.

[22] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp 637-641, Mar. /Apr. 2001.

[23] K. Hee-Jung, L. Hyeoun-Dong, and S. Seung-ki, "A new PWM strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed ac motor drives," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1840-1845, Nov./Dec. 2001.

[24] H. Zhang, A. Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645-1653, Nov./Dec. 2000.