SAND2018-7242C

Using MRED to Screen Multiple Node Charge Collection Mitigated SOI Layouts

Jeffrey D. Black, *Senior Member, IEEE*, Jeff A. Dame, Dolores A. Black, *Senior Member, IEEE*, Paul E. Dodd, *Fellow, IEEE*, Marty R. Shaneyfelt, *Fellow, IEEE*, John Teifel, Joseph G. Salas, Robert Steinbach, Matthew Davis, Robert A. Reed, *Fellow, IEEE*, Robert A. Weller, *Senior Member, IEEE*, James M. Trippe, *Member, IEEE*, Kevin M. Warren, *Senior Member, IEEE*, Andrew M. Tonigan, *Student Member, IEEE*, Ronald D. Schrimpf, *Fellow, IEEE*, and Richard S. Marquez

***Abstract*— Multiple node charge collection robust SOI latch designs and layouts are simulated and tested. MRED is used to identify potential single-event susceptibilities associated with different layouts prior to fabrication and to bound potential single-event testing responses.**

***Index Terms*—Single-Event Upset, Multiple Node Charge Collection, Sequential Circuits, Radiation Hardening by Design**

I. Introduction

MICROELECTRONICS technology nodes have scaled over the years, as has the critical charge needed to upset a memory cell produced in that technology [1]. Previous techniques used to increase the critical charge, such as adding parasitic resistance and/or capacitance, or increasing transistor drive, do not scale well [2]. Circuit designs and layout techniques can reduce the probability of the upset occurring by requiring charge collection at two or more nodes, e.g. Dual Interlocked Cell (DICE) [3], Transient Immune Composite Transistor (TICT) [4-5], and Triple Modular Redundancy (TMR) [6]. However, all of these designs have susceptibility to one or more single ion paths that can traverse multiple sensitive nodes in an isotropic environment [7]. In some cases, however, one wants to have a more robust storage cell that could be used for single event effect (SEE) built-in-self-test (BIST) [8] or used in a watchdog circuit element protecting softer circuit designs. This paper addresses how to design/layout those type of designs and how to verify the layouts prior to fabrication.

In this paper, we introduce two layouts that can be incorporated in Silicon-on-Insulator (SOI) technologies that require charge collection at a minimum of three locations. Monte Carlo Radiative Energy Deposition (MRED) simulations are used to screen the layouts to ensure there is minimal susceptibility to SEUs and heavy ion experimental data is used to validate the simulation results. Note, this paper is focused on static SEU mitigation, so it only discusses the memory storage circuits. However, this analysis can be extended to dynamic SEU mitigation.

II. Single Node Charge Collection Mitigated Designs

As microelectronics technology scaled, it was noted that the single event upset (SEU) threshold linear energy transfer (LET) was reducing, primarily due to reduced nodal capacitance and restoring current. Techniques to increase the SEU threshold LET include adding capacitance, increasing the restoring current by upsizing transistor drive, and/or adding a feedback resistor to slow down the circuit. These techniques run counter to microelectronics scaling which increases transistor density and speed. While the threshold LET is reducing, so is the circuit cross-section, so the net effect on soft error rate is not necessarily significantly changed. But, for higher reliability applications, the change in threshold LET does increase the potential for SEU.

To mitigate this reduction in SEU threshold LET, designers proposed circuits that needed to be affected at two circuit nodes for upset to occur. One of the first circuits to be implemented was DICE, a version of a DICE latch is shown in Fig. 1 [3]. A standard latch has two internal nodes, one for storing the held circuit state and one for the opposite state. The DICE latch has four internal nodes, two nodes for the held circuit state and two nodes for the opposite state. The basic layout concept is to place transistors where co-incident charge collection could cause a

Manuscript received July 13, 2018. This work was supported by Air Force Research Laboratory, Space Vehicles Directorate, contract FA9453-15-C-0450. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DENA0003525. (*Corresponding author: Jeffrey D. Black*).

J. D. Black and J. Teifel are with Sandia National Laboratories, Albuquerque, NM 87185-1072 USA (email: jefblac@sandia.gov).

J. A. Dame, R. Steinbach, and M. Davis are with Scientic, Inc., Huntsville, AL 35806 USA.

D. A. Black is with Sandia National Laboratories, Albuquerque, NM 87185-1159 USA.

P. E. Dodd, M. R. Shaneyfelt, and J. M. Trippe are with Sandia National Laboratories, Albuquerque, NM 87185-1083 USA.

J. G. Salas is with Sandia National Laboratories, Albuquerque, NM 87185-1168 USA.

R. A. Reed, R. A. Weller, K. M. Warren, A. M. Tonigan, and R. D. Schrimpf are with Vanderbilt University, Nashville, TN 37235 USA.

R. S. Marquez is with the Air Force Research Laboratory, Space Vehicles Directorate, Albuquerque, NM USA.

.

SEU. The four boxes in Fig. 1 show groups of transistors that should be maximally separated. It is similar for the groups of transistors not boxed. In SOI layouts, it is imperative that these set of transistors are also in separate Si islands.

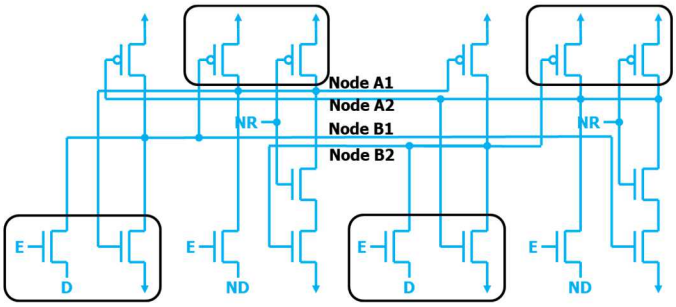

Fig. 1. Circuit schematic of DICE latch with black boxes showing transistors that should be maximally separated in the circuit layout.

A second approach to adding layout redundancy is called TICT [4-5] or transistor stacking, illustrated in Fig. 2. Fig. 2 shows a double transistor stack with the simplified schematic representation which will be used throughout this paper. Both transistors in the stack must collect a sufficient amount of the charge for a transient to be output from the composite drain. The key to the layout of the double transistor stack is that each transistor has its own silicon island when incorporated in an SOI technology and placed to minimize layout impact and SEU probability.

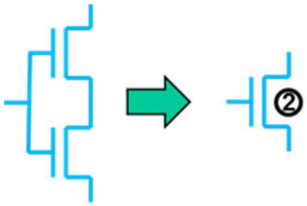

Fig. 2. Transient Immune Composite Transistor (TICT) or double stacked transistor circuit (left side) with simplified schematic representation (right side).

The third main approach to adding layout redundancy is TMR. This is the concept of triplicating the latch or flip-flop and voting at the output. The voter output can be fed back to the input to correct errors if one of the elements is upset. DICE and TICT generally double the transistor count in a design, while TMR triples the transistor count. But, the common theme in DICE, TICT, and TMR is that they are susceptible to co-incident charge collection in two circuit nodes, which has a probability in an isotropic radiative particle environment.

III. Multiple Node Charge Collection Mitigated Designs/Layouts

If DICE, TICT, nor TMR don't meet the reliability requirement, then there are some other options. First, the three designs can be increased in SEU hardness by adding capacitance, increasing restoring current, or adding feedback resistance. Second, SEU hardness can be increased at the integrated circuit (IC) level, e.g. error detection and correction. Third, the number of co-incident circuit node susceptibility can be increased beyond two. This paper introduces two radiation hardened by design (RHBD) circuits that do just that.

A. Triple Stacked Transistor Latch

A triple transistor stack (Fig. 3) incorporated in an SOI technology is more robust than the double transistor stack, assuming the three transistors are not collinear. Note that the triple stacked design as compared to a single transistor on the same W/L is going to be ~3x the size, ~3x the capacitive load, and ~1/3x drive. So, this design concept is expensive in terms of size and performance penalties versus a single transistor, but is a way to get SEE robustness that may otherwise be unobtainable.

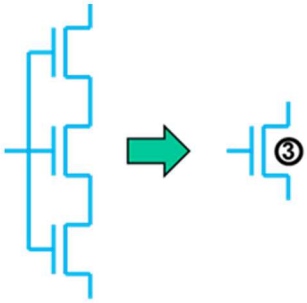

Fig. 3. Triple stacked transistor (left side) circuit with simplified schematic representation (right side).

A triple stacked transistor memory element for a latch is shown in Fig. 4. This design uses a NAND2 gate so that the latch can be asynchronously reset and an enabled inverter to select sample or hold. In static mode, NR and E are logic high and NE is logic low. In this latch design, ion strikes to five of the eight transistor stacks (designated with a small color box to their right) could cause an upset in the latch in this static mode. The color box next to each transistor stack corresponds to the layout at the bottom of the figure, which shows the relative placement of the three transistors in each of the five different transistor stacks. Note that the transistor placement of each stack is a right triangle pattern. This design and layout was performed in Global Foundries' 32 nm SOI process. The PMOSFETs are all drawn 600 nm/40 nm, the NMOSFETs in the inverter are 600 nm/40 nm, and the NMOSFETs in the NAND2 are 1200 nm/40 nm. In comparison, a basic unhardened latch design in this technology used PMOS and NMOS transistors that were 200 nm/40 nm and 400 nm/40 nm, respectively, that provides an equivalent output drive to the triple stacked design.

B. Stacked DICE Latch

A hybrid design combining the double stack and DICE concepts in a latch, called the stacked DICE, is shown in Fig. 5. The basic concept of the layout is that a single ion strike must deposit charge in four silicon islands to flip the latch, two stacked transistors of DICE susceptible pairs. The stacked transistors' redundancy is in the x-direction and the DICE redundancy is in the y-direction as shown in the relative placement diagram below the stacked DICE schematic in Fig.

4. Note that this is the first pass layout incorporated in the Global Foundries' 32nm SOI process and it does show SEU susceptibility to single heavy ion irradiation using MRED (discussed below). The PMOSFETs are all drawn 200nm/40nm, the NMOSFETs in the inverter are 200nm/40nm, and the NMOSFETs in the NAND2 and 400nm/40nm. In comparison, a basic DICE latch design incorporated in this technology used transistors that were the same size, which would have doubled the drive strength compared to the stacked DICE.

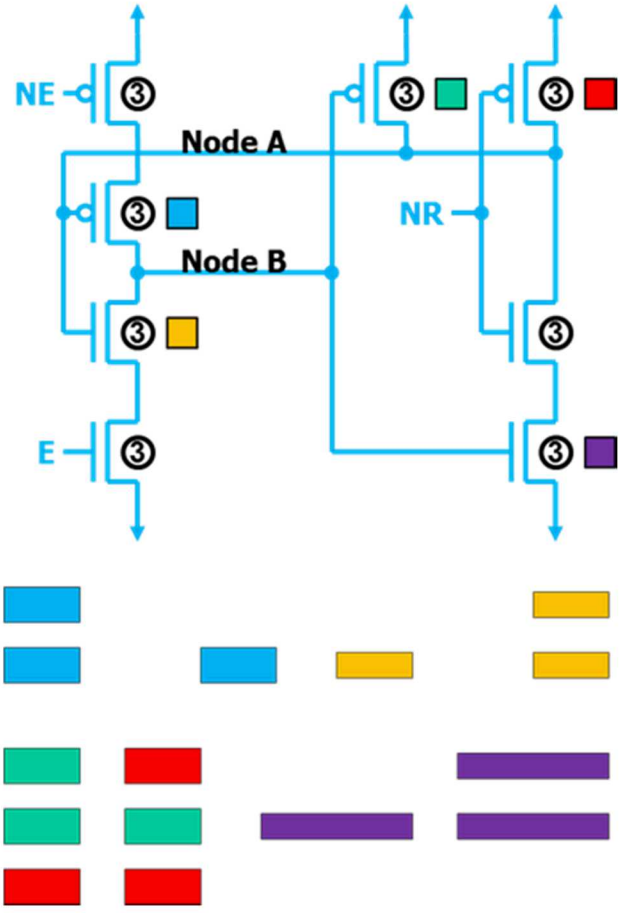

Fig. 4. Triple stacked transistor latch showing layout of susceptible circuit nodes.

IV. MRED Simulation

To provide some verification of the layouts, we ran simulations in the MRED tool [9-10]. This tool was developed by Vanderbilt University and is licensed by Sandia National Laboratories. The procedure used to perform this evaluation was to assess proposed latch schematics in a static (unclocked) mode, looking for the transistors that could cause the latch state to switch. This included both ON and OFF transistors since we assume the latch could be in either state. We defined the entire Si volume as the charge collection region for each of these transistors. Any charge deposited in this volume is assumed to be fully collected. In addition to the triple stacked latch layout shown in Fig. 4 and the stacked DICE latch layout shown in Fig. 5, a standard latch layout and a DICE latch layout were evaluated. The standard latch was the same schematic as Fig. 4 except that all transistors were singular and the DICE latch was the same schematic as Fig. 1.

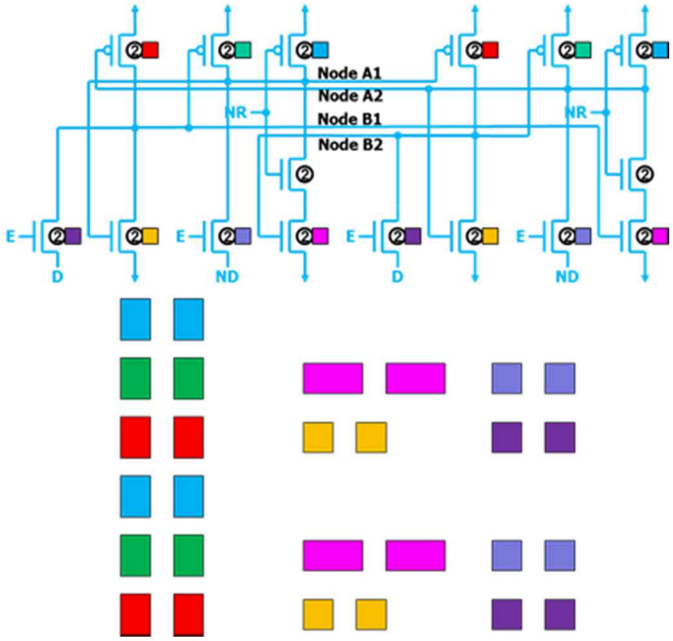

Fig. 5. Stacked DICE design with relative transistor placement.

MRED executed 100 million ion strikes of five different ions, based upon the test campaign used at the Texas A&M cyclotron facility, in both normal incidence and isotropic incidence for all four layouts. The ions and energies are provided in Table I. The simulated "world" used for the random ion strikes was 10 μm x 10 μm x 1 μm in all cases. All events in which 0.0001 fC or more was deposited were analyzed; Events that did not have at least one volume collect 0.0001 fC of energy deposited in one sensitive volume were discarded. The remaining events were analyzed by custom Python scripts. In the standard latch, all remaining cases are counted as upsets. In the DICE latch, only strikes with dual node charge collection for appropriate pairs were counted, though all cases on single strikes were also tabulated. For the triple stacked design, only strikes in all three volumes of the same transistor were counted, though all other events were tabulated. Finally, for the stacked DICE, only strikes in four appropriate volumes were counted, all other events were just tabulated. The results are provided in Tables II and III.

TABLE I
MRED Simulated Ions

Element	Atomic Number	Atomic Mass	Energy, MeV	LET at Top of IC
He	2	4	45	0.1
Ni	7	14	178	1.4
Ar	18	40	531	8.3
Cu	29	63	785	19.6
Kr	36	84	1032	27.8

TABLE II
MRED SIMULATION RESULTS FOR NORMALLY INCIDENT IONS, MINIMUM 0.0001 FC

Latch Type	He		Ni		Ar		Cu		Kr	
	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count
Standard	159	N/A	174,013	N/A	174,111	N/A	175,505	N/A	175,437	N/A
DICE	403	7	444,209	22	446,906	29	445,760	23	446,328	18
Triple Stacked	1,233	0	1,352,175	0	1,259,216	0	1,355,856	0	1,358,271	0
Stacked DICE	737	0	888,719	0	891,480	0	891,156	1	891,545	0

TABLE III
MRED SIMULATION RESULTS FOR ISOTOPICALLY INCIDENT IONS, MINIMUM 0.0001 FC

Latch Type	He		Ni		Ar		Cu		Kr	
	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count	Single Node Event Count	Multiple Node Event Count
Standard	283	N/A	111,815	N/A	151.282	N/A	157,445	N/A	158,036	N/A
DICE	747	7	284,410	814	389,401	868	403,165	946	405,494	874
Triple Stacked	1,698	0	798,883	0	990,497	0	1,013,661	4	1,019,973	0
Stacked DICE	1,378	2	553,376	114	752,736	154	778,702	166	783,126	160

While it was not expected, the simulations show that there are potentially observable upsets at normal incidence for the DICE latch layout. MRED output 7, 22, 29, 23, and 18 multiple node events from He to Kr. But, a more detailed analysis of the charge collection shows that at least one node collected less than 0.1 fC for most of the events. Simple circuit simulation using double exponential current sources [11] on the node pairs provides several curves like the one provided in Fig. 6 [12 – Wole]. In this case, the minimum charge collection on each node is 1.1 fC and minimum combined collected charge is 10.1 fC. Adding that criteria to the multiple node event count leaves a single SEU possible with Cu and two SEUs possible with Kr. An example MRED output showing double node charge collection with a normal incident Kr particle is shown in Fig. 7.

Performing a similar circuit simulation with the standard latch finds that single nodes are potentially upset with charge collection varying between 3.5 and 6.1 fC. Adding that criteria to the MRED results reduces the single node event counts for He and Ni at normal incidence, but does not significantly affect the rest. So, these results would suggest that a standard DICE latch incorporated in Global Foundries' 32nm SOI technology would be 10^5 times less likely to upset than the standard latch, 2 vs. 175k, at normal incidence. If you observe one upset every 10^5 particles/cm^2 in the standard latch, then you would have to test greater than 10^{10} particles/cm^2 to ensure that you would observe a DICE latch upset. The isotropic simulation case, which is more consistent with the space environment, shows the true susceptibility of the DICE latch. In this case the number of observed events with Kr increases from 2 to 762 (112 of the 874 events in Table III did not meet the double node charge collection criteria) ~400 times more events than observed for normal incidence ions. Even with the increased number of events, the DICE latch provides an improvement of a factor of ~2x10^2 over the standard latch with respect to cross-section.

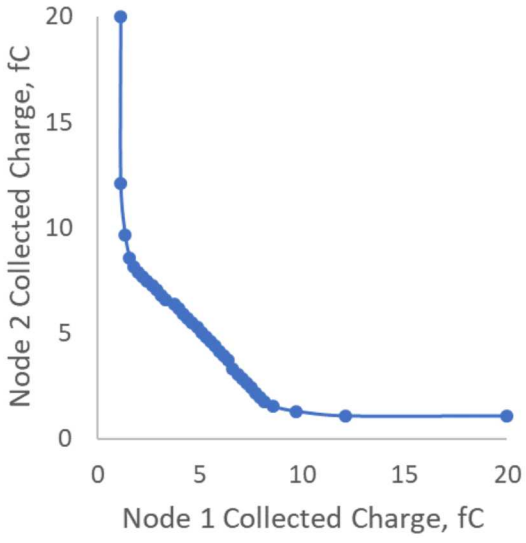

Fig. 6. Sample DICE latch two node charge collection SEU analysis for one set of circuit node pairs.

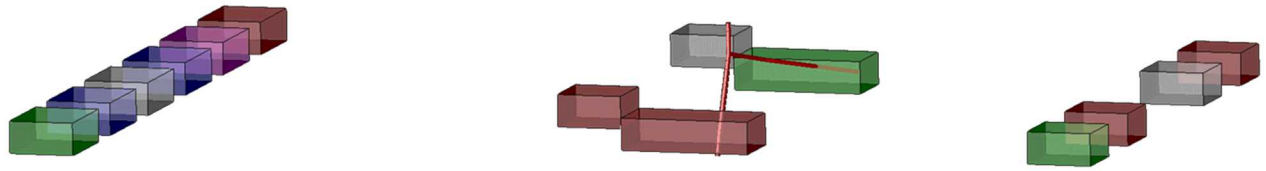

Fig. 7. Example MRED simulation output showing multiple node charge collection in DICE latch, 2 PMOSFETs.

The triple stacked latch fared well in this analysis, with only four multiple node events counted with Cu in isotropic simulation. Examining these four instances yields the following charge collections on the three nodes:

- 0.01 fC, 4.11 fC, 0.06 fC
- 0.10 fC, 0.12 fC, 0.31 fC
- <0.01fC, 38.77 fC, 20.12 fC
- 44.98 fC, 113.17 fC, 0.08 fC
- 0.15 fC, 0.43 fC, 2.38 fC
- 0.01 fC, 0.01 fC, 1.15 fC
- 0.07 fC, 0.07 fC, 88.57 fC
- 0.04 fC, 87.15 fC, 42.70 fC

It is noted that each of these cases provided two instances of triple node co-incident charge collection and always associated with the red and green boxes in the lower left part of Fig. 4. Unfortunately, the authors do not know of any circuit simulation method to use on TICT or stacked transistors that would provide good estimates for minimum charge collections. 3D Technology Computer Aided Design (TCAD) would be a suitable simulation tool to address this, but we do not have a model for the 32nm process. However, if we apply the DICE results and assume that each node needs at least ~1 fC, then none of these cases would cause an upset.

The interesting item to note from the four cases listed above, they appear to be from lateral ion strikes traversing left to right (or right to left) as depicted in Fig. 4. Given that the DICE latch had some potential double node events at normal incidence, it seems possible that ions traveling from left to right on Fig. 4, might lead to charge collection in all three nodes. We executed this scenario in MRED and obtained five triple node events, though in all these cases the third node collected less than 1 fC. These results suggest that the triple stacked latches with the right-angle layout should be very robust to signal-event effects.

On the other hand, the stacked DICE design/layout did not meet the expected robustness. In the isotropic simulation, there were many events that deposited charge in four distinct nodes with all the ions. Many of those can be disregarded with less than 0.1 fC charge deposition in one of the nodes, but not all. What remains are NMOSFET/PMOSFET stack charge collections on opposite nodes, for example nodes A1 and B1 (Fig. 5). A couple identified ion tracks (black lines in the figure) are shown in Fig. 8. The main issue with the layout approach used is that the PMOSFETs are all on the left and the NMOSFETs are all on the right. To make this layout more robust, all the NMOSFET stacks on nodes A1 and A2 and the PMOSFET stacks on nodes B1 and B2 need to line up in the opposite direction of the stack. Likewise, for the NMOSFET stacks on nodes B1 and B2 and the PMOSFET stacks on A1 and A2. This can be done; however, it results in a more complicated layout which increase the area penalty of using the stack DICE latch design.

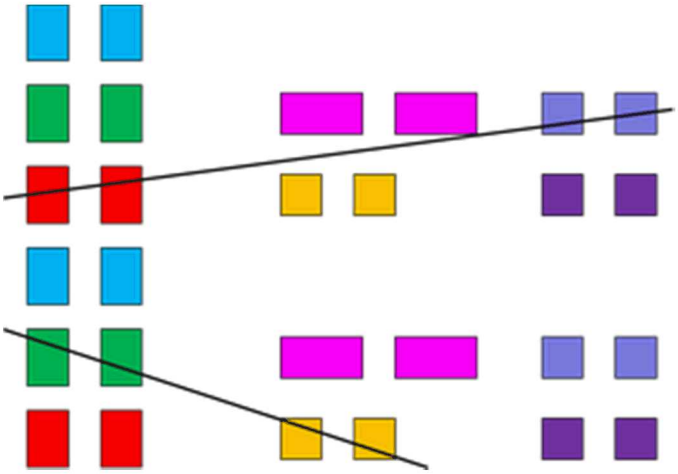

Fig. 8. Stacked DICE latch layout showing susceptible ion tracks that could lead to SEU.

V. Single Event Upset Test Results

All the latches listed in Tables II and III were used to design 2k shift register arrays in Global Foundries' 32nm SOI technology for SEU testing. Two identical 2k shift registers were used in a test structure with an BIST error detector examining their outputs. Both shift registers share a common clock and reset input, while the D inputs and Q outputs were separate. In SEU testing, the D inputs are tied together so the shift registers get the same data pattern. The BIST error detector is designed with the triple stacked latch elements. The test structure layout was performed so that the metal traces to and from each identical shift register were as close to equal as possible.

Before SEU testing, the BIST error detector circuits were evaluated on each test structure. This was accomplished by making the two differing data inputs; for example, one constant input and one pulsed.

The test structures were evaluated at the Texas A&M Cyclotron with the 15MeV/u ion beam with nominal biases of 0.9V. The ions and energies used are provided in Table I. The only upsets observed were in the standard latch design, the triple stacked transistor latch and DICE latch designs showed

no upsets. The testing was mostly done at normal incidence with some tests at 45 degrees of incidence. The IC package used prevented increasing the angle of incidence beyond 45 degrees. The test results for the standard latch at normal incidence are shown in Fig. 9. Overall, this is higher SEU cross-section than previous data for this process, but consistent with the shape [13]. Also shown on this chart are the MRED determined cross-sections for the standard latch and the DICE latch. Note we over-predict the cross-section for the standard latch, but that is expected given the fact we used the entire Si volume as fully collecting the deposited charge, which would not be the actual result.

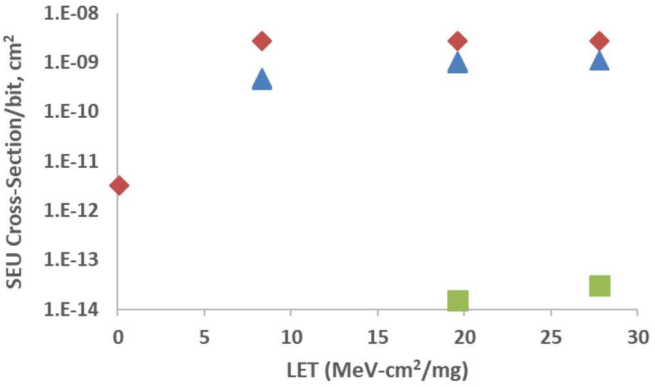

Fig. 9. SEU test results for the standard latch (blue triangles). Also shown are normal incident cross-sections from MRED simulation for the standard latch (red diamonds) and DICE latch (green squares).

Based upon the data, the standard latch upsets with about every $2.5x10^5$ particles/cm^2. From the MRED simulations, this shows the need to test to $>1x10^{11}$ particles/cm^2 to get a few upsets in the DICE latch, versus the $1x10^8$ particles/cm^2 maximum that was used. The MRED simulation also shows that if we wanted to observe lower LET upsets, we should have tested to $>1x10^9$ particles/cm^2. Finally, the MRED analysis showed that we should not have seen upsets on the triple stacked design, which agreed with the experimental data.

VI. Conclusions

This paper has presented two new latch designs/layouts, triple stacked and stacked DICE for more robust SEU circuits. The design/layout of both these latches demonstrates that the triple stacked version would be much easier to implement. MRED analysis has shown that it should provide a very robust SEU mitigation and no upsets were observed in the test structure fabricated using this latch design.

This paper has also demonstrated the utility of a tool like MRED to examine layouts prior to fabrication. With a simple analysis, MRED demonstrated flaws in the stacked DICE layout. It also demonstrated the robustness of the triple stacked approach. Finally, MRED allowed ion simulation that is unavailable or at best very difficult and time consuming in ground-based accelerators.

VII. References

[1] P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, and J. A. Felix, "Current and Future Challenges in Radiation Effects on CMOS Electronics, *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 1747–1764, Aug. 2010.

[2] L. R. Rockett, Jr., "Simulated SEU hardened scaled CMOS SRAM cell design using gated resistors," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 5, pp. 1532–1541, Oct. 1992.

[3] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2874–2878, Dec. 1996.

[4] K.K. Ma, Radiation-hardened transistor and integrated circuit, US Patent 7,298,010, 2007.

[5] K. P. Rodbell, D. F. Heidel, J. A. Pellish, P. W. Marshall, H. H. K. Tang, C. E. Murray, K. A. LaBel, M. S. Gordon, K. G. Stawiasz, J. R. Schwank, M. D. Berg, H. S. Kim, M. R. Friendlich, A. M. Phan, and C. M. Seidleck, "32 and 45 nm Radiation-Hardened-by-Design (RHBD) SOI latches," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2702–2710, Dec. 2011.

[6] R. Lacoe, "CMOS scaling, design principles and hardening-by-design methodologies," presented at the IEEE NSREC Short Course, Monterey, CA, USA, 2003.

[7] K. M. Warren, B. D. Sierawski, R. A. Reed, R. A. Weller, C. H. Carmichael, A. Lesea, M. H. Mendenhall, P. E. Dodd, R. D. Schrimpf, L. W. Massengill, T. Hoang, H. Wan, J. L. De Jong, R. Padovani, and J. J. Fabula, "Monte-Carlo based on-orbit single event upset rate prediction for a radiation hardened by design latch," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2419–2425, Dec. 2007.

[8] P. Marshall, M. A. Carts, S. M. Currie, R. A. Reed, B. A. Randall, K. E. Fritz, K. Kennedy, M. D. Berg, R. Krithivasan, C. M. Seidleck, R. L. Ladbury, C. J. Marshall, J. D. Cressler, G. F. Niu, K. A. LaBel, and B. K. Gilbert, "Autonomous bit error rate testing at multi-gbit/s rates implemented in a 5 AM SiGe circuit for radiation effects self test (CREST)," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2446–2454, Dec. 2005.

[9] R. A. Weller, R. A. Reed, K. M. Warren, M. H. Mendenhall, B. D. Sierawski, R. D. Schrimpf, and L. W. Massengill, "Monte Carlo Simulation of Single Event Effects," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 1726-1746, Aug. 2010.

[10] R. A. Reed, R. A. Weller, M. H. Mendenhall, D. M. Fleetwood, K. M. Warren, B. D. Sierawski, M. P. King, R. D. Schrimpf, and E. C. Auden, "Physical processes and applications of the Monte Carlo radiative energy deposition (MRED) code," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1441-1461, Aug. 2015.

[11] G. C. Messenger, "Collection of Charge on Junction Nodes from Ion Tracks," *IEEE Trans. Nucl. Sci.*, vol. 29, no. 6, pp. 2024–2031, Dec. 1982.

[12] O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, S. DasGupta, A. L. Sternberg, P. R. Fleming, C. C. Heath, and M. L. Alles, "Directional Sensitivity of Single Event Upsets in 90 nm CMOS Due to Charge Sharing," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2584-2589, Dec. 2007.

[13] R. C. Quinn, J. S. Kauppila, T. D. Loveless, J. A. Maharrey, J. D. Rowe, M. W. McCurdy, E. X. Zhang, M. L. Alles, B. L. Bhuva, R. A. Reed, W. T. Holman, M. Bounasser, K. Lilja, and L. W. Massengill, "Heavy ion SEU test data for 32nm SOI flip-flops," in Proc. IEEE Radiation Effects Data Workshop (REDW), Boston, MA, USA, Jul. 2015, pp. 40–44.