SANDIA REPORT

SAND2016-6275
Unlimited Release
Printed July 2016

Insulation Resistance of Flat Flexible Circuit Boards

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Insulation Resistance of Flat Flexible Circuit Boards

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Abstract

The insulation resistance (R_I) between parallel copper traces embedded on flexible, polyimide-based circuit boards was measured as a function of temperature, substrate type, copper thickness, and feature size. The results show a strong dependency on temperature: the measured R_I decreases nearly seven-orders of magnitude upon a 90°C change. Also measured was R_I as a function of the trace and space of parallel copper circuits. This dependency is less obvious but a correlation showing narrower spacing leads to lower R_I is evident. The thickness/width of the copper traces has less of an effect on the measured R_I. The thickness of the polyimide-based substrate, or core of the circuit boards, was also varied. Measurements of the R_I versus substrate thickness were inconclusive. The height of the copper traces was changed and shows that heavier (or taller) traces result in a lower measured R_I. Lastly, it was shown that the adhesive found between the copper traces and the polyimide core on so-called "LF" Pyralux® boards significantly reduces the measured R_I compared to "AP" Pyralux® boards of the same dimensions. The presences of this adhesive in all LF materials, including LF coverlays should be avoided if high R_I is desired for narrowly spaced copper traces. Alternative materials like AP Pyralux® or HT Pyralux® available from DuPont™ should be investigated when designing copper-based flat-flex circuit boards that require demanding environmental specifications.

ACKNOWLEDGMENTS

The data presented in this report do not fully capture the efforts involved in characterizing the insulation resistance of flat flexible circuit boards as a function of temperature. Setting up equipment, experimental protocols, bake-out schedule, measurement parameters and data processing were previously developed by Wiley Neel and Jim Brennan. The flexible board design conceived by Joseph Cordaro and Wiley Neel was drafted by John Warmouth. We also offer credit to panel manufacturer Cirexx International for helping lay out our boards to be manufactured in a reasonable timeframe and cost.

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FIGURES

TABLES

NOMENCLATURE

AP	Adhesiveless type polyimide films
DXF	Drawing Interchange Format
JGCFLEX	the name used for overall pattern of flat flexible circuit boards tested
h	height (also weight of copper in this report)
L	length of copper trace
LF	Polyimide film with adhesive
ℓ	distance between two parallel plate capacitors (also space in this report)
Mil	thousandth of an inch (0.001 inches)
µm	micrometer or micron ($1x10^{-6}$ meters)
Ω	ohm
R_I	insulation resistance
ρ	resistivity
ρ_a	apparent resistivity
SCFH	standard cubic feet per hour
SNL	Sandia National Laboratories
STD-FF-V2	Standard Flat Flex Board Version 2
T/S	trace and space

1. INTRODUCTION

Flat flexible (flat-flex) circuit boards composed of a polyimide Kapton® film core, copper traces, and a Kapton® coverlay are common in many applications, ranging from aerospace to ink jet printers. These boards are typically manufactured at specialized flexible circuit board shops—and the multistep fabrication process requires intense capital investment and expertise. Materials companies such as DuPont™ make the starting copper laminated polyimide films, coverlays, adhesives, etching films and assembly aides; various board shops purchase these materials to manufacture the flexible circuit boards.

The ubiquity of flat-flex boards means a myriad of data exist regarding their physical and electrical properties. However, for one particular application used at Sandia National Laboratories (SNL) characterization of an atypical electrical property is required: characterization of the insulation resistance (R_I) between parallel traces held at constant voltage over a wide temperature range. To obtain this property, an SNL team conducted experimental characterization of seven varieties of flat-flex circuit boards, as described in this report.

The results of this work show how changes in three factors—substrate type, copper thickness, and distance between copper traces—affect insulation resistance. The dependencies revealed between variables will inform future designs of copper-based flat-flex circuit boards to meet challenging requirements. The work described here supplements an initial investigation (detailed in SAND2015-8878) and will likely be followed by future studies.

2. GENERAL CHARACTERISTICS OF TEST SPECIMENS

This section describes the characteristics of the flat flexible circuit board components tested and states the scope and purpose of the testing.

Material Description and Manufacturing

The core of a flexible circuit board is a polyimide film called Kapton® manufactured by Dupont™. The panels are supplied as 24″x36″ sheets with copper foil bonded to the Kapton® core on one or both sides. All boards in this study have copper on both sides.

Materials can be designated *LF* or *AP*. Material designated LF features a proprietary C-staged modified acrylic adhesive between the copper and the polyimide core. Figure 1 shows a cross-sectional schematic of an LF flat-flex board with an LF coverlay. (The coverlay is a polyimide film with a modified acrylic adhesive similar to the LF substrate. All coverlay used in this study were of the type LF0110: 1 Mil (25 µm) polyimide and 1 Mil (25 µm) adhesive. Variations of thickness, copper weight, coverlay type, etc. are available from Dupont™ and other vendors.)

Material thicknesses for individual layers in thousands of an inch, mil (µm)			
Coverlay	Adhesive	Copper	Kapton
1 (25)	0.5 – 1 (12.5 – 25)	0.7 – 1.4 (18 – 36)	2 – 6 (50 – 150)

Figure 1. Cross-section of a double-sided LF stack-up with LF coverlay

Material designated AP has no adhesive between the copper and polyimide. Figure 2 shows a double-sided AP stack-up with an LF coverlay. The amount of copper is typically called out by weight. A 1-oz copper panel has 1 ounce of copper per side, which translates to a thickness of 1.4 Mil (36 µm). A ½ oz. copper panel has a thickness of 0.7 Mil (18 µm) on each side.

Material thicknesses for individual layers in thousands of an inch, mil (µm)			
Coverlay	Adhesive	Copper	Kapton
1 (25)	0.5 – 1 (12.5 – 25)	0.7 – 1.4 (18 – 36)	2 – 6 (50 – 150)

Figure 2. Cross-section of a double-sided AP stack-up with LF coverlay

Flexible circuit boards are manufactured in a clean-room like environment, following these steps:

- Tool, cut, and clean the copper-clad polyimide boards
- Apply a photoresist film to the copper surface using a heated roller
- Cure (crosslink) the photoresist using a laser or traditional masking lithography to "write" the desired traces onto the copper (each panel usually has multiple repeats of the same circuity or "board" and test coupons used for quality control)
- Remove uncured photoresist using a solvent etch
- Remove the exposed copper using a chemical etching process that leaves intact the desired circuitry
- Remove the crosslinked photoresist
- Clean the exposed copper circuits using a mild acid wash
- Apply a coverlay to the panel to protect the copper circuits using a hot vacuum press
- Cut out the individual parts

All board shops must employ rigorous quality control at every step to ensure a high yield. Multiple factors—such as feature sizes, substrate thickness, and etching bath pH—will affect yield. Contaminates can cause shorts or opens in the circuitry. Shorts can be repaired with a fine-tipped tool that scrapes away copper that was not etched properly. Opens are never repaired in standard industrial board shops and result in scrapped parts. For this study, all panels were manufactured at Cirexx International in Santa Clara, California.

Production of Test Panels

Test panels containing ribbon- and lollipop-shaped parts were produced and serialized, as shown in Figure 3. Two panels each of seven different types (see below) were produced.

Panel serial numbers range from 001 to 002 in most cases; in one case, they range from 003 to 004. A part number was assigned to each board on a panel; these numbers range from 01 to 34. An example of a serial and part number would look something like 001_24.

The location of a board of a certain trace and space (T/S) can be found using the diagram in Figure 4. Numbers of part can be correlated to T/S parameters by combining the information in Figure 3 with the information in Figure 4.

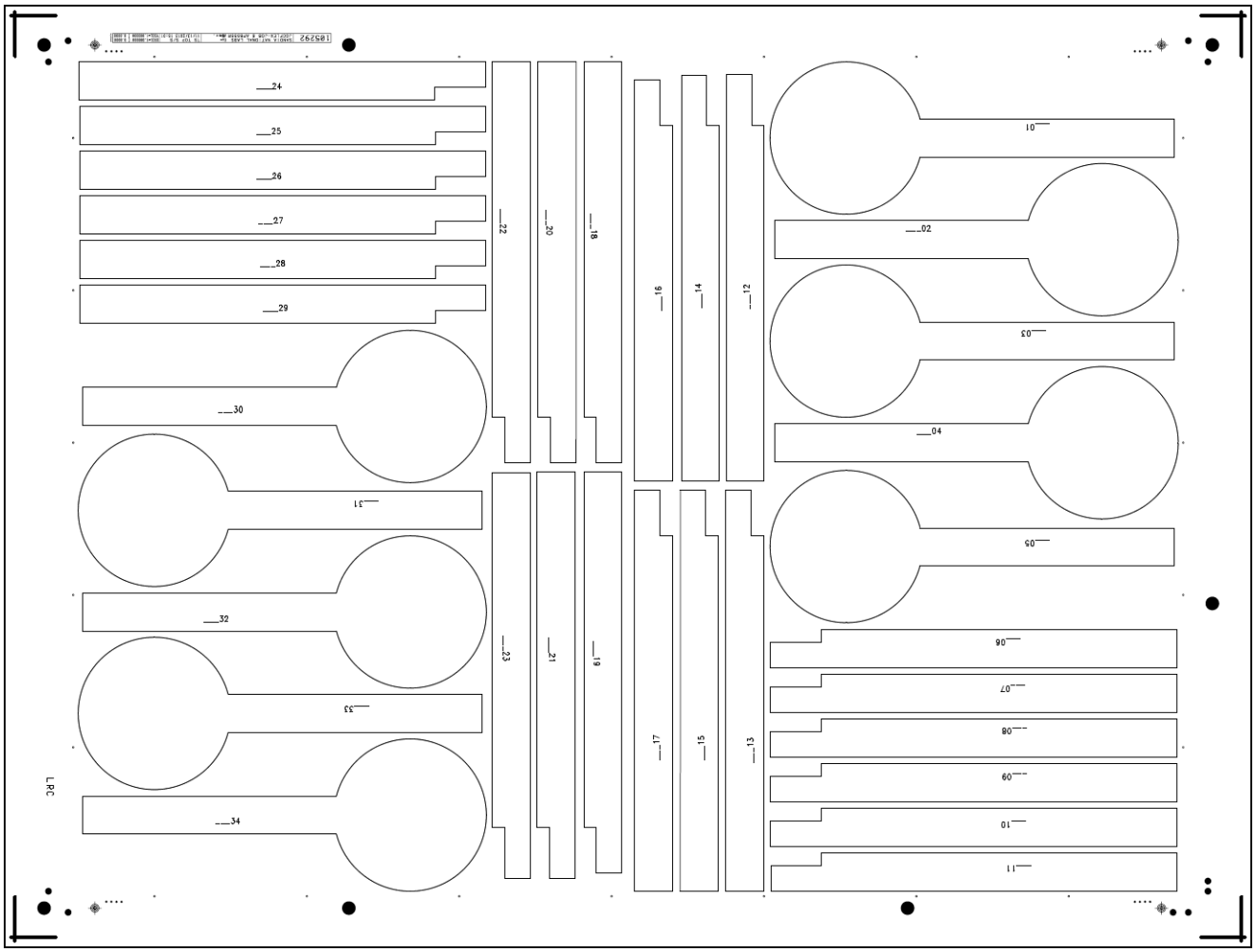

Figure 3. The part number layout scheme as it would appear on a board from the manufacturer

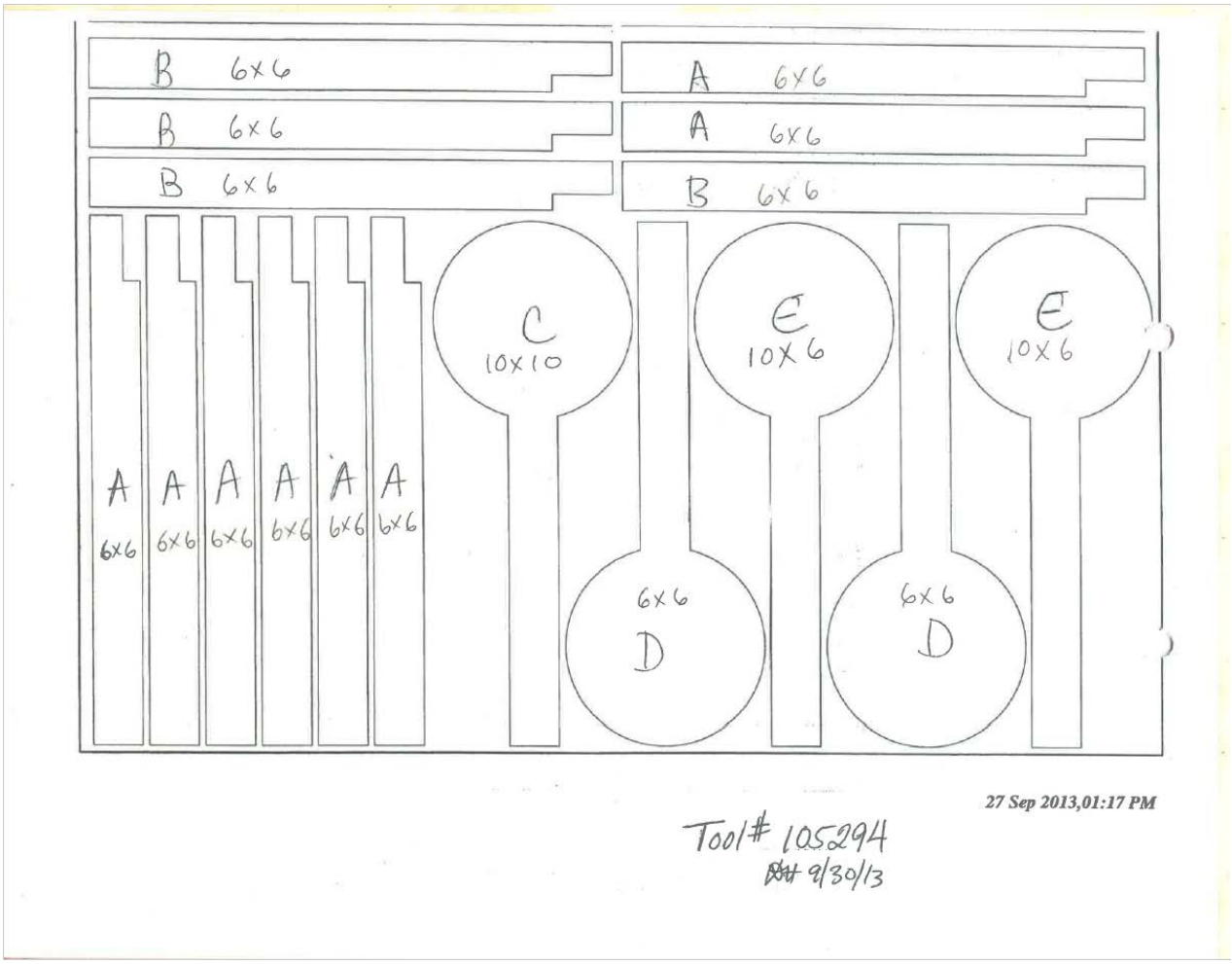

Figure 4. The location of boards by different trace and space

Types of Panels

The seven types of panels manufactured at Cirexx International, referred to as JGCFLEX panels, consisted of the same coverlay (LF0110) and different combinations of the following parameters:

- Material of substrate (LF, AP)
- Weight of copper traces: 18 μm (½ oz.) thick or 36 μm (1 oz.) thick
- Thickness of polyimide substrate

The nomenclature for the boards consists of Job 'n' where, for example, the fourth board type is called Job 4. Table 1 correlates the names of the seven panels to the set of associated parameters.

Table 1. Parameters of 7 Double-Sided Flex Board Types

Nomenclature/LF or AP type	Substrate (Kapton®) thickness (Mil)	Adhesive thickness (Mil)	Copper weight (oz)[a]	Substrate product number[b]	Total thickness[c] Mil (µm)
Job 1 (LF)	2	1	1	LF9121R	10.8 (270)
Job 2 (LF)	2	1	½	LF8525R	9.4 (235)
Job 3 (LF)	3	1	1	LF9131R	11.8 (295)
Job 4 (AP)	4	0	½	AP8545R	9.4 (235)
Job 5 (AP)	4	0	1	AP9141R	10.8 (270)
Job 6 (AP)	5	0	½	AP8555R	10.4 (260)
Job 7 (AP)	5	0	1	AP9151F	11.8 (295)

a) Copper weight: 1 oz = 1.4 Mils (35 µm); ½ oz = 0.7 Mils (18 µm)
b) Product numbers from two brochures: *Dupont™ Pyralux® LF Copper-Clad Laminates* or *Dupont™ Pyralux ® AP Flexible Circuit Materials*
c) All coverlay material was of the type LF0110 at 1 Mil (25 µm) adhesive and 1 Mil (25 µm) Kapton® thick

Geometry

The two types of part geometries found on the seven panel types have the following approximate dimensions:

- Ribbons: ~8″ x ~0.8″ rectangles
- Lollipops: ~3″ diameter discs with a ~5″ x ~0.8″ stem

Two Parallel Traces

All parts contain two copper traces, which originate at the rectangular contact pad (top right) and run in parallel over the entire front and back of the part in a serpentine pattern, as shown in Figure 5. These traces are electrically isolated from one another and jump to the back side of the panel at the villas (small green dots above the serpentine pattern). After completing the serpentine pattern on the back side the traces terminate at the two left contact pads.

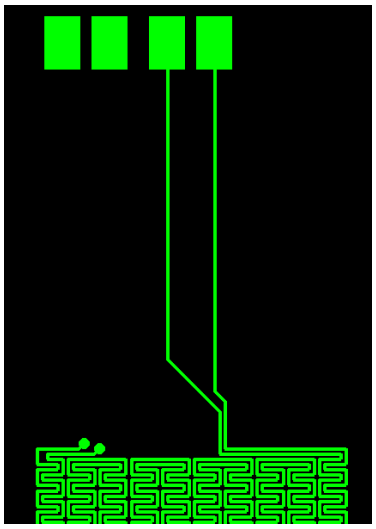

Figure 5. Trace terminals and part of the serpentine pattern of a JGCFLEX test specimen

Variation of Trace and Space

Within each of the Job types, the width of the copper traces and the spacing between the parallel copper traces are varied:

- Trace widths: 0.006″ or 0.010″ (150 µm or 250 µm)
- Spacing: 0.006″ or 0.010″ (150 µm or 250 µm)

The dimension of trace and space is colloquially stated as 6/6, 10/6, or 10/10.

Lollipop parts were manufactured with trace and space (T/S) combinations of:

- 6/6
- 10/10
- 10/6

Ribbons were only made to have a T/S of 6/6.

Total Length

As the space and trace changes on each part, the total length of copper changes. Using a CAD tool and analyzing the DXF file for each part type the total length of each trace (front and back) was calculated and is given in Table 2.

Table 2: Total length of single copper trace for each part

Panel	Trace (thousandths of an inch)	Space (thousandths of an inch)	Total single circuit length (L) (top and bottom) (inches)
Ribbon	6	6	419.0
Lollipop	10	10	340.8
Lollipop	6	6	564.0
Lollipop	10	6	421.9

Full Nomenclature

Boards are named as follows: JGCFLEX-Job‘n’-‘S/N’_‘P/N’-‘T/S’.

In this nomenclature:

- S/N is the serial number
- P/N is the part number
- T/S is the trace and space.

An example name is JGCFLEX-Job4-001_24-6x6

Test data file names are similar to the following: “JGC-JOB4-001-24-001-6x6-001-CC_1_Converted.txt”.

The meaning of this file name will be covered in the Experiment section.

Test Intent/Scope

The intent of the tests were to measure the insulation resistance, denoted as R_I, between the two parallel copper traces over a range of temperatures. The goal was to characterize the effects of varying different manufacturing parameters on insulation resistance.

3. EXPERIMENT

This section describes multiple aspects of the experimental setup used to measure the insulation resistance of the two parallel copper traces on the JGCFLEX boards over a range of temperatures.

Location

The tests were performed Sandia National Laboratories in California in Building 916, room 164.

Equipment

The following equipment was used for all measurements:

- Computer, S990110
- Thermotron oven
- Two Keithley electrometer/high resistance meters 6517B, SNL-203112 and SNL-203095
- Labview program written by Jim Brennan (Org. 08625)
- Weller soldering iron
- Two spools of wire with the following specifications:
  - MIL-w-16878
  - 22 AWG
  - Type: ET
  - Color: Lavender/Grey
- Kapton® tape
- Wire strippers and cutters
- Solder, SNL chemical inventory number: LV00123858
- Keithley multimeter

Specimen Preparation

The following tasks were performed for specimen preparation:

1. Individual boards were cut from the panels.
2. Two separate wires were soldered at 440°F to the right-most copper contacts (reference Figure 5). If the connections from these contacts to the traces were damaged, the left-most copper contacts were used.
3. The wire leads were labeled (for example, as “Job 4 001_24”) to indicate the type of board and to allow identification of boards in the oven from outside the oven. Connectivity checks were performed with the multimeter.

System Hardware Preparation

System hardware preparation entailed the following steps:

1. A maximum of two specimens were placed in the oven with the leads running out of a thermally insulated port located on the left side of the oven. Two thermocouples were placed in the oven using this port and fastened to the specimens using Kapton® tape. The oven was shut and sealed.
2. Outside of the oven, the positive voltage lead from one of the electrometers was connected to one of the leads from one of the specimens and the ground lead from the

electrometer was connected to the other lead from the specimen. The same was done for the second electrometer and the second specimen.

Purge, Bake, and Sweep

These steps were performed as part of the purge, bake, and sweep activities and partially controlled in LabVIEW

1. The nitrogen valve near the oven was opened to allow a flow rate of approximately 15 standard cubic feet per hour (SCFH). Within the LabVIEW program, the nitrogen purge duration was set to 1.5 hours.
2. To remove any moisture, a bake-out was set as follows: 120°C; 3-hour duration; and ON.
3. The temperature setpoints were set to 120°C and 30°C.
4. The data output location was set and the data files were given names in this format: JGC-JOB'n'-'S/N'-'P/N-001-'T'x'S'-001-CC, where
   - 'n' is the board type (see Table 1)
   - 'S/N' is the serial number of the panel
   - 'P/N' is the board part number (see Figure 3)
   - 'T' and 'S' are trace and space, respectively
   - The two instances of '001' are artifacts and were left in the file names for consistency with older tests
   - CC represents a fixed (or constant) current range throughout the duration of the temperature sweep
5. Once the program was set to run, these steps occurred:
   - The oven was purged with nitrogen for the purge duration.
   - The oven controller brought the oven temperature up to 120°C and held for three hours to bake-out moisture and purge the oven.
   - After bake-out, the two Keithley meters chose an optimal current range for the resistance measurements, a range which would remain constant throughout the sweep. (Note: What may have been optimal at 120°C might not have been optimal at 30°C due to changes in R_I. However, changing the current range mid-test produced unwanted spikes in the data.)
   - Once the current range was established, a bias of 12V was applied and the oven was brought to the first set temperature (usually 120°C).
   - In some tests, the oven was unable to reach the setpoint due to a discrepancy between the oven thermocouple and the thermocouple attached to the test specimen. The reading taken by the thermocouple attached to the test specimen was used as the input variable for the control loop. The oven thermocouple reported the current oven temperature to the oven. Thus it was possible for the oven to "think" it had reached 120°C and the test specimen thermocouple to read the oven temperature as something lower, maybe 118°C. As the input control variable, the test specimen thermocouple is waiting to read the setpoint temperature. If the setpoint temperature was not reached the test sequence would not progress to the next setpoint (usually 30°C). Consequently, in early studies when a difference (or margin) between the oven and specimen thermocouple temperature was greater than 1.7°C, the test sequence did not begin but held a 12V bias attempting to reach the setpoint temperature. Increasing the margin to 2.5°C eliminated this issue in subsequent tests.

6. After completing measurements, data were simplified using a separate LabVIEW program to output four columns:
   - Insulation resistance
   - Temperature (read by thermocouple #1)
   - Temperature setpoint
   - Time

   The names of the converted files gained the extension ‘Converted’ and looked something like: JGC-JOB4-001-24-001-6x6-001-CC_1_Converted.txt. (Note: the ‘1’ that appears before ‘Converted’ is added by the LabVIEW program to indicate the first run.)

Data Processing

Most data with the JGCFLEX board tests were processed using Excel. Large data sets with file sizes on the order of megabytes had to be processed using MATLAB. Troy Dillinger (Org. 08221) produced a script for this purpose.

4. RESULTS AND ANALYSIS

This section presents results and analyses of the measured data. Plots of the insulation resistance versus temperature can be found in the appendices. Specifically, Appendix A contains plots for trace and space comparisons, Appendix B contains plots for copper weight comparisons, Appendix C contains plots for substrate thickness comparisons, and Appendix D contains plots for substrate type comparisons.

Temperature

All plots shown in the appendices are plotted using a $\log_{10}$-based y-axis for the resistance measured in ohms (Ω). The x-axis is given in temperature (°C). The insulation resistance between two serpentine copper traces is inversely related to the temperature of the board. The measured insulation resistance decreases with temperature up to seven-orders of magnitude over a 90°C temperature change.

Comparing Trace and Space

The plots in Appendix A show the effects of T/S on the apparent resistivity while keeping other parameters constant. Since the measured R_I does not account for a change in total length (and hence surface area), results were normalized to account for the different copper circuit lengths. As seen in Table 2 the lengths of the lollipop parts vary from 340 to 564 inches. The measured insulation resistance in ohms (R_I) was normalized by taking the product of the measured R_I and total length (L). This normalization is based on a parallel plate capacitor model, which suggest that the width of the copper traces should not affect the measured R_I given everything else remains unchanged. For these parts, the total surface area of the part is fixed. The copper height is also fixed for a specified Job. This simplifies the normalization process and allows for the y-axis in Plots 1 – 7 of Appendix A to be labeled as $\log_{10}$(apparent resistivity) in units of $\rho \cdot A \cdot \ell^{-1}$ or simply Ω·in. While this normalized value has the units of resistivity, it is a combination of surface and volumetric properties and should be considered the apparent resistivity, ρ_a.

It was expected that increasing the space between traces (ℓ) would increase the apparent resistivity, ρ_a. The plots shown in Appendix A partially support this hypothesis. Data from Job 1 are unexpected and when the parts where re-measured the apparent resistivity did not match the original data (designated at 6x6-2 and 10x10-2). Job 2 data followed the expected trend with 10x10 parts having the highest measured resistivity after normalization. The apparent resistivity for 10x6 and 6x6 were nearly identical confirming the hypothesis that the space between parallel traces dominates the measured R_I. More ambiguity is evident in Job 3. Specifically, the curves for apparent resistivity versus temperature cross-over more than one time.

Jobs 4 – 7 all follow the same order for apparent resistivity: 10x10 > 10x6 ≈ 6x6. Prior to normalization when data were plotted as the measured R_I, the 6x6 curve was the lowest. However, upon accounting for the 35% longer traces in the 6x6 parts it become clear that the main factor controlling R_I is the space between traces.

The inconsistent results measured for LF-type boards (Jobs 1 – 3) compared to the AP-type boards (Jobs 4 – 7) may be attributed to the presence of an adhesive between the copper and

polyimide Kapton core. In the manufacturing process, the adhesive should be removed during one of the etching steps. If narrow spacing prevents complete removal of the adhesive, residual adhesive in the part could affect the measured R_I. AP boards with no adhesive (except for on the coverlay) would not suffer from this manufacturing variable. No data are available to support this hypothesis but it could be investigated if LF-type boards are selected for high R_I applications.

Comparison of Copper Weight (Height of Trace)

The plots in Appendix B show the effect on R_I of varying the copper weight while keeping other parameters constant. These measurements were performed using both LF and AP substrates and with all T/S combinations. The initial prediction, based upon a parallel plate capacitor model, suggests that for a reduced surface area, a higher R_I should be measured. The data show that, in general, an inverse relationship between R_I and copper height is measured. For taller (1 oz.) copper traces, is R_I lower and for ½ oz. copper traces.

Comparison of Substrate Thickness

The plots in Appendix C show the effect on R_I of varying the thickness of the substrate while keeping other parameters constant. It was expected that a thicker substrate would have a higher measured R_I if leakage from the top to bottom circuit was occurring.

The data collected were inconsistent. Comparisons of Job 1 and 3 (Figures C-1 and C-2) show the thicker core to have a higher R_I for 10/10 and 10/6 T/S. However, a higher R_I was observed for the thinner-core Job 1 with a 6/6 T/S. This inconsistency could be the result of switching data or an unexplained phenomenon where leakage current from top to bottom is significantly affected by the copper trace thickness.

The fact that most boards tested in this series of measurements had undergone previous testing may provide another explanation for the anomaly. It was originally believed that all effects occurring during the testing within this study were reversible. However, the data seen in the “Burned” Boards section would indicate otherwise. Thus, the history of a test specimen—which may be unknown—could be the source of certain unexpected results.

Comparisons between Job 4 and Job 6 (Figure C-4) reveal more unexpected results. The measured R_I for 10/10 is greater than that for 10/6, which is greater than that for 6/6. However, R_I is higher for the 4-Mil core than for the 5-Mil core. It is possible that the boards were switched and labeled incorrectly. (Data were not normalized for copper length.)

Finally, the AP board comparisons between Job 5 and Job 7 (Figure C-4) show the measured R_I for 10/10 is greater than that for 10/6, which is greater than that for 6/6 and that R_I is higher for 5-Mil than for 4-Mil, as expected. (Data were not normalized for copper length.)

Comparison of Substrate Type

The plots in Appendix D show the effect on R_I of varying the type of substrate while keeping other parameters constant. In all cases, the boards manufactured from an AP core (with no adhesive) showed a higher measured R_I. These results were expected, based on the lower volume resistivity and surface resistance of LF materials compared to AP materials. Specification sheets

from Dupont™, which provide these values, should be consulted when designing flexible circuit boards for atypical applications.

5. “BURNED” BOARDS

This section discusses the effects of exposing boards to high temperature for long durations.

Effects of Long Exposure to High Temperature and Voltage

Two factors led to a failure to achieve temperature setpoints in portions of these measurements:

- An offset between the temperature read by the thermocouple and the temperature read by the oven
- A low margin for acceptable setpoint error set in the LabVIEW program

In the sweep phase of one particular test of Job 4 10/6 boards, the thermocouple failed to register that the oven had reached the 120°C setpoint. As a result, the oven stayed at nearly 118°C for approximately 92 hours while a 12V bias was applied. A subsequent test of these “burned” boards under normal purge, bake, and sweep conditions showed that long exposure to high temperature and voltage bias resulted in an insulation medium with higher impedance than that of the untested medium.

Follow-Up Tests

The following test sequences were performed on previously untested Job 4 6/6 ribbons to better quantify the phenomenon described above:

- **Test 1**: A standard purge, bake, and sweep test was run on the test specimens to establish a baseline for R_I. The test specimens were held at 118°C with a 12V bias for 92 hours. A second standard purge, bake, and sweep test was run on the specimens to demonstrate changes in R_I. Results are shown in Figure 6.
  Test 2: Using the same boards tested in Test 1, a standard purge, bake, and sweep test was run approximately 4 months later to demonstrate the permanence of the observed effect. Results are shown in Figure 6 by the green data points.
  Tests 3a-3e: A baseline R_I was established as before. The test specimens were held at 30°C with a 12V bias for 92 hours. Then a second standard purge, bake, and sweep test was run on the specimens to demonstrate changes in R_I. This test was repeated using the following temperatures: 50°C, 70°C, 100°C, and 120°C. Results are shown in Figure 7.

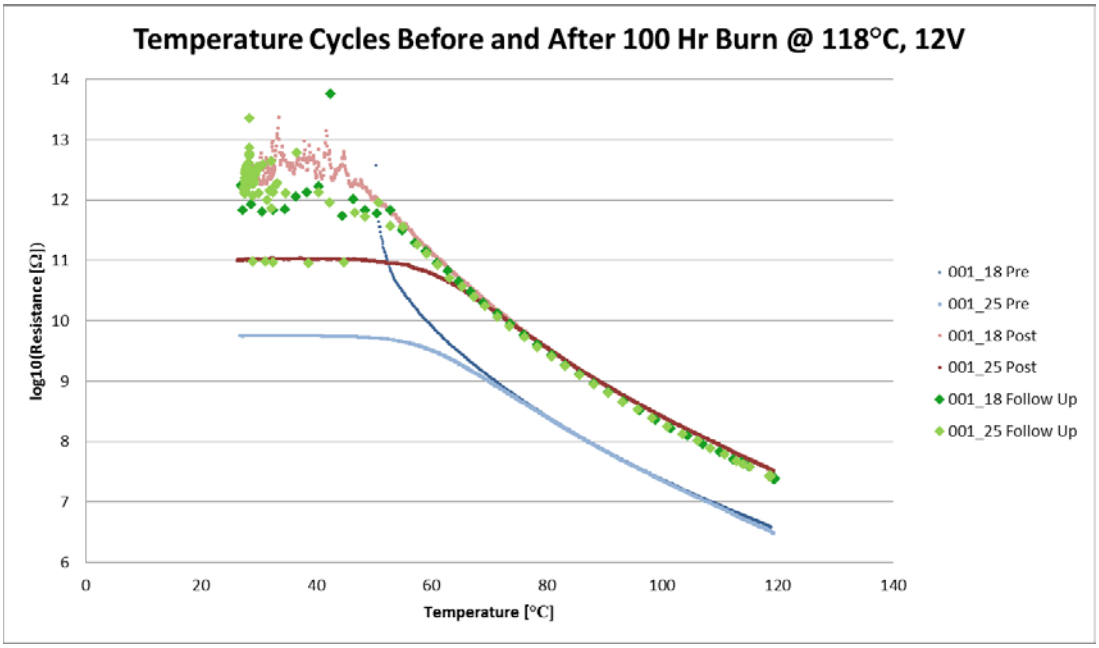

Figure 6. R_I values of two test specimens (labeled 18 and 25) before (blue) and after (red) the long hold at high temperature and 12V bias. A follow-up test conducted approximately four months later produced the R_I data points in green.

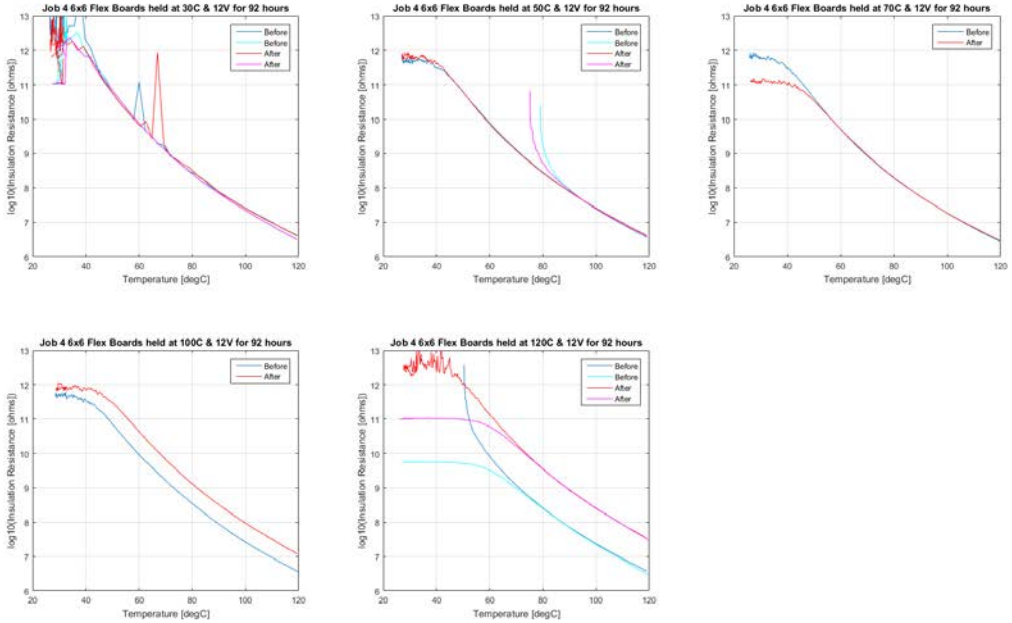

Figure 7. R_I curves for test specimens held at various temperatures (30°C, 50°C, 70°C, 100°C, and 120°C) with a 12V bias applied

Remarks on the Results

The large increase in R_I measured after 92 hours at 118°C and a 12V bias (or "hold") could be attributed to reversible polarization of the adhesive between the copper traces. However, upon retesting "burned" boards after four months, the measured R_I remained high suggesting that the process is irreversible. It appears that application of a high temperature and bias may create a permanent effect. This effect seems to be proportional to the temperature at which the test specimens are held. For the specific boards used to demonstrate this effect, the emergence of this effect exists at some temperature between 70°C and 100°C. When a board was held at 30°C and 12V, no change in R_I was measured. While no test was performed to confirm, we assume that a board held at 120°C for 92 hours without bias would show no change in R_I compared to virgin boards. This assumption is based on the fact that normal LF or AP boards are laminated at 192 – 199°C for 1 – 2 hours during the manufacturing process. Burn-in effects are common in microelectronics but were not anticipated for flat-flex cables. The fact that an adhesive is present between the copper traces could explain the temperature dependency of the burn-in onset. More work is required to understand these recent observations.

6. DISCUSSION

The materials, panel layout, and board designs were selected to provide a platform to measure both intrinsic and extrinsic properties affecting the insulation resistance. The two most significant intrinsic dependencies were space width and substrate material. Traces closer together give a lower measured R_I than do traces with wider spacing. Normalization of R_I to account for the total length of trace on each board confirmed the direct relationship between spacing and apparent resistivity.

The adhesive present between the Kapton® core and copper on LF panels yields an order of magnitude difference in R_I over the measured temperature range compared to the R_I of panels using AP substrates. It should be noted that AP boards had a coverlay (LF0110) with an adhesive. Until mid-2015, LF-type coverlays with adhesive were the only available material sold by DuPont™. Since that time, a new coverlay without an adhesive was released, designated as Pyralux® HT. Measurements of AP substrates with HT coverlay, the subject of a subsequent report, show significantly higher measured R_I values than those with the LF coverlays.

Substrate thickness and copper weight can both be tuned to optimize R_I, but the effects are small compared to the effects of substrate type and copper spacing. The most significant extrinsic variable is temperature. A seven-order magnitude change in R_I is measured over a 90°C temperature change.

These selections should produce a flexible circuit board with the highest R_I over a given temperature range (listed in order of importance):

- An adhesiveless-type substrate and coverlay (AP or HT)
- Wider copper spacing
- Lighter copper (½ oz. or ¼ oz.)
- Thicker core

7. FUTURE STUDIES

The following studies are recommended to provide further insight into some of the results discussed in this report.

The Semi-Permanent Polarization Counterargument

When a voltage bias is applied at certain high temperatures, some kind of polarization is occurring that could not occur at lower temperatures—a phenomenon that provides a possible counterargument for the permanence of the effect seen in the "Burned" Boards section. Because the boards are cooled down to room temperature while the bias is still applied, the state of the polarization remains fixed even after the bias is removed. To test this hypothesis, a board that had already experienced the aforementioned effect could be brought up to temperature and the polarity could be reversed. Examining the results would determine if the R_I of the material was reversed, i.e., returned to its original value.

Demystifying Unexpected Results by Analyzing Test Histories

As discussed in the Results and Analysis section, several plots showed unexpected results. One proposed possibility for these results—that the test histories of the specimens affect the measured R_I—is supported by the "Burned" Boards study. Nearly every board tested in this report had been tested before. A review of the test records could reveal a correlation between unexpected results from certain boards and the test histories of those boards.

Standard Flat Flex Version 2 (STDFFV2)

Given some of the results discussed above, a new flat-flex board (designated STD-FF-V2) was designed and fabricated in early 2016. The T/S parameters, total length of each circuit, and substrate type were all varied to systematically understand some of the ambiguous relationships found for JGCFLEX. The forthcoming empirical data from these measurements will hopefully lead to a theoretical model of leakage current in flat-flex circuit boards.

Furthermore, studies to understand the "Burned" board effect should be performed using the new AP-HT and HT-HT type panels. Direct comparisons to AP-LF or LF-LF type panels could reveal whether the glass-transition temperature (T_g) of the adhesive relates to the activation temperature for burn.

No Coverlay

Panels without a coverlay were manufactured at Cirexx using both LF and AP substrates. These were used to directly measure the effect of adding an adhesive between the copper and polyimide film used as the substrate. Preliminary results clearly show that the presence of an adhesive changes the measured R_I by orders of magnitude. AP boards with no coverlay had an R_I value that was beyond measurement using a 12V bias. Parts made on an LF board with adhesive show typical temperature-dependent R_I properties, as seen for every part with an LF coverlay. This topic will be discussed in a separate report.

APPENDIX A: TRACE AND SPACE PLOTS

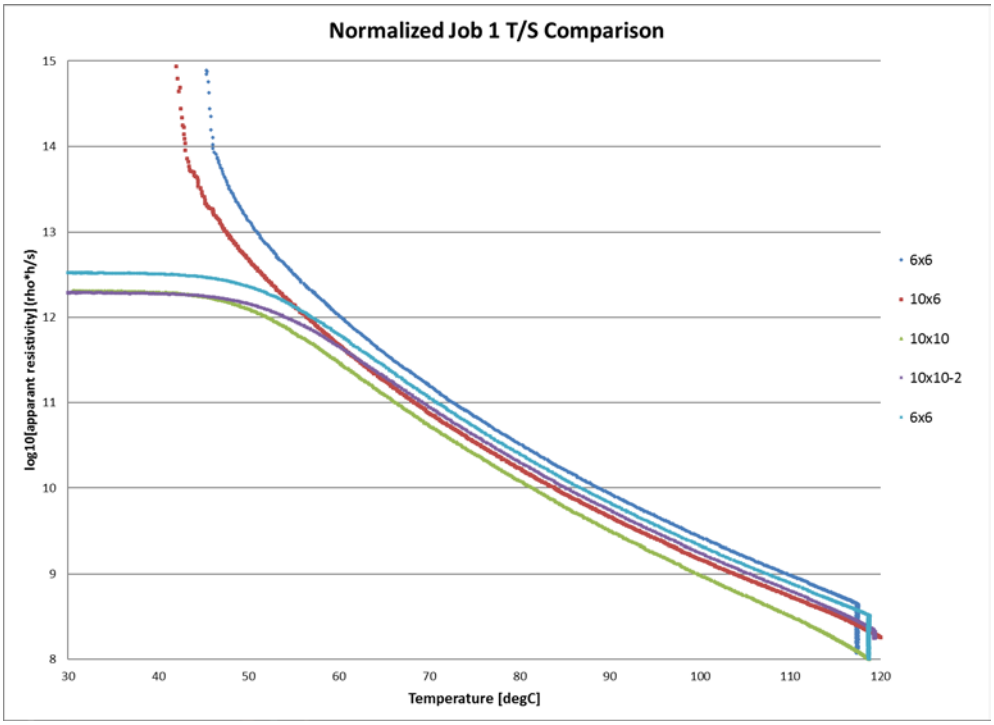

Figure A-1. T/S Comparisons between test specimens of Type 1

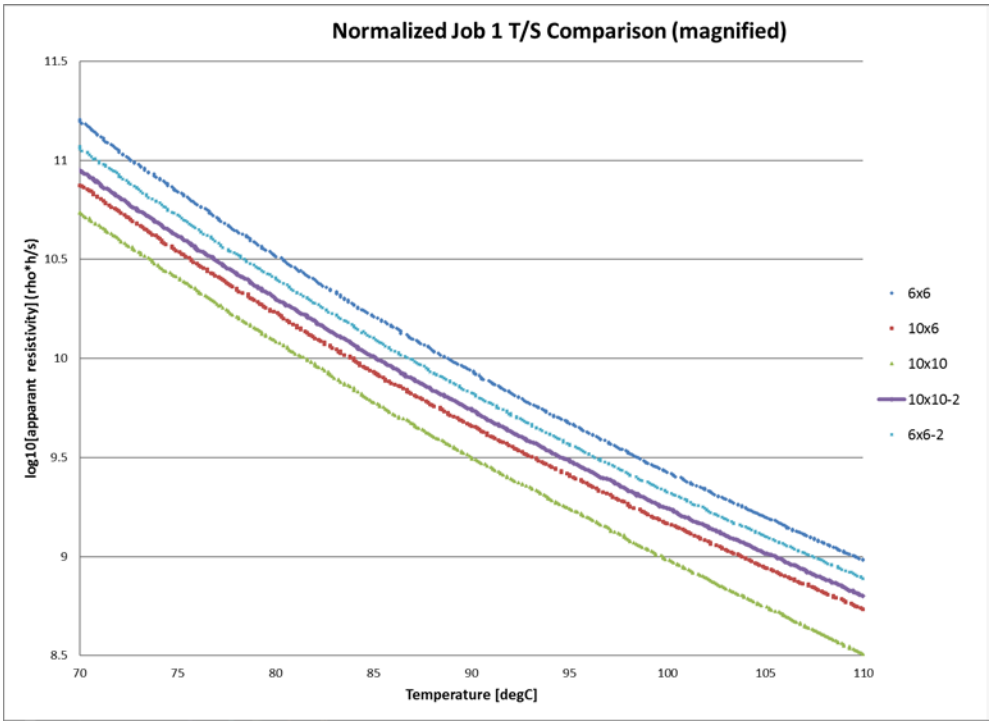

Figure A-2. A magnified version of Figure A-1 to better distinguish between curves. This plot shows T/S comparisons that are quite far from expectations.

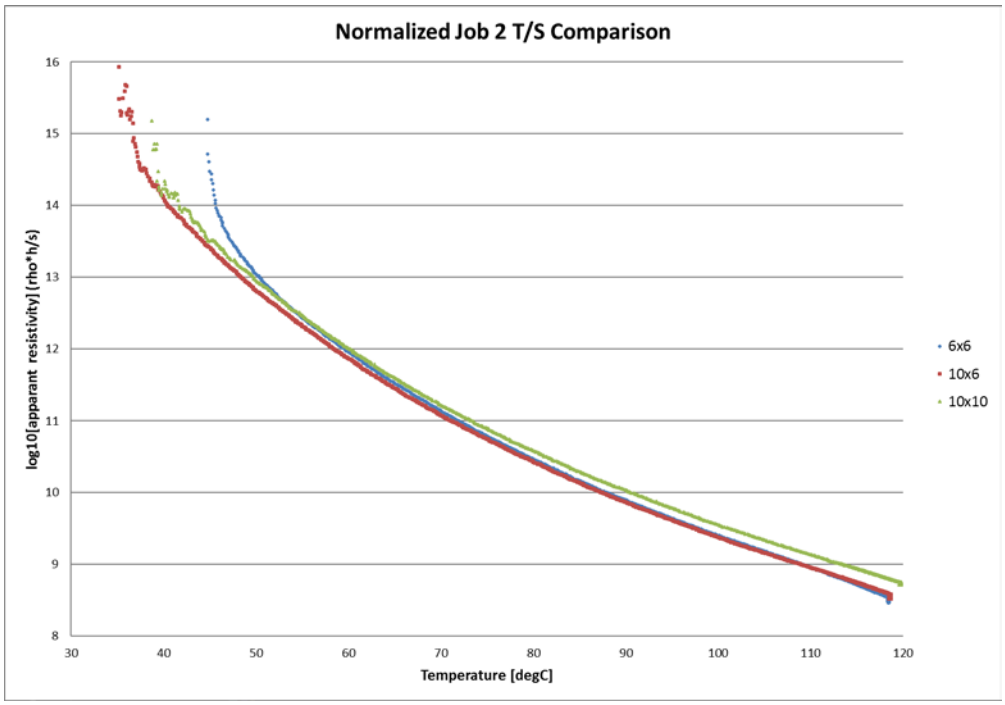

Figure A-3. T/S comparisons between test specimens of Type 2

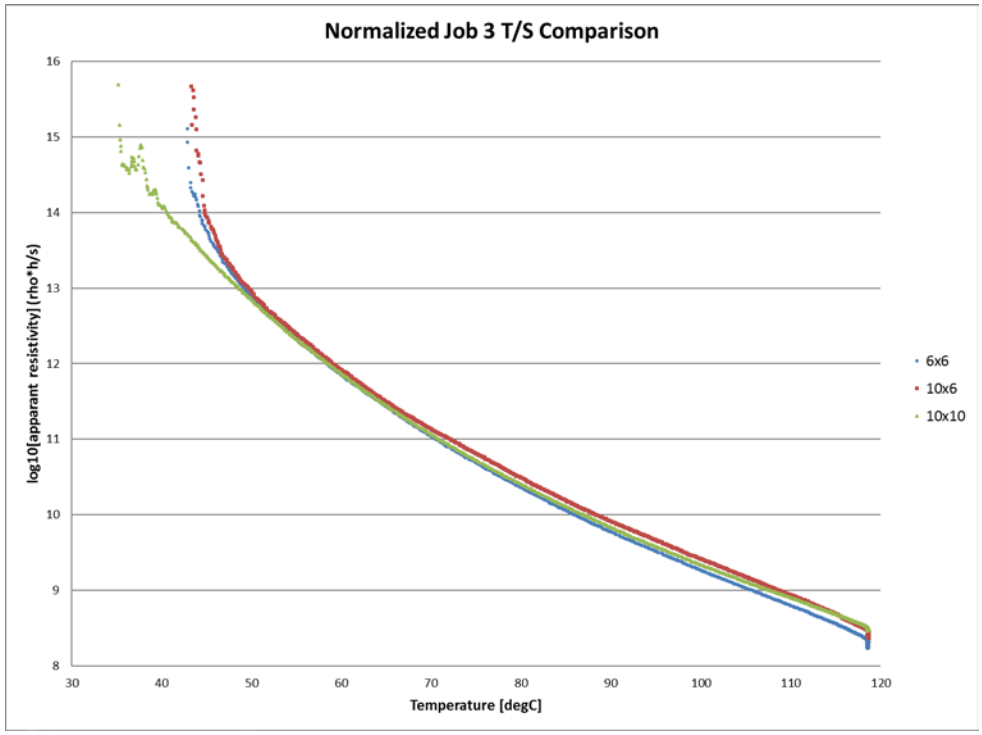

Figure A-4. T/S comparisons between test specimens of Type 3

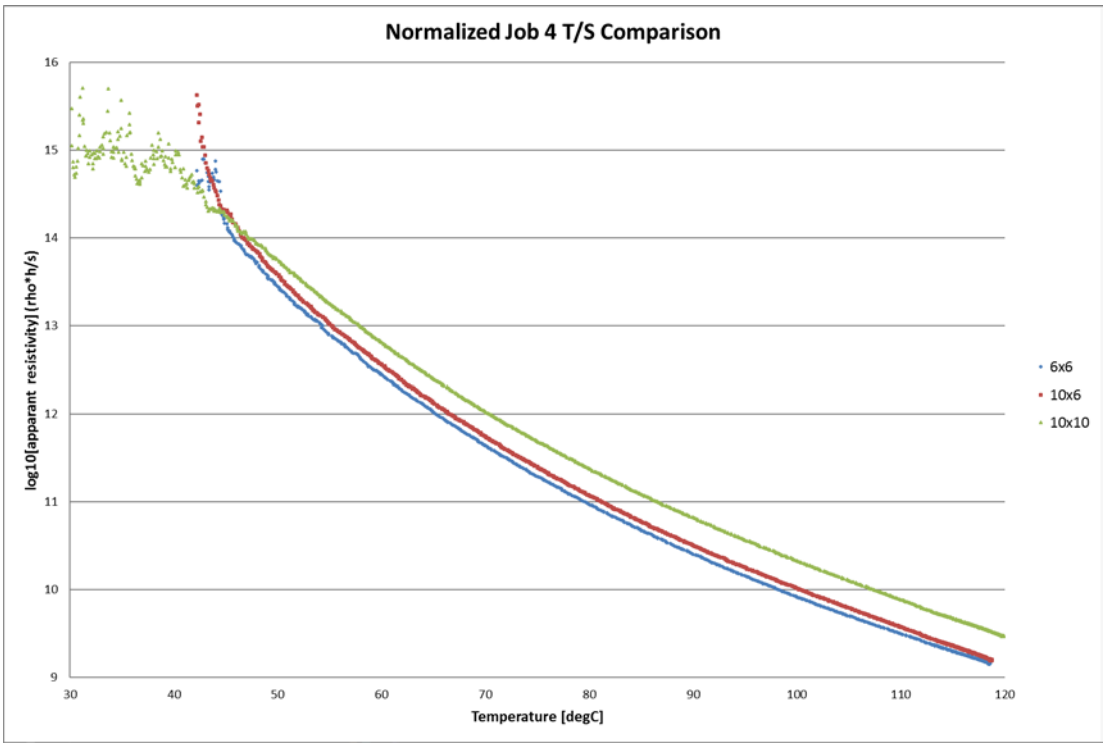

Figure A-5. T/S comparisons between test specimens of Type 4

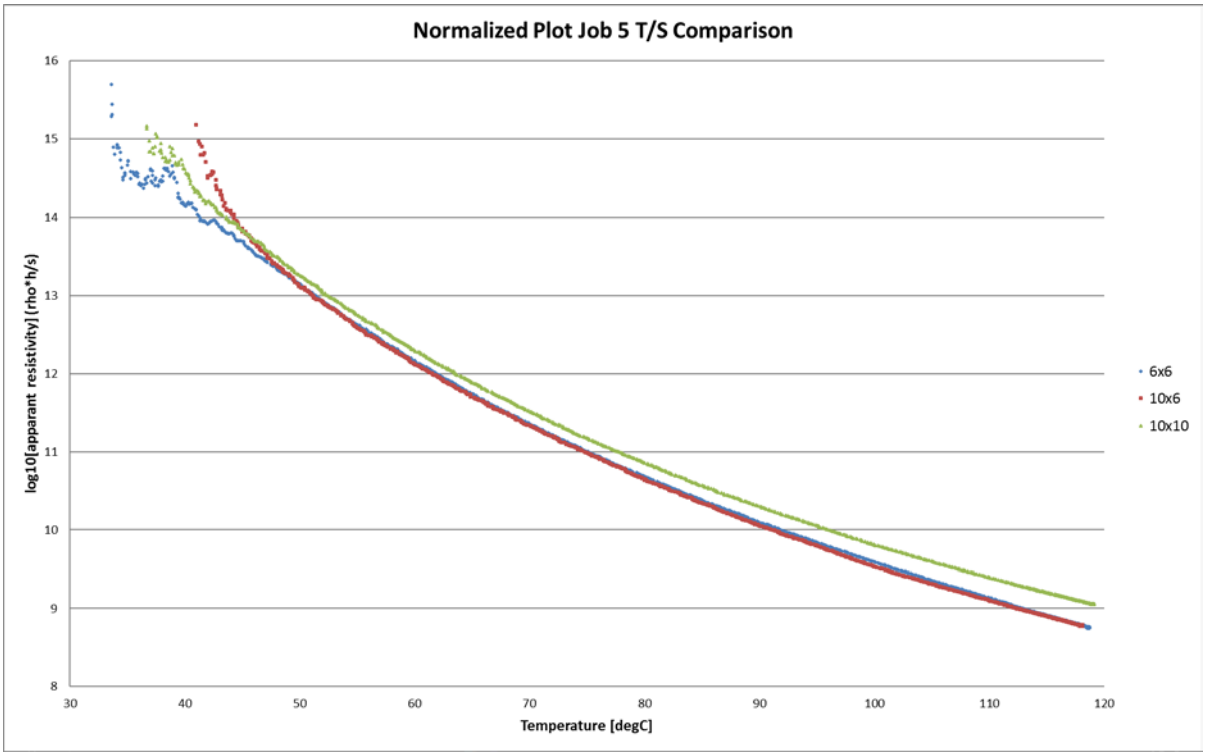

Figure A-6. T/S comparisons between test specimens of Type 5

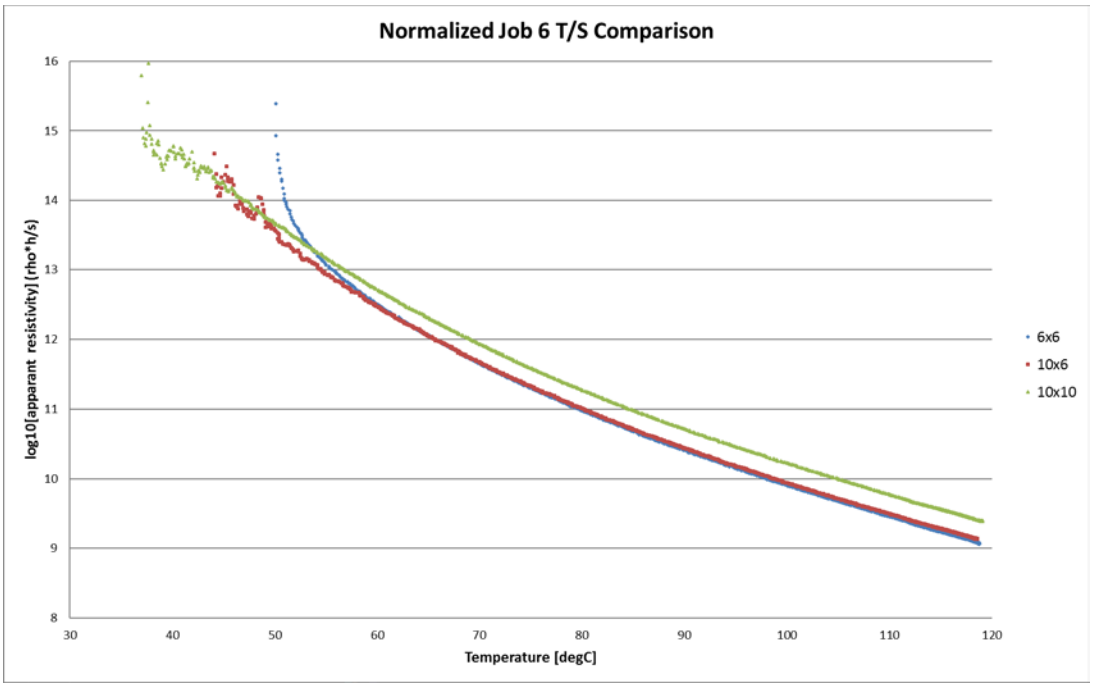

Figure A-7. T/S comparisons of test specimens of Type 6

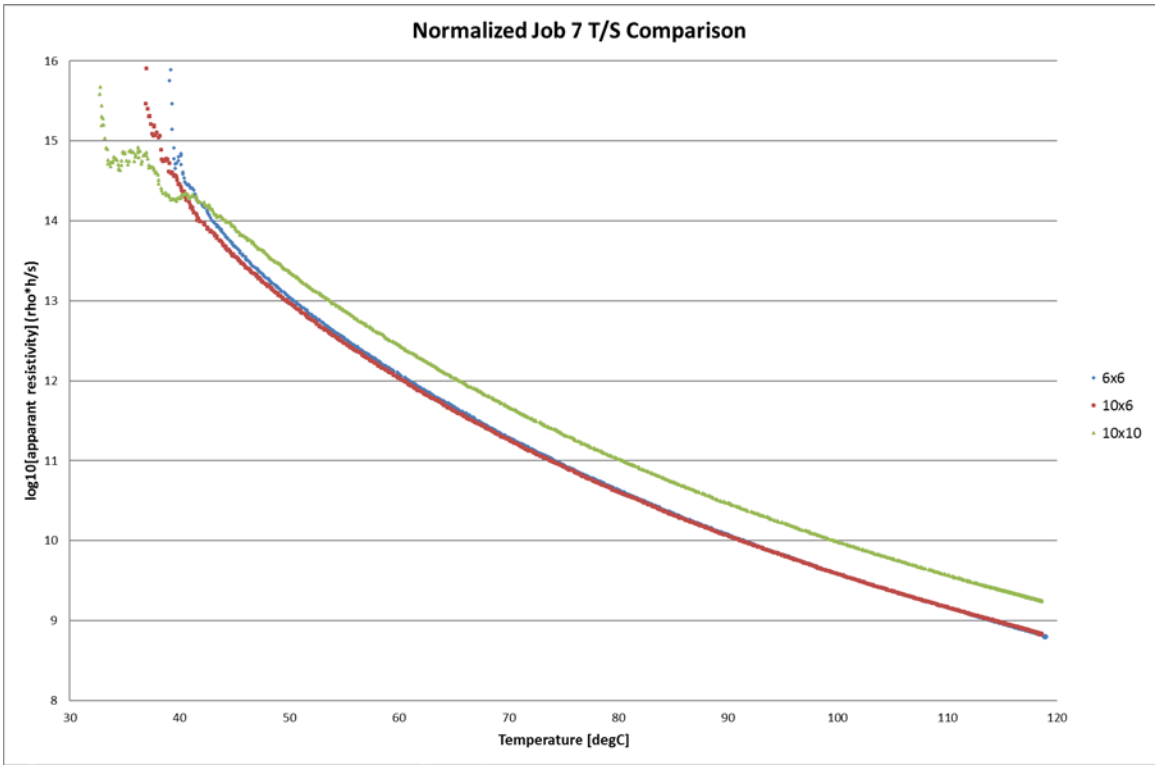

Figure A-8. T/S comparisons of test specimens of Type 7

APPENDIX B: COPPER WEIGHT PLOTS

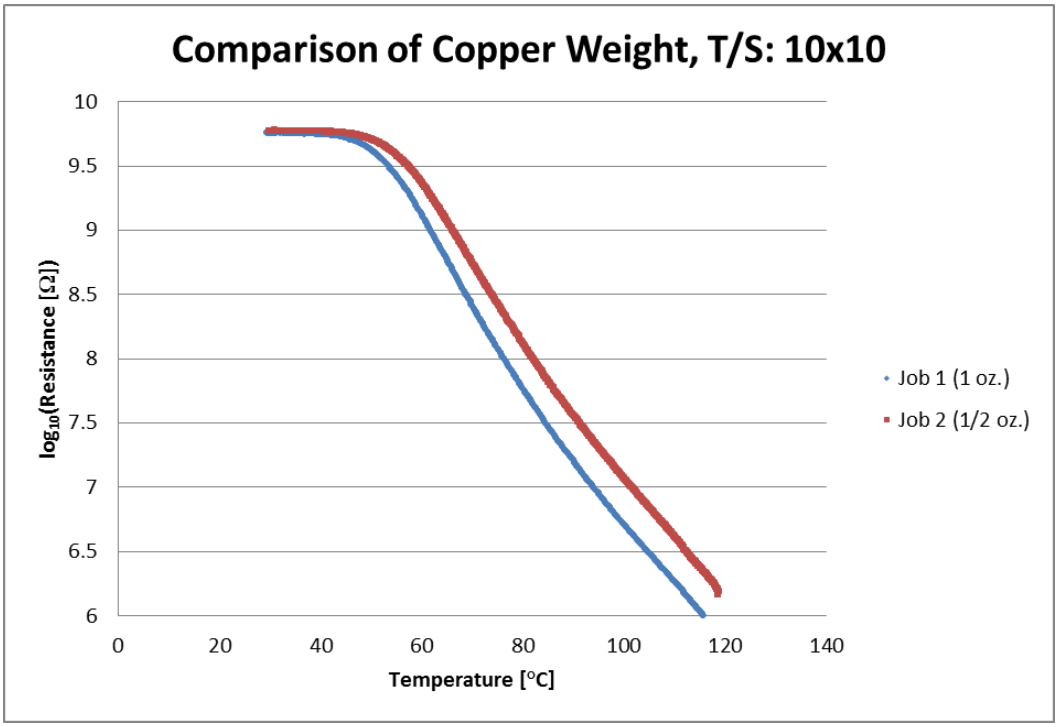

Figure B-1. Comparison of copper weights on two LF boards of T/S 10/10

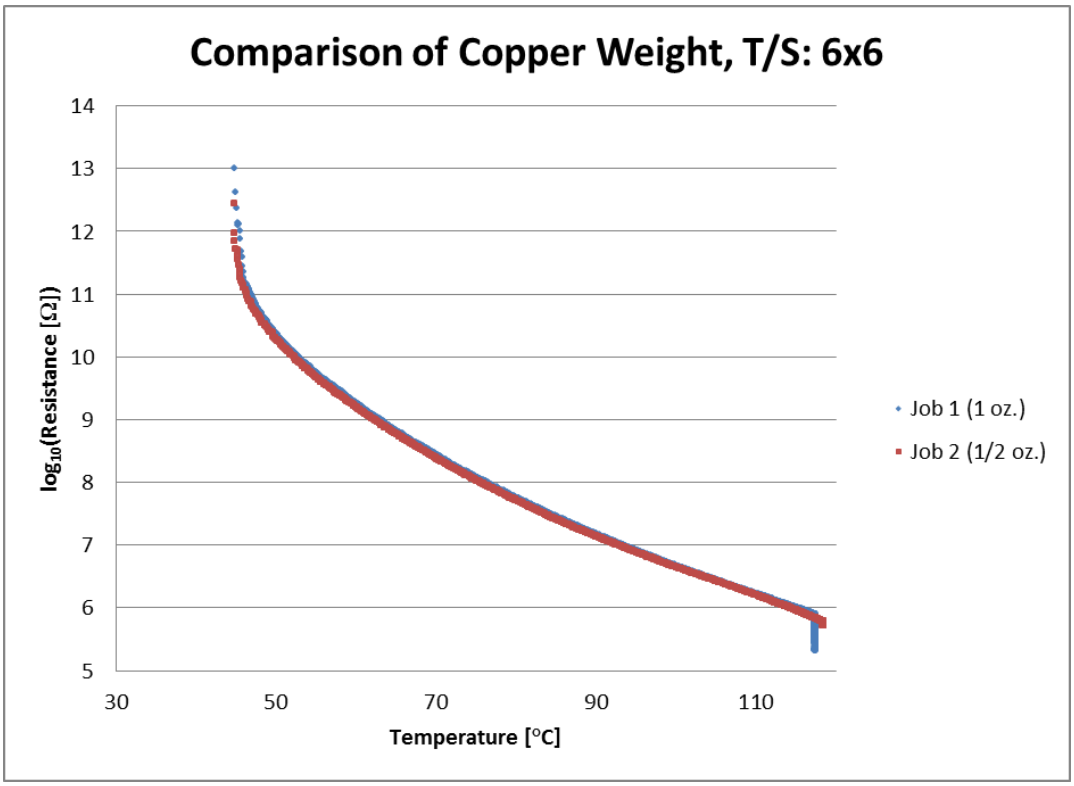

Figure B-2. Comparison of copper weights on two LF boards of T/S 6/6

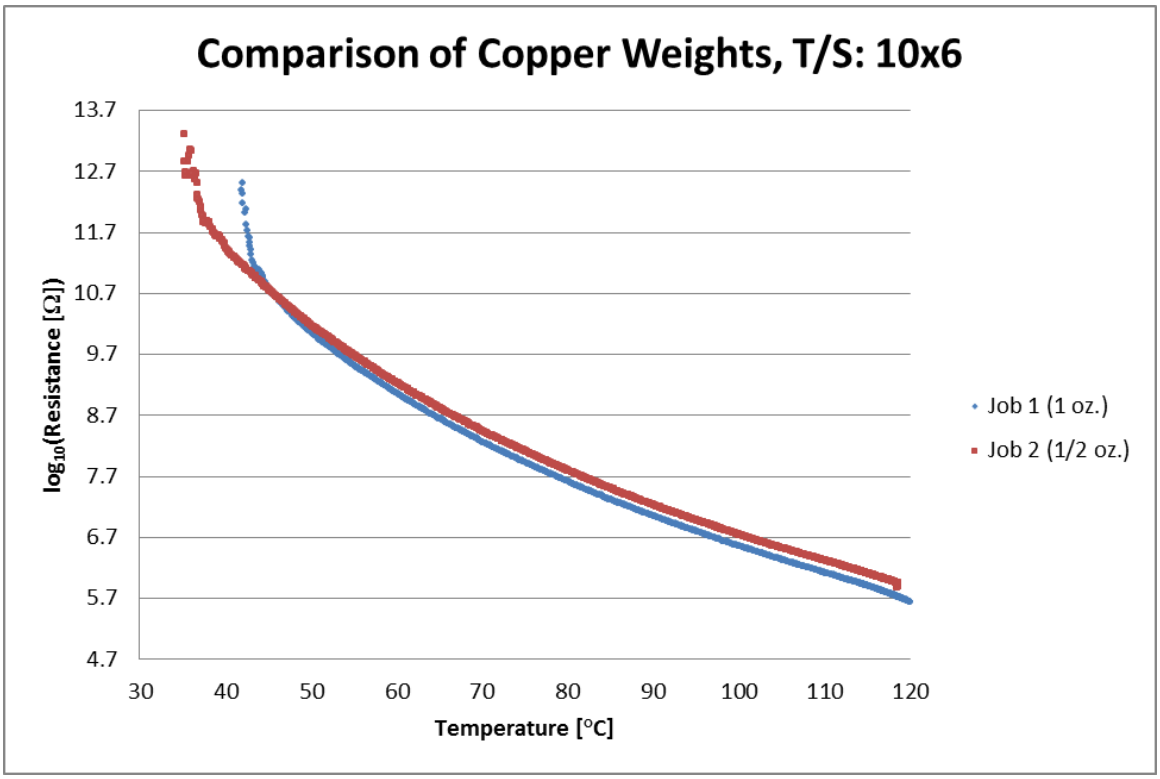

Figure B-3. Comparison of copper weights on two LF boards of T/S 10/6

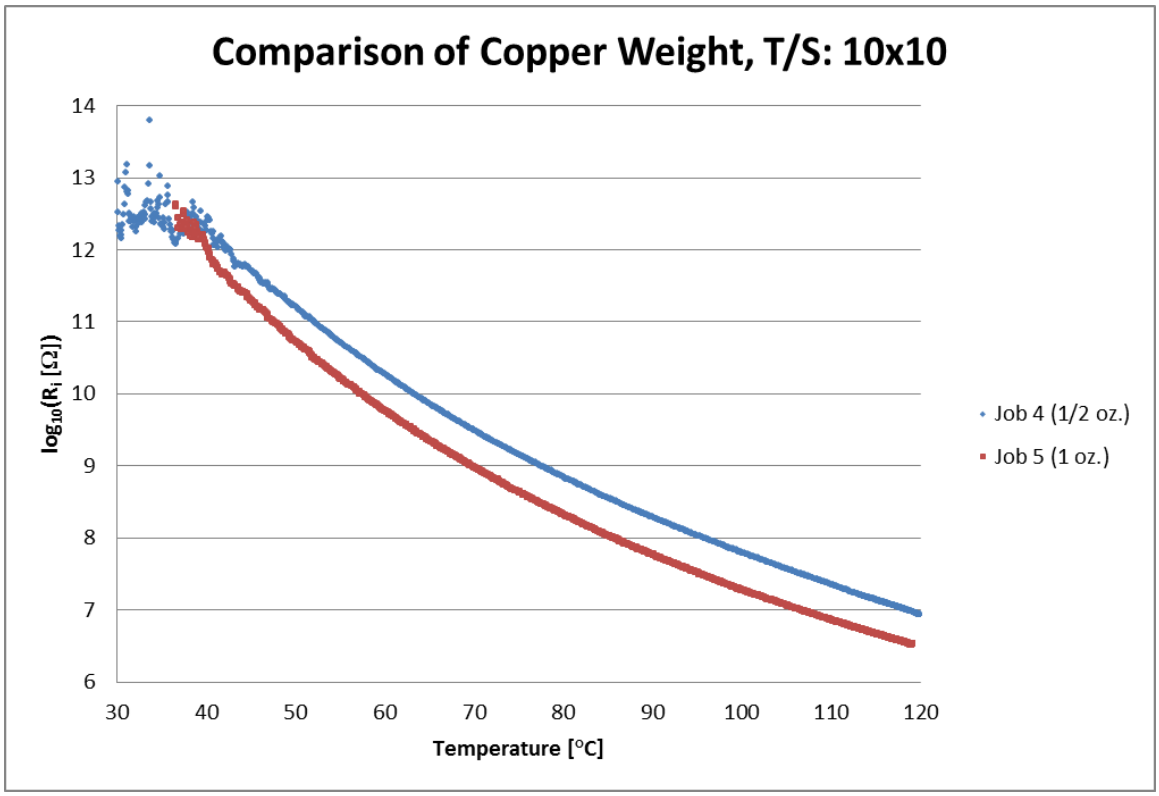

Figure B-4. Comparison of copper weights on two AP boards of T/S 10/10

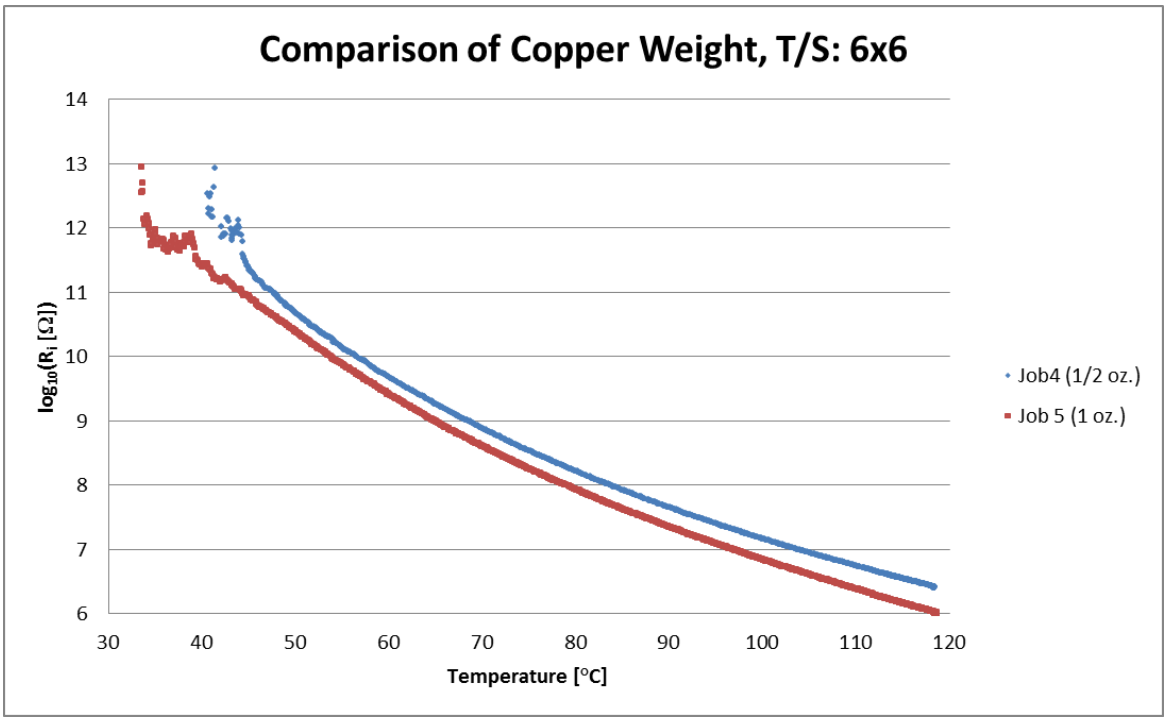

Figure B-5. Comparison of copper weights on two AP boards of T/S 6/6

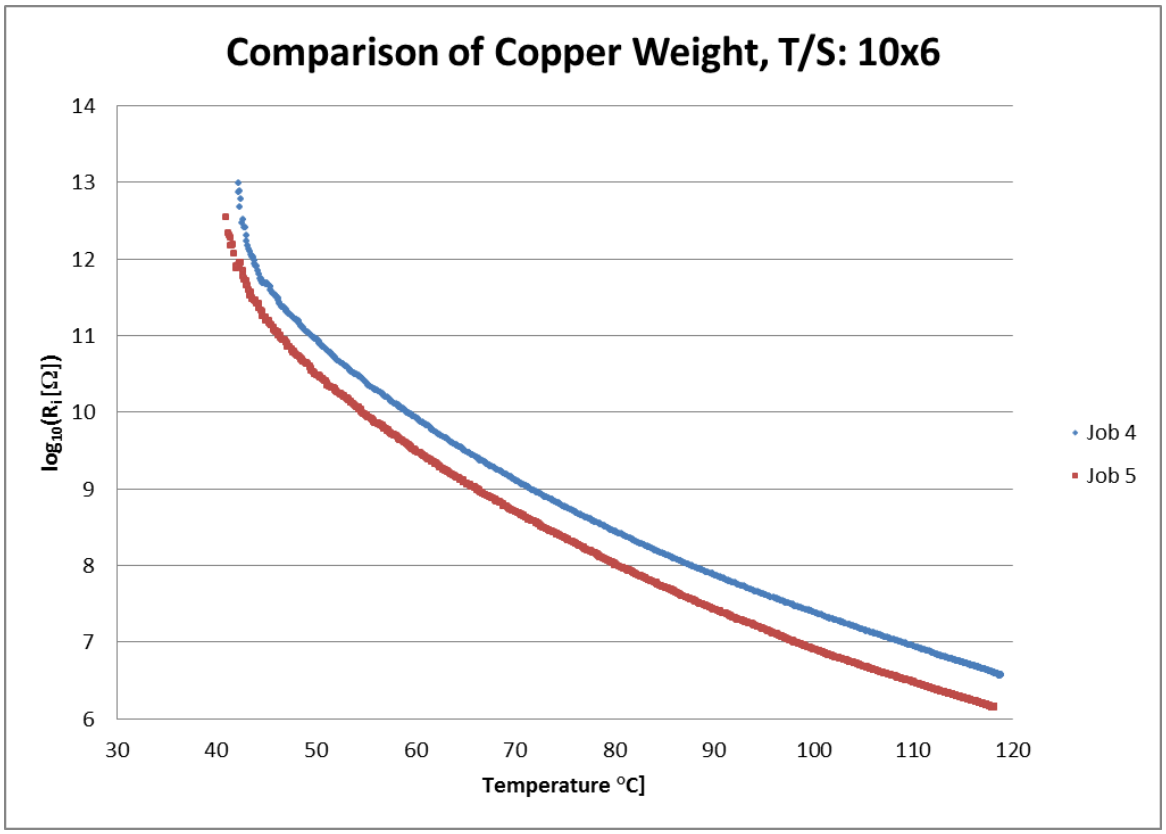

Figure B-6. Comparison of copper weights on two AP boards of T/S 10/6

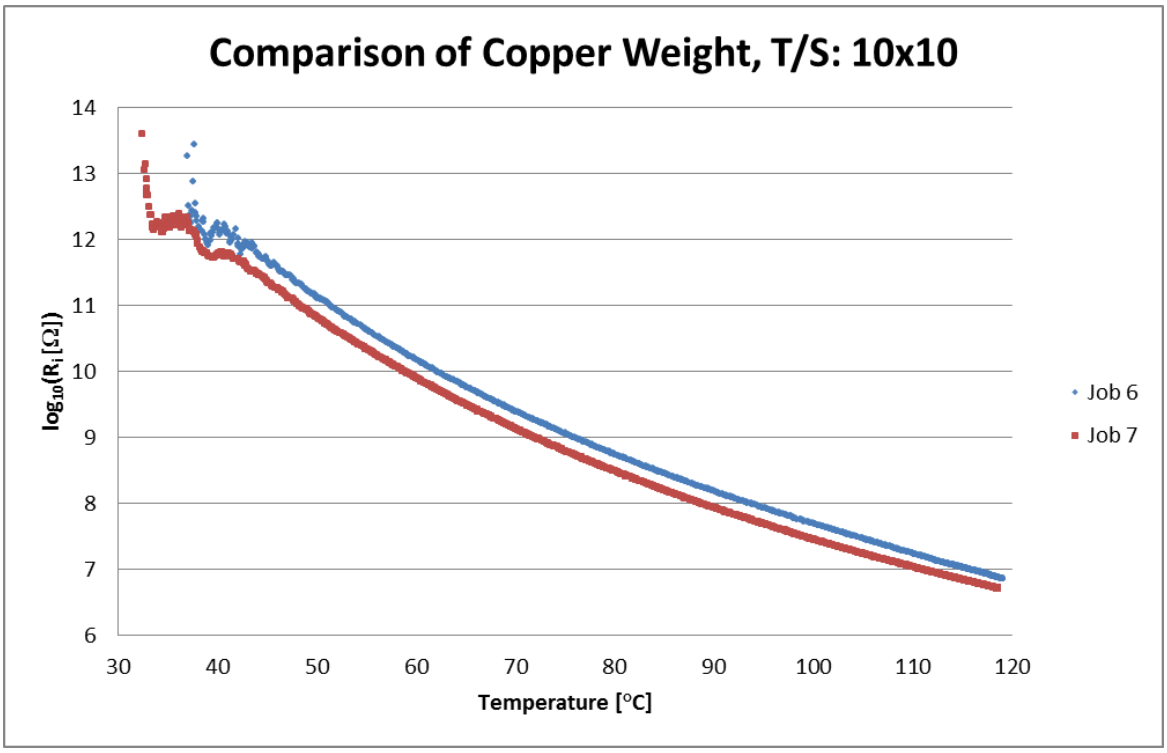

Figure B-7. Comparison of copper weights on two AP boards of T/S 10/10 (Board types 6 and 7 have a thicker substrate than do board types 4 and 5)

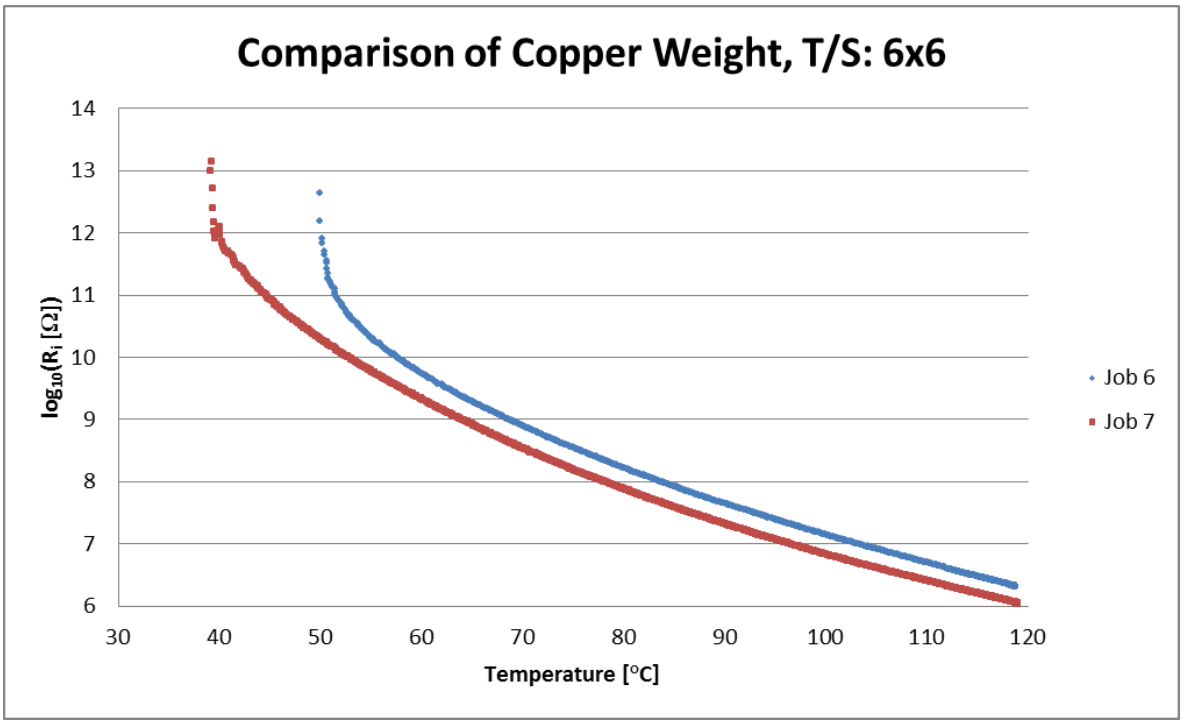

Figure B-8. Comparison of copper weights on two AP boards of T/S 6/6

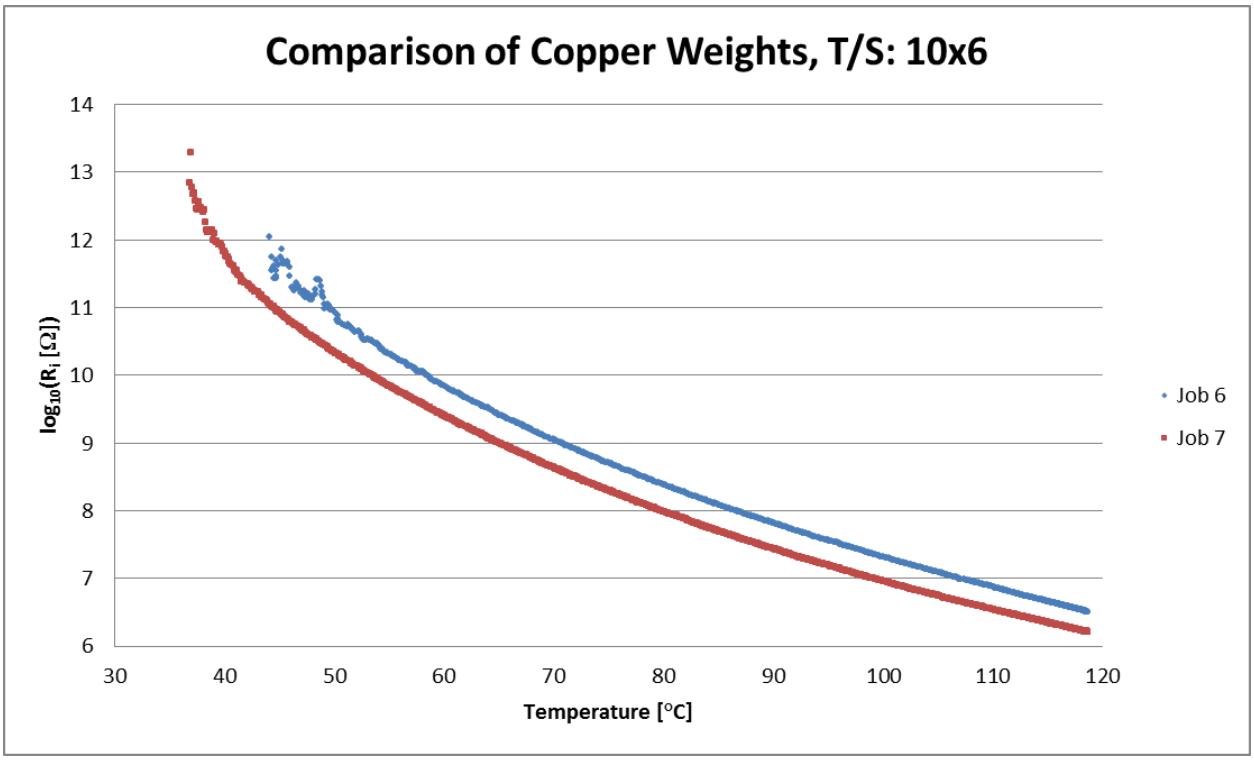

Figure B-9. Comparison of copper weights on two AP boards of T/S 10/6

APPENDIX C: SUBSTRATE THICKNESS PLOTS

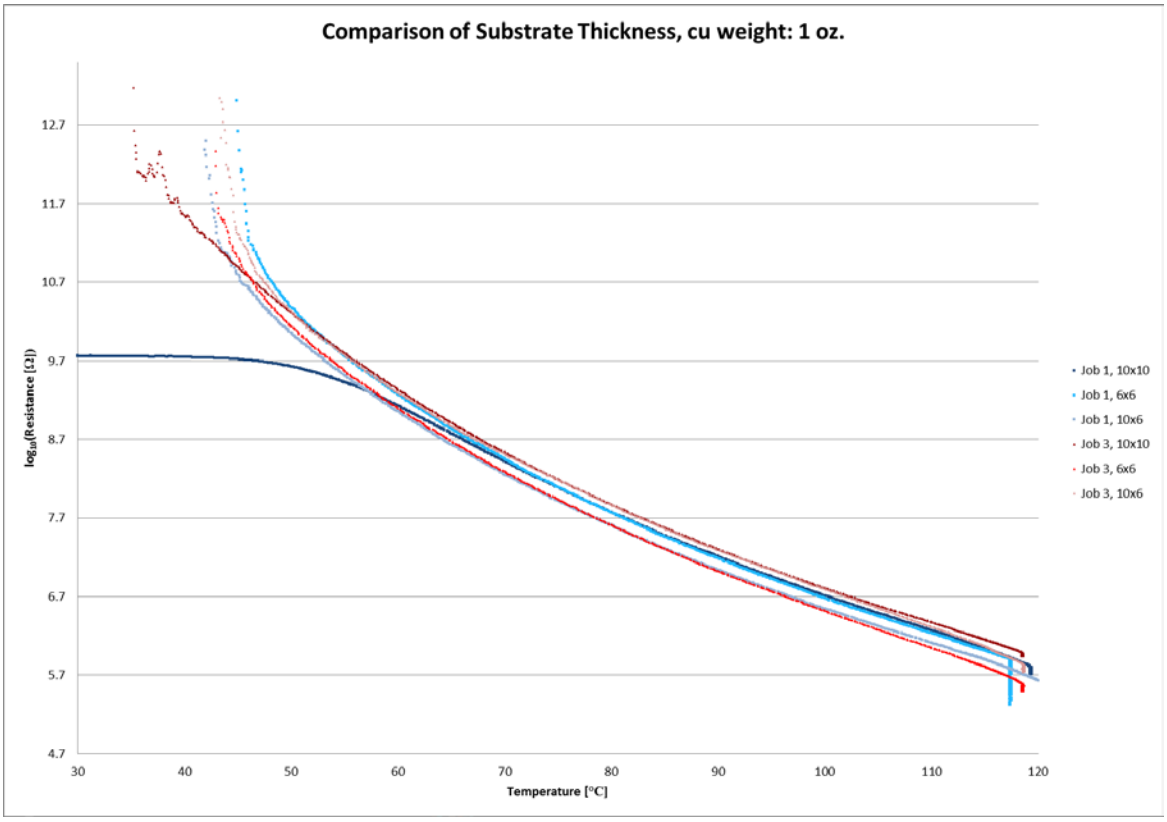

Figure C-1. Comparison between substrates of 2 Mil thickness (Job 1) and 3 Mil thickness (Job 3) (magnified below)

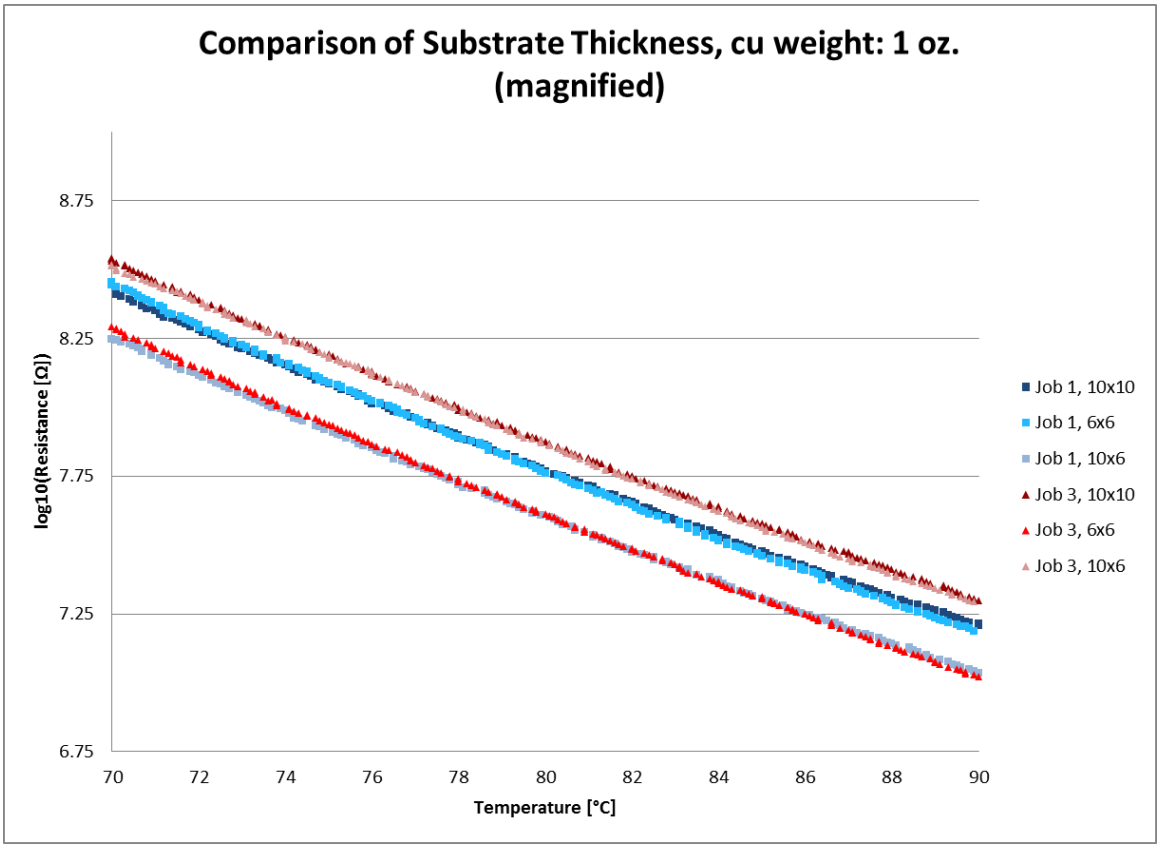

Figure C-2. A magnified version of Figure C-1. The thickness of the Job 1 and Job 3 substrates are 2 Mil and 3 Mil, respectively. Job 3 6x6 and Job 1 10x6 do not match expectations.

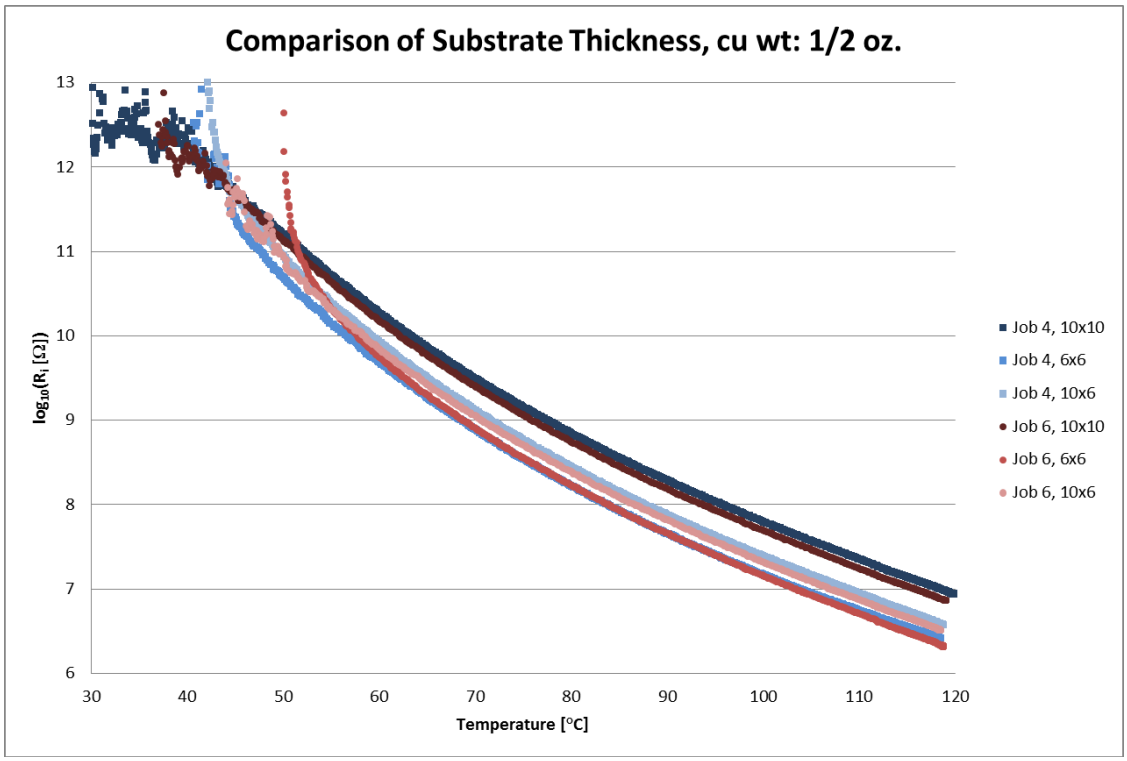

Figure C-3. The thinner substrate specimen of 4 Mil (Job 4, blue curves) shows a higher insulation resistance than do comparable specimens of thicker substrates of 5 Mil (Job 6, red curves). This finding does not match expectations.

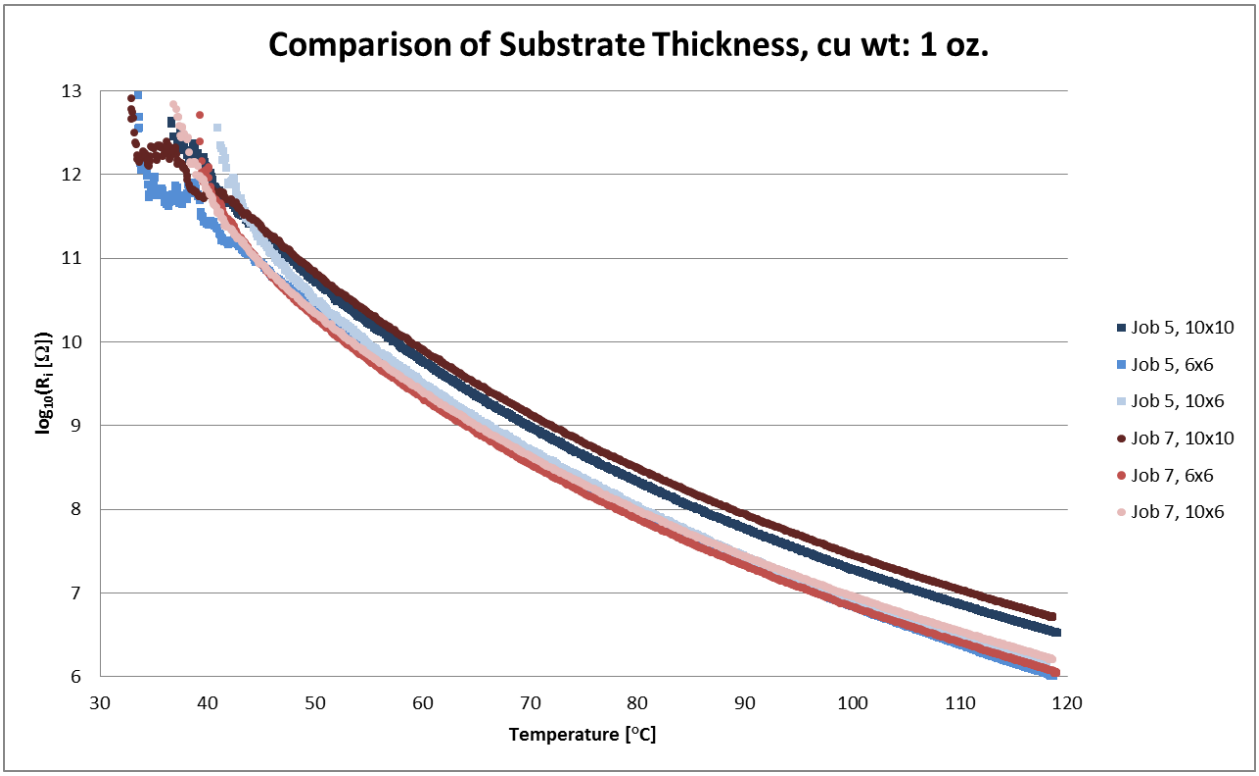

Figure C-4. The thicker substrate specimen of 5 Mil (Job 7, red curves) has a higher insulation resistance than do the comparable specimens of thinner substrates of 4 Mil (Job 5, blue curves). This finding is opposite of that of Figure C-3. The only difference in these two groups of specimens is the copper weight.

APPENDIX D: SUBSTRATE TYPE PLOTS

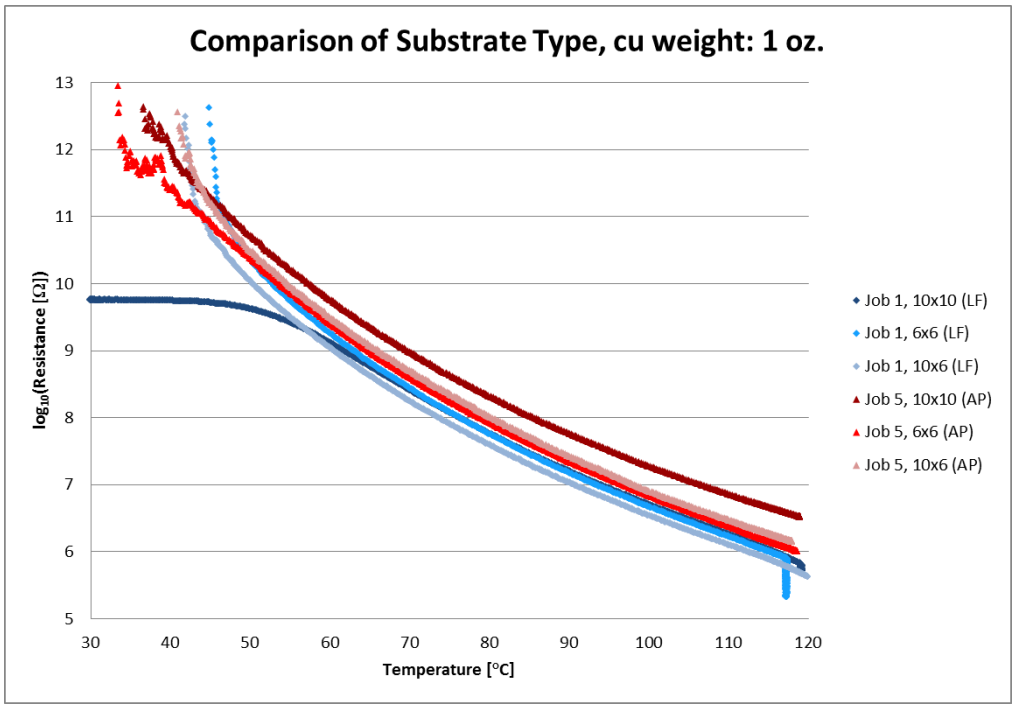

Figure D-1.The LF substrates have a lower R_I than do the AP substrates for specimens having a copper weight of 1 oz.

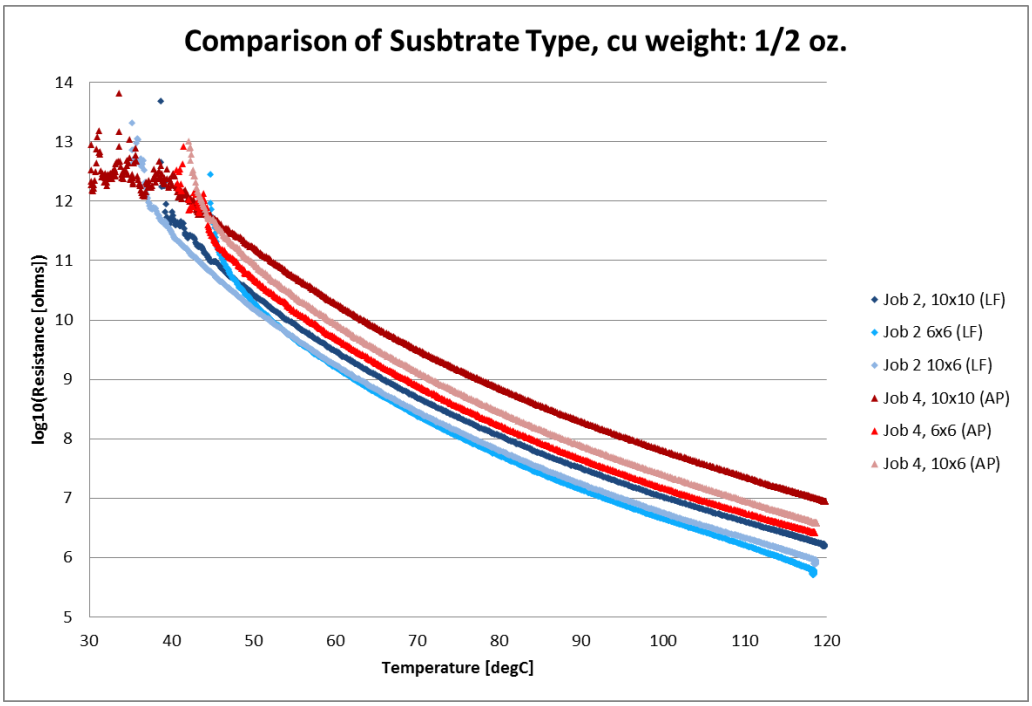

Figure D-2. The LF substrates have lower R_I than do the AP substrates for specimens having a copper weight of ½ oz.

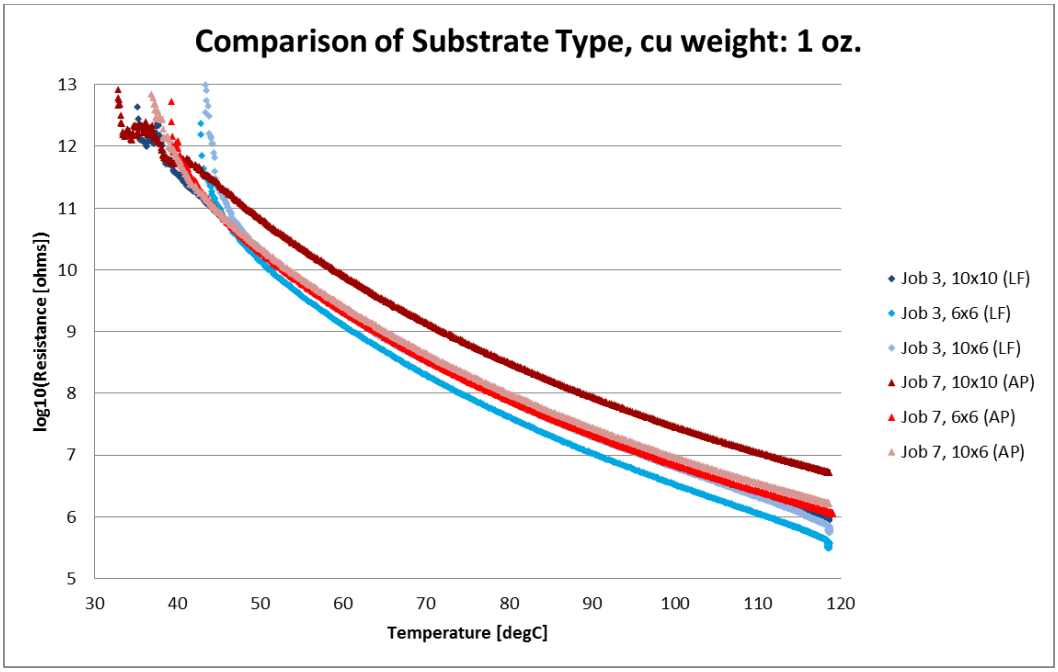

Figure D-3. In this data set, specimens with an LF substrate prove to have a lower R_I than do specimens with an AP substrate.

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