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Thermal Testing Quality Assurance of 24LCC & 3LCC Electronic Packages

Graduate Project

The University of New Mexico
Department of Mechanical Engineering

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Introduction

The purpose of this project is to experimentally validate the thermal fatigue life of solder interconnects for a variety of surface mount electronic packages. Over the years, there has been a significant amount of research and analysis in the fracture of solder joints on printed circuit boards. Solder is important in the mechanical and electronic functionality of the component. It is important throughout the life of the product that the solder remains crack and fracture free. The specific type of solder used in this experiment is a 63Sn37Pb eutectic alloy. Each package was manufactured with conformal coating along with and without an underfill material below the device.

Conformal coating helps protect the board from environments such as electrostatic discharge and humidity. It is commonly used in broad types of engineering disciplines such as commercial, military, research and development, etc. Conformal coating can also pose a risk for the life of the board because of its high thermal expansion coefficient. This can greatly decrease the life of the product if it regularly sees high temperature variations. This leads to a shorter fatigue life of the solder. The fatigue life is a common mechanical problem in the field of electronic devices. Adding underfill can help increase the fatigue life of the solder. However, applying underfill adds time to manufacturing and production. This ultimately increases the cost per unit. The study of conformal coated printed circuit boards with and without underfill was done on two different surface mount electronic packages.

The electronic packages studied were 24 and 3 contact Leadless Ceramic Chips packages. When the package was not underfilled, the coating was allowed to flow underneath. The assembly was analyzed and tested to obtain the best available combination of conformal coating, underfill, and potting to design the most robust and reliable circuit board while keeping in mind certain factors such as cost, manufacturing time, and need. Different types of conformal coatings were considered with and without underfill for each device. 29 of each component were manufactured to have a large sample size and for the sake of individual defects and imperfections.

Finite Element Analysis (FEA) was performed by an engineer at Sandia National Laboratories for both Leadless Ceramic Chips. From the FEA results, a test acceleration profile was derived and the number of temperature cycles to fail the solder interconnects were found for three different cases. Experimentation was done as a secondary measure to validate this data to show confidence in the theoretical analysis.

Accelerated testing functions as a quality check for the product. Accelerated testing is extremely useful in the research and development phase of engineering. It can save money from the potential of early life defects and the costs that come along with warranties. Accelerated

testing makes a weaker design more robust and checks the reliability of a strong design in a shorter period of time. It is extremely helpful in a world where deliverables are in high demand and scheduling is tight. Accelerated testing helps the engineer gain an understanding of what needs to be improved and what works well. There are many different types of accelerated tests. Our circuit boards were accelerated inside a closed thermal chamber because of the high number of use cycles.

The ultimate goal of this experimentation is to help identify what will prevent any premature cracking or fracturing in the solder alloy. It is important to understand that underfilling each component may or may not be needed. If underfill is not needed, there are several production benefits.

Surface Mount Technology

There are many different kinds of electronic packages that do not require the use of through holes in a circuit board. Surface Mount Technology (SMT) started to become widely used in the 1980's [30]. SMTs have many different forms. Examples are microprocessors, transistors, and capacitors. Quad Flat No-lead (QFN), Ball Grid Arrays (BGA), and Leadless Ceramic Chips (LCC) are all of the semiconductor family. All of these have their own advantages and disadvantages in various applications. They also vary in size as well as the number of contacts. These various devices were all considered for testing. Adding these components into the design of regular PCBs greatly reduces the manufacturing cost. Pick and place techniques for these devices also helps to simplify the manufacturing process.

Since we are in between preliminary research and manufacturing it was decided to go ahead and underfill the larger components (56LCCs and BGAs) and not to test. These components have larger surface areas and more contacts, increasing the probability of failure. The electronic packages that were focused on for thermal testing were the LCCs.

1.1 Leadless Ceramic Chips

There are a few advantages to using an LCC. They typically have a low number of joints, are rugged, have low inductance, and are affordable [10]. The performance of an LCC is adequate compared to its competitors. LCC's can be susceptible to potentially large temperature differences. The change in temperature can lead to cracks and even fractures in the solder joint.

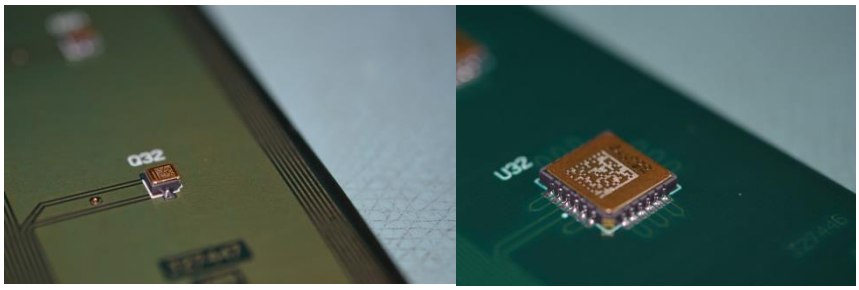

Figure 1. 3LCC and 24LCC test units

The chip carrier packages used in this experiment have 24 and 3 solder interconnects. Like the QFN, the LCC device has its solder contacts around the perimeter. The bottom surface has an area of 0.1225 in^2 and 0.012 in^2 for the 24 contact and 3 contact packages respectively.

1.2 Materials

There can be many different materials that make up electronic package assemblies such as underfills and coatings. The package protects the semiconductor from a variety of different environments that the circuit board is exposed to during assembly, shipping and handling, and operations of the device. However a package can cause thermal mismatches due to the different materials that come into close contact with one another. Due to the difference in thermal properties, the life of the solder can be drastically reduced if no underfill is used.

Conformal coatings protect the electronic components on a circuit board from environmental and mechanical interactions such as moisture, humidity, particulates, corrosion, as well as electrostatic discharge and vibration. Coating can be fairly simple to apply onto a Printed Circuit Board (PCB). Before coating the board, the surface and all components should be clean and free from all particulates and foreign object debris (FOD). Coatings can be dipped, sprayed, or spread onto a board. Uvikote 7503 and Arathane 5750 were both considered as the two types of coatings studied. Arathane is Military Specification (Mil spec) approved and will cure within 7 days at 20°C. It is translucent in appearance and is made up of a two part polyurethane compound [2]. Uvikote 7503 is also a translucent, Mil Spec approved coating, which is made up of two components [1]. When exposed to ultraviolet (UV) light, Uvikote is able to cure to the electronics assembly. At 23°C, Uvikote can be post cured in 14 days.

During the manufacturing phase, it was determined that only Arathane would be tested for several different reasons. The first, most significant reason for not testing Uvikote was due to time and schedule constraints. One vendor was not able to deliver the material 4 to 6 weeks before the deadline. The other vendor did not have the UV light capability it takes to cure Uvikote. This leads to a broader perspective to consider in that not all manufacturers would have this capability. It can also take a considerable amount of time to cure Uvikote, even up to 2 weeks to do so. Long curing times would offset testing time and could ultimately delay the

project deadline. A positive reason for only testing for Arathane coating is the limited number of units under test (UUTs). Only 29 of each package were manufactured for testing. This allowed for testing a larger number of samples for one study.

Every device was experimentally tested in conformal coating. Nine of each package type were underfilled. Underfill serves a quality purpose for protecting the solder joints from shock, vibration and various thermal environments. If the product undergoes these various stresses, underfilling can increase the reliability, and extend the life of the component. For underfill to be applied, it is usually dispensed along the edge of the package in a straight line with a syringe like tool. It then spreads under the rest of the unit. Underfill covers the top surface of the PCB and the bottom surface of the chip. Depending on the type, it can take between 5 minutes and 1.5 hours to cure [27]. Underfill makes the product more rigid, and is very effective in mitigating coefficient of thermal expansion (CTE) mismatching [31]. For the underfilled boards in these environmental tests, Almatis 20% was used. The mechanical properties of the underfill material can change as the temperature goes towards the glass transition temperature of 80°C. Table 1 shows the mechanical properties of Uvikote, Arathane, and Almatis 20%.

Material	**Young's Modulus (MPa)**	**Poisson's Ratio**	**Thermal Expansion Coefficient ($1/^{o}C$)**	**Glass Transition Temperature (°C)**
Arathane 5750 Conformal Coat	8.80	0.499267	190.0×10^{-6}	-70
Uvikote 7503 Conformal Coat	28.0	0.497667	222.0×10^{-6}	-55
Almatis 20% Fill Underfill	5,443	0.3684	40.60×10^{-6}	80

Table 1. Coating and Underfill Mechanical Properties [6]

Solder joints provide mechanical connection and electrical conduction by making contact from the electronic package to the substrate. It has a low melting point, is affordable, and is favorable for contact onto metallic surfaces [12]. There are many different varieties of solder alloys today. Tin lead solder alloys are extremely common and are offered in a variety of compositions. Figure 2 is the phase diagram of tin lead solder alloys.

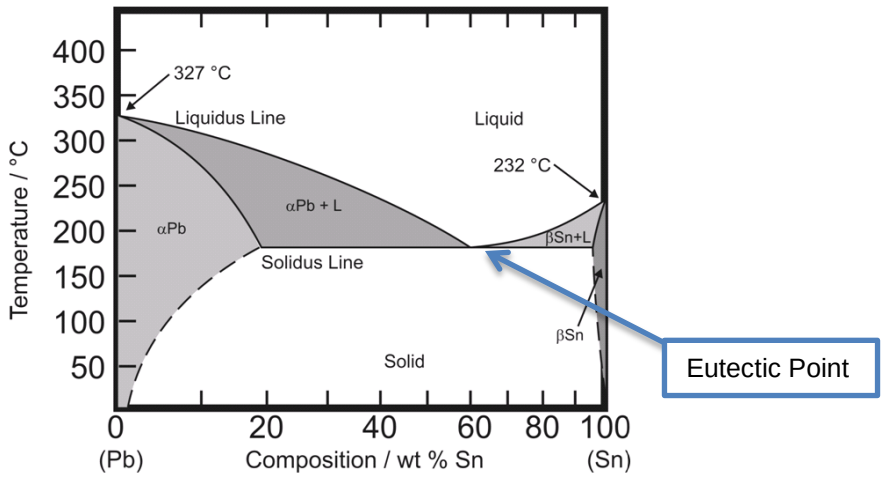

Figure 2. Phase diagram for Tin-Lead solder alloys [39]

63Sn37Pb solder was used in this research. This is considered a eutectic alloy. The point where it has a direct transition from solid to liquid without any α phase or β phase material is shown on the on the phase diagram above. There has been a considerable amount of research on the mechanical characterization of Tin-Lead solder. Thermal stress is one of the main reasons why solder fails. The amount of strain the solder interconnects experience varies on the location and geometry. It is treated as a very ductile material, and is assumed to be isotropic. The alloy's material properties vary significantly as the temperature ranges from -60 to 100°C. The mechanical properties of 63Sn37Pb at different temperatures are shown in Table 2.

Temperature (^{o}C)	-60.0	21.0	100.0
Young's Modulus (MPa)	48,276	43,255	36,860
Poisson's Ratio	0.38	0.39	0.40
Thermal Expansion Coefficient(1/^{o}C)	25.0×10^{-6}		
Melting Temperature (°C)	183		

Table 2. 63Sn37Pb Solder Mechanical Properties [6]

It is important to note that there are different standards and specifications that are undergone when soldering. Sandia follows a requirement for soldering from aerospace and medical applications based on the standard defined by IPC-JSTD-001F [34]. Soldering is based on class 3, high performance, and harsh environment electronic products. This class is more demanding than the other three, and states equipment will have little to no down time, and must function properly when the device is operational.

Polyimide was chosen for both PCB tested in these experiments. Along with FR-4, Polyimide is an extremely popular choice for the PCB material. The different Modulii, CTEs, and Poisson's ratios are showed in table 3. These material constants for underfill, coating,

63Sn37Pb solder, and polyimide were necessary in determining the FEA results that were performed.

Material	Arlon 85N
Young's Modulus XX, ZZ (MPa)	22,069
Young's Modulus YY (MPa)	5,517
Poisson's Ratio YX	0.0234
Poisson's Ratio ZX	0.150
Poisson's Ratio ZY	0.380
Shear Modulus XY (MPa)	5,545
Shear Modulus YZ (MPa)	5,545
Shear Modulus ZX (MPa)	9,593
Thermal Expansion Coefficient XX,ZZ ($1/^oC$)	$17.0x10^{-6}$
Thermal Expansion Coefficient YY ($1/^oC$)	55.0×10^{-6}

Table 3. Polyimide Mechanical Properties [6]

Preliminary Theory

2.1 Thermal Cycling

Almost every engineering design is exposed to a set of temperature differences during its lifetime. These temperature changes can happen in thousands or even millions of cycles. During the high temperature phase the material can experience creep depending on the time of the cycle, temperature extreme and melting point of the material. Through the cycling process the combinations of materials can be stressed from thermal expansion and contraction which can lead to crack appearances leading to fractures as explained later.

For this project the UUT will be exposed to a maximum and minimum temperature and will be held at 20 minute dwell times for each cycle. This leads to a compressive and tensile strain hold for the cold and hot temperatures respectively. An example of this can be shown in Figure 3 [19].

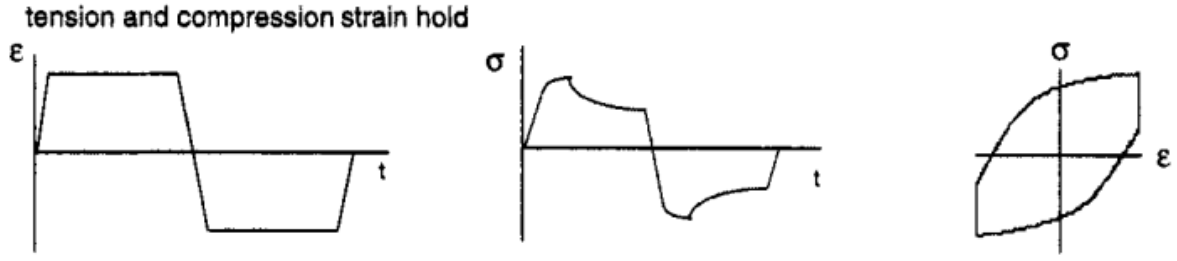

Figure 3. Strain Hold for Thermal Cycling (Remy, 1994)

The strain is held constant over a period of time for both cold and hot temperature cycles. The middle graph shows that as the strain is held to a constant value the stress is then relaxed. When stress is plotted as a function of strain the graph shows the constant strain as the vertical component of the graph.

Because of the difficult constraints and geometries of electronic packaging, FEA is usually performed to show the contour plots of stress and strain for thermal cycling [22]. Without explaining the theory in too much detail, the finite element method derives strain from the node deformation. The stress is in turn computed from the strain by applying Hooke's Law. The equivalent strain and Von Mises stress have been used in the past to quantify the state of the solder [37] from the FEA. The Von Mises stress in terms of the principle stresses is defined as:

$$\sigma_{vm} = \left(\frac{1}{\sqrt{2}}\right) * \sqrt{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}$$

Von Mises stress is of course compared to the yield stress σ_y, in a conservative manner. The equivalent strain is defined in terms of the calculated principle strains as:

$$\epsilon_e = \left(\frac{\sqrt{2}}{3}\right) * \sqrt{(\epsilon_1 - \epsilon_2)^2 + (\epsilon_2 - \epsilon_3)^2 + (\epsilon_3 - \epsilon_1)^2}$$

For this testing, the thermal cycle consisted of temperature extremes of -20 and 70°C. The ramp rates were determined to be 5°C/min, and the dwell time for each temperature extreme was 20 minutes. Figure 4 shows a graphical representation of the thermal cycle profile starting at ambient.

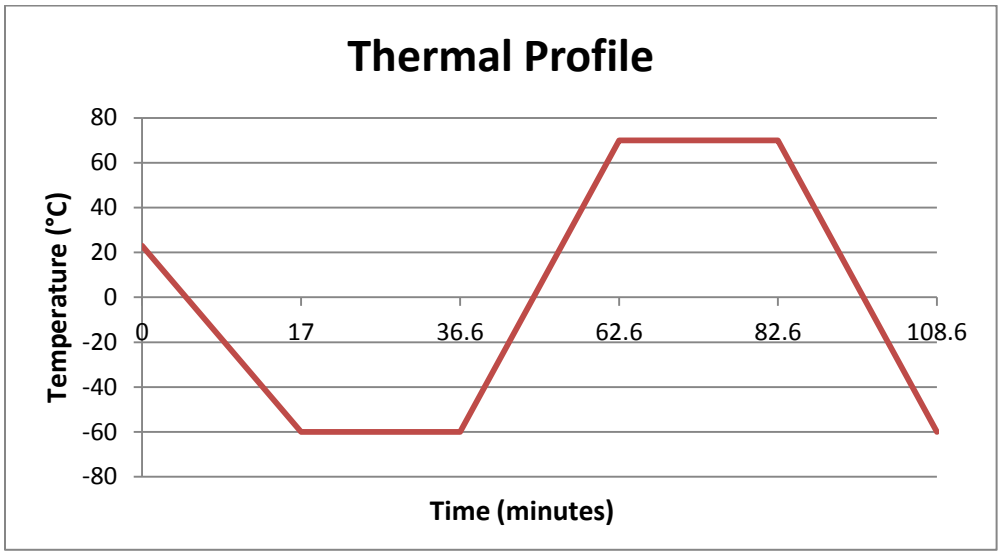

Figure 4. Thermal Cycle Profile

After a certain number of cycles were performed, the UUTs were brought back down to ambient and held there until the user could safely remove them from the thermal chamber. The explanation of how this profile was derived is explained in the accelerated testing section.

2.2 Thermal Expansion

The change in temperature is critical to consider when designing PCBs. Depending on the materials in the assembly, the constraints, and the difference in temperature that the product experiences, there can be plastic deformation from thermal stresses alone. For there to not be any plastic deformation the temperature difference has to be small enough to stay in the elastic range of the material. As the temperature increases, there is a positive change in length on the material leading to a positive normal strain. Conversely, as the temperature decreases, the length becomes smaller, and the material exhibits a negative normal strain. The CTE is a constant material property that describes how the material reacts to a temperature change. In many instances, engineers are unable to control the environment of their product. This is why it is important to select materials in an assembly that have as close of a coefficient of thermal expansion as possible. The change in length a material undergoes from a temperature difference is:

$$\Delta l = \alpha l_0 \Delta T$$

Where α is the linear coefficient of thermal expansion and is defined as strain per unit temperature. For Isotropic materials, the change in area and volume expand or contract two and three times as much as the length does respectively. How a material expands or contracts depends on the bonds of the materials atoms. For example: silicon carbide and diamond have strong atomic bonds and have higher CTE values than common metals such as stainless steel. It is important to note that if the material being subjected to a change in temperature is free, there will be no induced stress. Thermal stresses can appear in a couple of ways. The first would be if the material is under constraint. It can also depend on how other interacting materials react to the heat. Other instances to cause thermal stresses to appear would be if the temperature distribution is non-uniform. Examples of this would be external heat, or if the temperature profile along the material is transient. In electronic devices the thermal stress is caused by both of these factors.

Thermal expansion happens in all three directions and does not affect the shear strain components in the strain tensor. The normal strains can be defined as:

$$\epsilon_{11} = \left(\frac{1}{E}\right)[\sigma_{11} - \nu(\sigma_{22} + \sigma_{33})] + \epsilon_{11}^{p} + \alpha\Delta T$$
$$\epsilon_{22} = \left(\frac{1}{E}\right)[\sigma_{22} - \nu(\sigma_{11} + \sigma_{33})] + \epsilon_{22}^{p} + \alpha\Delta T$$
$$\epsilon_{33} = \left(\frac{1}{E}\right)[\sigma_{33} - \nu(\sigma_{11} + \sigma_{22})] + \epsilon_{33}^{p} + \alpha\Delta T$$

The plastic strain that has already taken place in the material is defined as ϵ_{ij}^{p}. This project focuses on the thermal cycling stress analysis and does not add any mechanical force or vibration into the testing environment.

2.3 Electronic Package Thermal Stress

When two or more objects meet at an interface, the change in temperature often cannot be neglected because of the differing CTE values. As already described, a non-uniform temperature profile, or constraint scenarios can cause thermal stress. Both of these cases are commonly seen in electronic packaging. Individual parts of the assembly will exhibit more strain than others when an assembly of materials have different CTE constants. Ways to maximize the life of the solder joint is to increase the height h, minimize the CTE mismatching, and keep the size of the electronic package as small as possible [36].

Shown in the previous tables, the CTE for Arathane is significantly greater than Almatis 20%, 63Sn37Pb, and Polyimide. The conformal coating is able to flow underneath the electronic packaging and is allowed to cure to test specimens where no underfill material is used. As the board is in operation the coating expands faster than the rest of the assembly as the heat flows from the package to the substrate. This poses a risk for the reliability of the solder joints. When the heat migrates from the package to the board, the coating expands at a much faster rate than the solder and with the added constraints; the solder is under a much more stressed state. In a cross section such as Figure 8 [21], the solder takes up considerable less area than the coating does. The solder can typically be neglected when analyzing this layer of the composite. The amount of thermal stress resulting in the coating layer can cause the joints to fracture or crack. This poses many risks for the component such as reduced reliability and life expectancy.

Horizontal displacements dominate the deformation in electronic packages. Electronic packages are often symmetric about an axis that is in the center of the chip. There is no resulting deformation from the differing CTE values along the axis of symmetry. As the distance away from the axis increases, the resulting stresses also increase. Figure 5 illustrates how the package responds to the CTE mismatch [21].

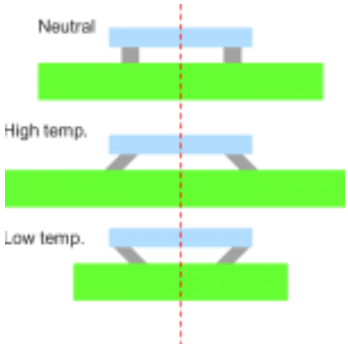

Figure 5. Solder Joint Strain from CTE Mismatch (Sharon, DFR Solutions)

When the temperature increases, the materials expand and the resulting force pulls the solder away from the symmetric axis. As the temperature decreases, the materials shrink at various amounts depending on their given CTE values, and a compressive like force pulls the solder toward the axis of symmetry. The distance from the symmetric axis to the solder joint is referred to as the Distance to the Neutral Point or (DNP). As this DNP increases, so does the stress that the solder joint experiences.

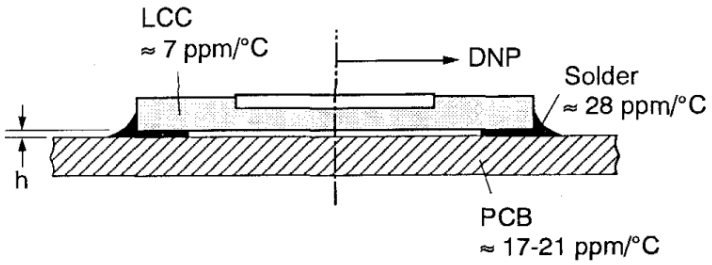

Figure 6. Thermal Expansion of an LCC Package (Han/Guo, 1996)

Figure 6 shows the approximate CTE values corresponding to each assembly material for a typical LCC [11]. For electronic package assemblies, the maximum average shear strain of a solder joint γ_{ave}^{max} is:

$$\gamma_{ave}^{max} = DNP * (\alpha^{PCB} - \alpha^{LCC}) * \Delta T * \frac{1}{h}$$

3LCC: $0.050^{in} * \left|(7 - 55) * 10^{-6\frac{1}{^\circ C}}\right| * 130^{^\circ C} * 0.005^{in} = 1.56 * 10^{-6}$

24LCC: $0.115^{in} * \left|(7 - 55) * 10^{-6\frac{1}{^\circ C}}\right| * 130^{^\circ C} * 0.005^{in} = 3.59 * 10^{-6}$

h is equivalent to the solder joint thickness. The height can be characterized by the distance the LCC is away from the PCB. For void growth that leads to solder fractures, the equation below relates the stress as a function of temperature extremes [14].

$$\sigma_t = 3\Delta\alpha\Delta TK$$

K is the bulk modulus of the conductor. This assumes that the passivation film that covers the conductor, such as silicon nitride, remains rigid.

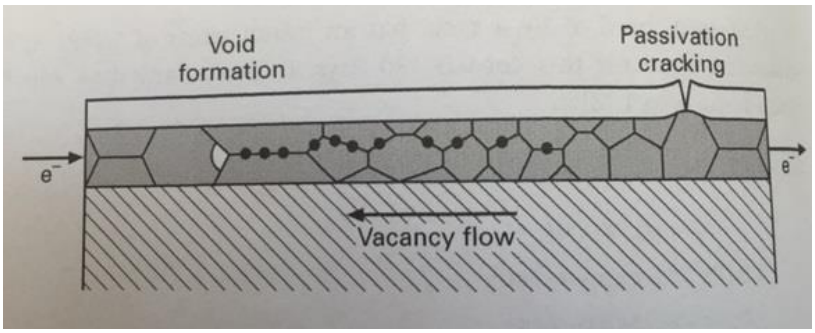

Figure 7. (Meyers, 2009)

Figure 7 portrays how the solder interconnect, (in this case made of aluminum) is covered by a passivation layer over a silicon board [14]. It can be seen that the vacancy flow is in the opposite direction of the electron flow. The passivation layer cracks due to the formation and buildup of voids that result from the thermal mismatch. This also leads to the solder alloy fracturing.

2.4 Creep

Creep is defined as material plastically deforming at a constant stress at a temperature a fraction below the melting point. For creep to take place, the temperature of the environment is typically in the range of 40% to 65% of the melting temperature [14]. The material undergoes both mechanical and chemical degradation during this environment. Mechanical degradation depicts how the material expands as time increases. Chemical degradation describes how the material reacts with its environment.

Creep can especially take place because of the low melting point of solder. The melting temperature of 63Sn37Pb solder is 456°K. Creep must be taken into consideration during the 20 minute dwell time at 343°K. This is 75% of the melting point. Creep can very well induce a fracture in the solder alloy. Cavities start to form in between grain boundaries after creep has taken place. Once this happens the cavities begin to grow and come closer to one another ultimately leading to a fracture. The cracks appear at the grain boundaries. There are equations that predict the time to failure, as this one for example:

$$\dot{\epsilon} t_r = k$$

The above relation is called the Monkman Grant equation [14]. Where $\dot{\epsilon_s}$is the steady state creep rate, t_r is the time to rupture, and k is the material constant.

2.5 Glass Transition Temperature

Part of the process in choosing an appropriate thermal profile was to take into the glass transition temperature (T_g) of the underfill, coating, and solder alloys. If testing temperature falls below the T_g, the material can function as a glass, meaning that no specific order exists between

the atoms [14]. This phenomenon takes place for metals, polymers, and ceramics. The packing between the atoms is less effective when they are in a glassy state. The atoms are packed in a random order and will occupy more space than a crystalline structure. If the materials assembly only stays within a specific glass transition temperature range, it is important to replicate the same environment in accelerated testing.

The higher extreme was bounded by the glass transition temperature of Almatis 20% as 80°C. Arathane were found to be -69°C [2]. To stay as close to this temperature as possible, helps to ensure that the underfill remains in a glass state. This will be similar to the real life scenario of the product.

2.6 Crack Propagation

If the 63Sn37Pb eutectic solder does become damaged from the thermal cycling it is still possible for the unit to function electrically. It is simply not enough necessary diligence in our testing to daisy chain the unit and then perform a continuity check. The cracked solder still qualifies as mechanical damage to the unit. The crack can easily transform into a fracture if stressed further over time. It is not until the lead is fully open where current will not be able to flow through the joint. This will in turn cause a hard failure in the device. There are different modes that describe how cracks are allowed to propagate. They are often referred to as opening, in-plane shear, and out-of-plane shear. The crack propagation modes are presented in Figure 9 [16].

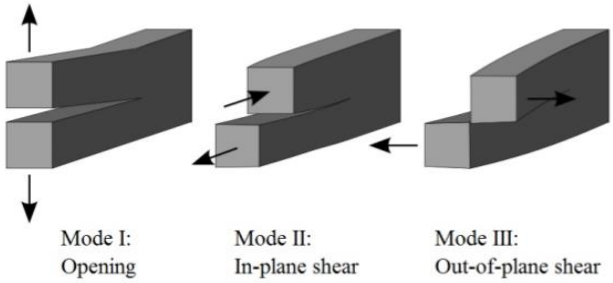

Figure 9. Modes of Failure (Patil, 2014)

Thermal cycling leads to the "open" case of crack propagation in solder joints. Assuming plane strain, the fracture toughness can be described in terms of stress [14] by this equation:

$$K_{IC} = Y\sigma\sqrt{\pi a}$$

Where a is the semi-length of the crack, Y is called the stress intensity factor and is geometry dependent. Once a crack is initiated it becomes a stress concentrator. The fracture toughness of 63Sn 37Pb solder is 8.36 $MPa\sqrt{m}$ [32]. This was determined from the "open" crack propagation case. According to the Griffith criterion, a crack will become larger if the elastic

strain energy released is larger than the surface energy from the new crack surfaces. Under most cases the solder joint does not fail at the interface. It usually fractures just below the interface [8]. Figure 10 illustrates a fractured joint under thermal fatigue.

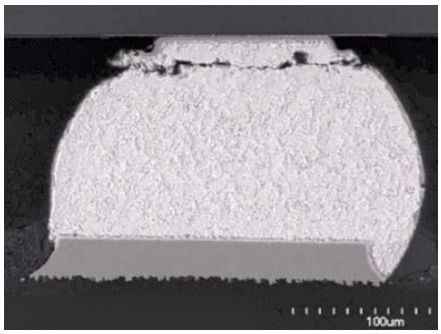

Figure 10. Common Solder Fracture (Edwards, 2012)

Through the FEA model it is possible to predict where the cracking will occur given the geometry and temperature profile.

Initial FEA Research

The 3LCC and 24LCC electronic devices were modeled using FEA software developed at Sandia called "CUBIT". These models were simplified due to geometry and to save computational processing time as explained above. There were many different types of modeling scenarios for the LCC components. Due to the difficulties to achieve some of these scenarios physically the experimentation was scaled down to conformal coating with and without underfill. There are three modeled scenarios that I compared my test results to. The first had conformal coating above the package, as well as a layer between the Polyimide and the device. This particular scenario had the lowest number of cycles to failure and affected the solder the most. The second scenario had conformal coating over the board and component with a void in between the component and PCB. The scenario with the highest number of cycles to failure was also conformal coating above the components with underfill in between the board and component. A list of the theoretical cycles to failure for each component is listed in Table 3.

24 LCC Cycles to Failure	
Arathane above and below component	22.2
Arathane above component only	88.6
Arathane with UF	328.6
3LCC Cycles To Failure	
Arathane above and below component	24.1
Arathane above component only	457.6
Arathane with UF	4800

Table 3. Analytical Predicted Number of Cycles to Failure

There were two different temperature profiles that were simulated, one was daily use and the other was an accelerated profile. The daily use profile simulated a small change in temperature over a period of 24 hours. The number of cycles to failure averaged in the hundreds of thousands and was not of much significance. The daily use profile was accelerated and the FEA was redone to greatly reduce the number of cycles to failure so that the UUTs could be tested experimentally.

The accelerated temperature extremes simulated were -50°C to 85°C. The dwell times were for 1.5 hours. As expected, the number of cycles to failure was significantly higher if the package was not underfilled. Experimentation was not performed in the same manner as the modeling. The temperature range was slightly narrower, by 5 degrees, the ramp rate was increased, and the dwell time was taken to be 20 minutes to perform a higher number of cycles in a shorter period of time.

When comparing the FEA analytical data to the results obtained experimentally, it was important to realize the advantage if the data sets did not match. It was often discussed what the implications were if the experimental results yielded a higher number of cycles to failure compared to the analytical results. There are a few advantages to having a higher number of cycles to failure experimentally. The first gain would be time. On average, it takes several minutes to underfill a component. Once the resin is placed underneath, the package is placed in a chamber for the underfill to cure. For both circuit boards tested, this process took 48 hours for 18 components. While the cure time for Almatis 20% is short, additional turnaround time involves contact and planning with the vendor, working the project into the queue, and delivery of the UUTs. Another advantage is cost. By going into production needing a large number of units populated, savings in cost can be in the upper thousands of dollars. Since underfill is done by hand, this leads to an increase in reliability by eliminating an unnecessary step in the assembly line.

Environment Safety and Health (ES&H)

There were a couple of issues and concerns pertaining to ES&H while testing. While checking for functionality in between testing cycles, time had to be taken to bring the board up to a safe “usable” temperature. After the extreme cycles were complete, the board was brought down to ambient conditions and held at a constant temperature in the chamber for 20 minutes. The thermocouples were also monitored to verify the parts were at a safe handling temperature. The thermal chamber is secured with a stainless steel latch and when opened, the safety switch disengages and the thermal cycling stops. There were periods of the day when the chamber would run without supervision. A safety sign was posted with instructions how to power the chamber off incase an emergency did occur.

The use of 63Sn37Pb solder did not bring any ES&H concerns during testing and inspection. Strict Sandia safety procedures were practiced when soldering the devices onto the board. Also, there is a minimal amount of outgassing produced from the conformal coating during the experiment [1& 2] so this was not a concern.

3.1 Electrostatic Discharge

It is important to consider the damage caused from electrostatic discharge (ESD) when working in a robotics or electronics lab. There are many different controls that can be used when protecting again static electricity such as flooring material, different types of shoes and clothes, and even the proper posture of the tester. Static electricity can be built up, released on the circuit board, and damage components, traces, and other critical components that affect the reliability of the circuit.

Both of the PCBs were susceptible to ESD damage and there were several controls in place when protecting against it. The first, probably most important control was wearing a grounded ESD jacket to protect against electrostatic build up from clothes and movement. Other ESD protections involved ESD safe flooring, and grounded mats on the top of the workbenches.

It is also possible for static electricity to be generated through the air. Ionizing fans were used to blow a mixture of positive and negatively charged ions onto a surface to neutralize a surface. When transporting the PCBs, ESD safe bags were used to insulate the boards. In addition, the X-TEK was not grounded and the electronics assemblies were kept in their ESD bags.

Accelerated Testing

Accelerating the mechanical environment is a useful practice that is rapidly gaining popularity. Perhaps the most useful aspect of accelerating the mechanical testing is to save time, and ultimately save money. The primary goal of Accelerated Testing is to gain an understanding of the performance and life of the product in a timely manner.

With accelerated testing, engineers can perform the test quickly and efficiently without the worry of extending deadlines and design phase changes. Accelerated Testing (AT) is part of the field known as Quality and Qualification Engineering. This concept can save millions of dollars in qualifying the product in the design phase rather than spending time repairing each unit after it has already hit production.

It is important to consider a few factors when accelerating thermal tests. One can increase the use rate of the product lifespan or the aging rate to accelerate the reliability. There are many different mathematical models that can be used to see how fast a product is accelerated. It is extremely important to determine the correct acceleration profile for the component. Choosing an incorrect profile can lead to different failure modes and will lead to useless information for the product. For this project the aging rate was increased by altering the use environments the product functions in.

The sole purpose of accelerated testing is to check for possible failure modes in the unit in the R&D phase rather than after it has already hit production. This is done by making the test environments more extreme than the use environment. The temperature environment was made more severe by increasing the maximum and minimum temperature extremes, the temperature ramp rate, and the number of cycles performed. The temperature extremes, ramp up and down rate, dwell time, and number of cycles all have a number of effects on the accelerated test [33].

The higher change in temperature extremes causes the material to strain more [33]. Obviously it is important to consider the temperature range the tester is capable of as well as the glass transition temperature of the epoxies and fill materials. This was further explained in the glass transition temperature section. At the larger temperature extreme creep can take place if the testing temperature is greater than about .45 to 0.6 the melting temperature of the material.

The dwell times that the maximum and minimum temperatures are held also play a large role in accelerating the life of the part [33]. In general the longer the dwell time in each model, the longer the Acceleration Factor (AF). Conversely, if the dwell time is to long the cycle time is increased and the AF is slowed down. Dwell times are also used to ensure that the tested component has hit a steady state temperature. The length of the dwell time is solely used for this purpose.

The ramp rate is also an important factor when dealing with AT. This helps accelerate weaknesses in the product that are thermal rate dependent [33]. The strain rate increases as the ramp rate increases. Increasing the strain rate leads to the stress in the solder to rise. A typical ramp rate is around 5°C per minute. All of the acceleration models described in the next section do not take into account thermal change rate.

One of the most important factors in accelerated testing is the number of thermal cycles performed. For qualification and quality performing somewhere between 5 and 20 cycles can be adequate [5]. In some mathematical models, the number of cycles is not taken into account when calculating the acceleration factor. The primary focus in accelerated testing is to perform a large number of cycles in a short amount of time.

4.1 Acceleration Models

There are several different models that have been developed to determine the AF. Various AF models were researched and compared to gain a better understanding on how the normal environmental profile can be increased. Coffin Manson, Vasudevan, Miremadi, and Clech acceleration models were all used and compared to gauge a better understanding of which thermal profile would be the most optimal.

4.2 Coffin Manson Equation

The Coffin-Manson equation was developed by L.F. Coffin in 1954 and S.S. Manson in 1953. The equation is used for low-cycle fatigue experiments and is commonly used for solder fatigue. The long expression for the number of cycles to failure [33] is:

$$N_f = A * f^{-a} * \Delta T^{-b} * \exp\left(\left(\frac{EA}{K}\right) * \left(\frac{1}{T_{max}}\right)\right)$$

- N_f = number of cycles to failure
- A = coefficient
- f = cycle frequency
- a = -1/3
- ΔT=Temperature range through 1 cycle
- $b = 1.9$
- EA = Activation energy taken to be 0.42
- K = Stefan Boltzmann constant $8.623*10^{-5}$ eV/K
- T_{max} = Maximum Temperature

For 63Sn37Pb solder the Coffin-Mason equation can relate the number of cycles to failure N_f, to the plastic shear strain range $\Delta\gamma_p$, or the equivalent plastic strain $\Delta EQPS$ [6].

$$N_f = \left(\frac{1.14}{\Delta\gamma_p}\right)^{\frac{1}{0.51}} = \left(\frac{1.31636}{\Delta EQPS}\right)^{1.96078}$$

This simplified form of Coffin-Manson is particularly useful in FEA studies for solder reliability. The number of cycles to failure is found from the equivalent plastic strain. The plastic strain is calculated from FEA results which are derived from temperature the UUT is exposed to. The strain is a function of the change in temperature and how the solder is constrained.

The Coffin Manson equation can also be expressed in terms of AF. This takes into account the dependent factors explained above such as temperature extremes, and number of cycles. It can also be defined as the ratio as number of cycles to failure for the experiment and use environments [33].

$$AF = \frac{N_L}{N_H} = \left(\frac{\Delta T_H}{\Delta TL}\right)^b * \left(\frac{f_L}{f_H}\right)^{-a} * \exp\left(\left(\frac{EA}{K}\right) * \left(\frac{1}{T_{KL}} - \frac{1}{T_{KH}}\right)\right)$$

- AF = Acceleration Factor
- N_L = Number of cycles to failure at the use condition
- N_H = Number of cycles to failure at the experimental condition
- ΔT = Temperature Range
- f = Cycles per day
- T_{KL} = Maximum use temperature in Kelvin
- T_{KH} = Maximum experimental temperature in Kelvin
- EA = Activation Energy
- K = Stefan Boltzman Constant $8.623 * 10^{-5}$eV/K

The subscript *H* and *L* are for the accelerated testing and use conditions respectfully. The other constants and variables are the same as the number of cycles. One note of concern is that Coffin Manson model does not depend on the dwell time and ramp rate of the conditions. They are not explicit as they are both expressed in the number of cycle's term of the equation. Coffin Manson is unable to distinguish thermal cycling compared to thermal shock. The difference between the two is generally described by the temperature ramp rate [33].

There were other AF equations that were researched to see how Coffin Manson differed compared to other acceleration factor models. It is important to note that each equation takes into account different test variables. The Vasudevan model takes into account cycles per day for use and test temperatures. Dauksher and Miremadi take into account the change in temperatures and dwell times with different constant variations. All of these models can be used for the purpose of solder joint fatigue. These are listed to show the differences between them, and how there are different methods and assumptions used in each. These models were compared in Matlab to gain an understanding of the differences between them and how varying the test parameters would affect the AF.

The Dauksher model [36] can be defined as:

$$AF = \frac{N_2}{N_1} = \left(\frac{\Delta T_1}{\Delta T_2}\right)^{1.75} \left(\frac{t_1^{HOT}}{t_2^{HOT}}\right)^{\frac{1}{4}} exp\left(1600\left(\frac{1}{T_{2,MAX}} - \frac{1}{T_{1,MAX}}\right)\right)$$

The Vasudevan model [36] is:

$$AF = \frac{N_1}{N_2} = \left(\frac{\Delta T_1}{\Delta T_2}\right)^{-1.9} \left(\frac{f_1}{f_2}\right)^{-.33} \exp\left(1414\left(\frac{1}{T_{1,max}} - \frac{1}{T_{2,max}}\right)\right)$$

The Miremadi model [36] is:

$$AF = \frac{N_o}{N_t} = \left(\frac{\Delta T_t}{\Delta T_0}\right)^{a} \left(\frac{t_t}{t_0}\right)^{b} \exp\left(c\left(\frac{1}{T_{max,0}} - \frac{1}{T_{max,t}}\right)\right)$$

The Coffin Manson method combined with using FEA software to calculate an equivalent number of cycles to failure is the primary method that Sandia uses for accelerated testing. There has been a considerable amount of research done to determine the acceleration profile for these materials. The different AF models were used to compare the FEA model acceleration factor with the experimentally derived model. The Coffin Manson model showed an AF of 1.53 from the FEA model to the experimental model. Even though Coffin Manson showed an increase, 2 of the 4 models showed a decrease in acceleration from the FEA model to the experimentation profile. It was assumed that both models were similar to compare the experimental and FEA data.

The experimental acceleration profile is slightly different compared to the accelerated FEA model. The temperature range will be -20 to 70°C. This range will keep all materials in between their glass transition temperatures and allow for over shoot in the chamber. The dwell time will be 20 minutes for each extreme instead of 90. This will allow for more cycles to be complete in one day. The ramp rate will be 5°C/min to reach the hot and cold cycles. Different numbers of cycles were run before and after each failure mode.

It would take approximately 29 and 300 days to achieve 457 and 4800 cycles respectively for the experimentally tested profile to reach the FEA predicted cycles to failure. Once the electronics assemblies had been thermally cycled past the second failure with a considerable amount of margin, it was assumed that the remainder of the surviving devices would follow the underfilled failure model.

Manufacturing

5.1 PCB Fabrication & Population

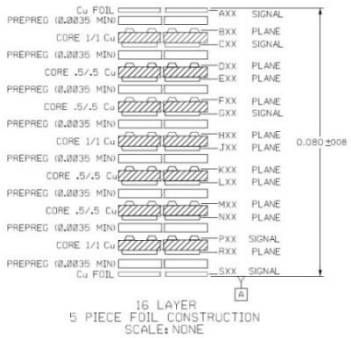

Figure 11. PCB layers

The PCBs being tested were populated and coated at L&L Electronics, Inc., (L&L for short) in Albuquerque, NM. Sandia was able to manufacture the circuit boards and the devices. Each PCB is composed of 16 layers with datum A as the bottom surface described in Figure 11. Overall, both circuit boards measured 7 by 8 inches, as shown in Figure 12, with a nominal thickness of 0.080 inches.

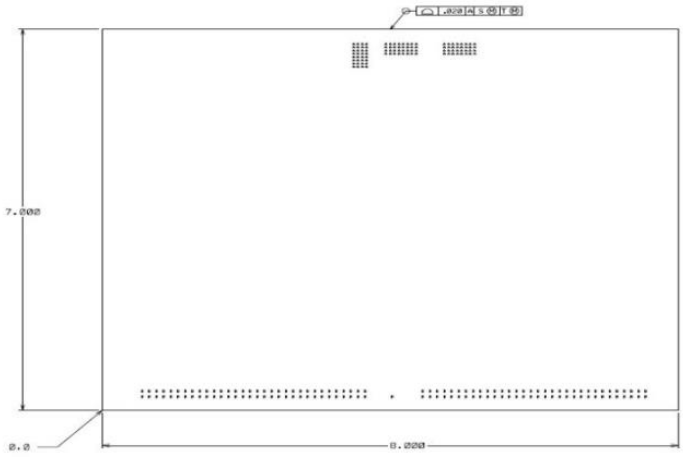

Figure 12. J27446 and J27447 PCB size

Photos of the blank boards are shown in Figure 13. The 24LCCs were placed on Board J27446 and the 3LCCs were placed on board J27447. The boards had 32 pads for components to be placed on and came in a 5x6 grid with 2 extra pads near the top.

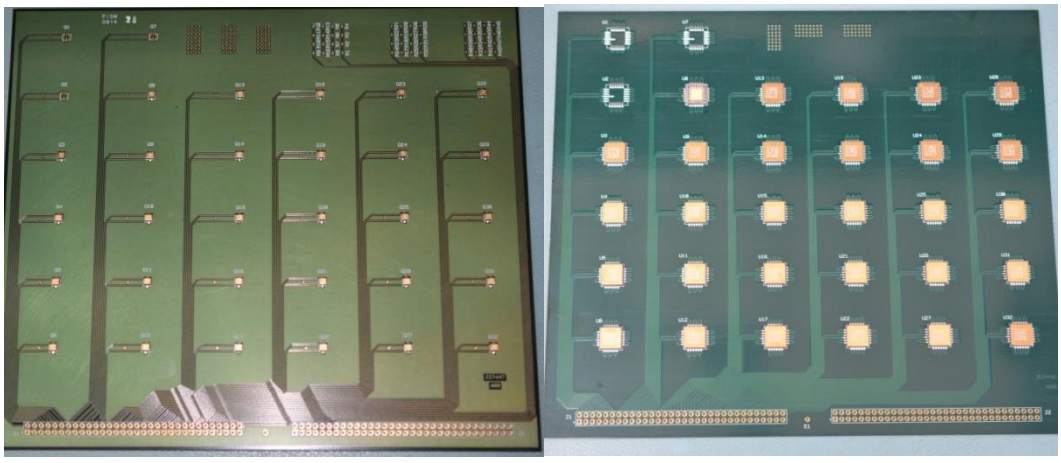

Figure 13. Populated electronics assembly

The Microsystems Group produced shorted components for 29 of the 32 spots on the board. When it came time to populate, L&L left reference designators Q1, Q2, and Q7 empty on the top left corner for board J27447 and similarly U1, U2, and U7 for board J27446. In addition, one of the 24LCCs was de-lidded in manufacturing. This unit was placed in designator U8 and was tested in comparison with the other units. This is shown in more detail in Figure 14.

When placing surface mounts on PCBs, manufacturers make a custom stencil that traces out the pads for the electronic packages. Solder paste is swabbed over the stencil and applied over the pads. The stencil is then removed and the components are placed by hand on top of the solder pads. L&L then places the PCBs in a reflow oven completing the placement procedure. If the device is not placed in line with the pads by hand, the oven will correct the position.

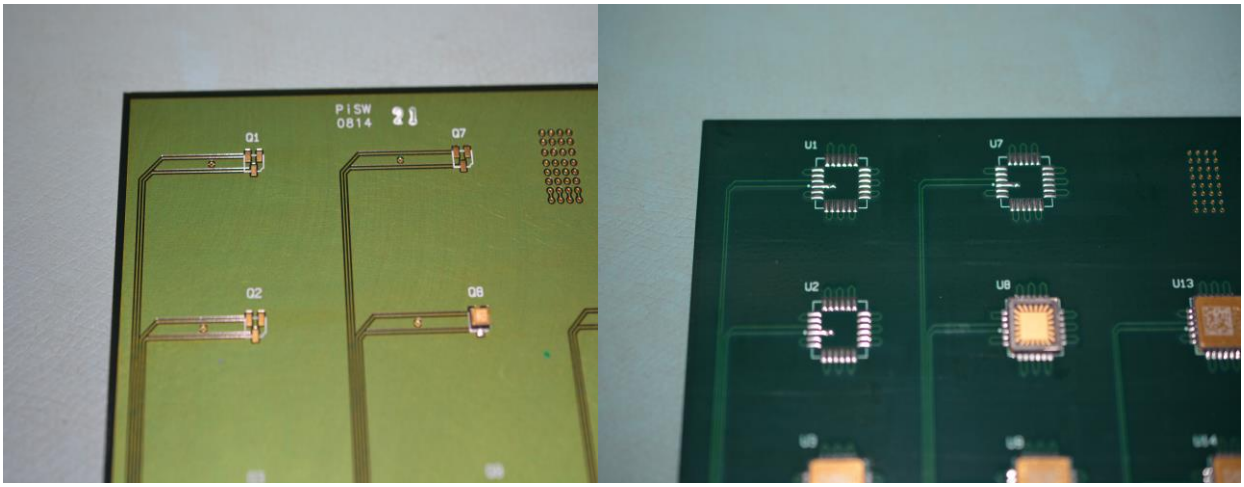

Figure 14. Detail view of blank pads and de-lidded component U8

5.2 Underfill & Conformal Coating

There were more components tested with only conformal coating rather than the combination of conformal coating and underfill. This was due to an uneven number of test combinations. It was decided that a higher number of components were to be tested with no underfill because the number of cycles to failure is much lower than the underfilled components as explained in the Coffin Manson section. Figure 15 shows a layout of the boards and identifies which components were to have underfill using Almatis 20%.

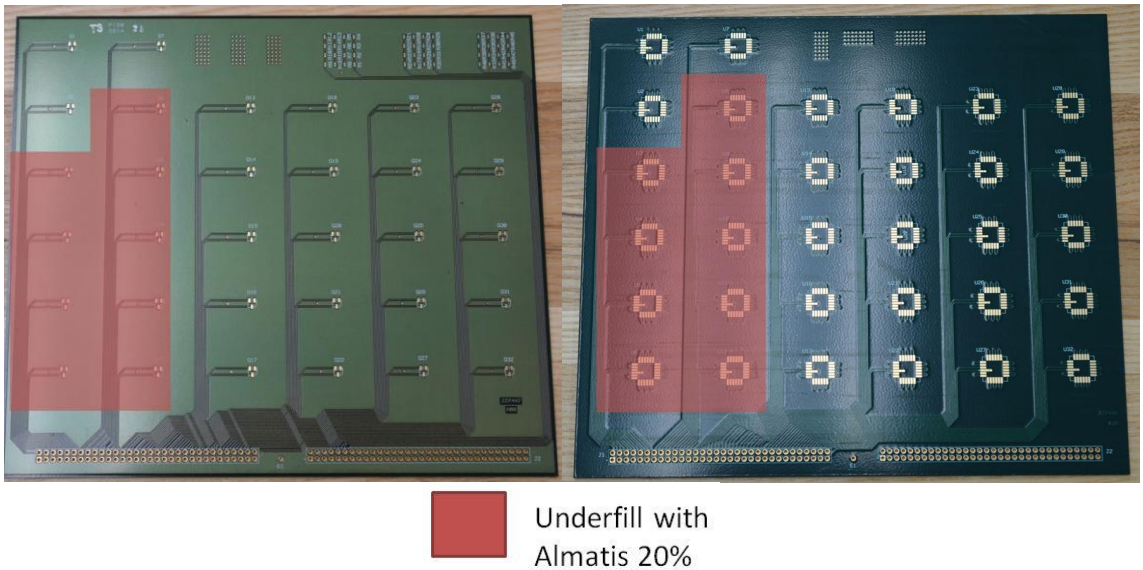

Figure 15.

Various sections of the boards had to be masked out to properly expose test points on the board. The majority of the boards were conformal coated by L&L on the front and back side of the

boards. The areas that were masked out included continuity test points, vias, and pads for resistors. Figure 16 and 17 show the areas that were requested to be masked out.

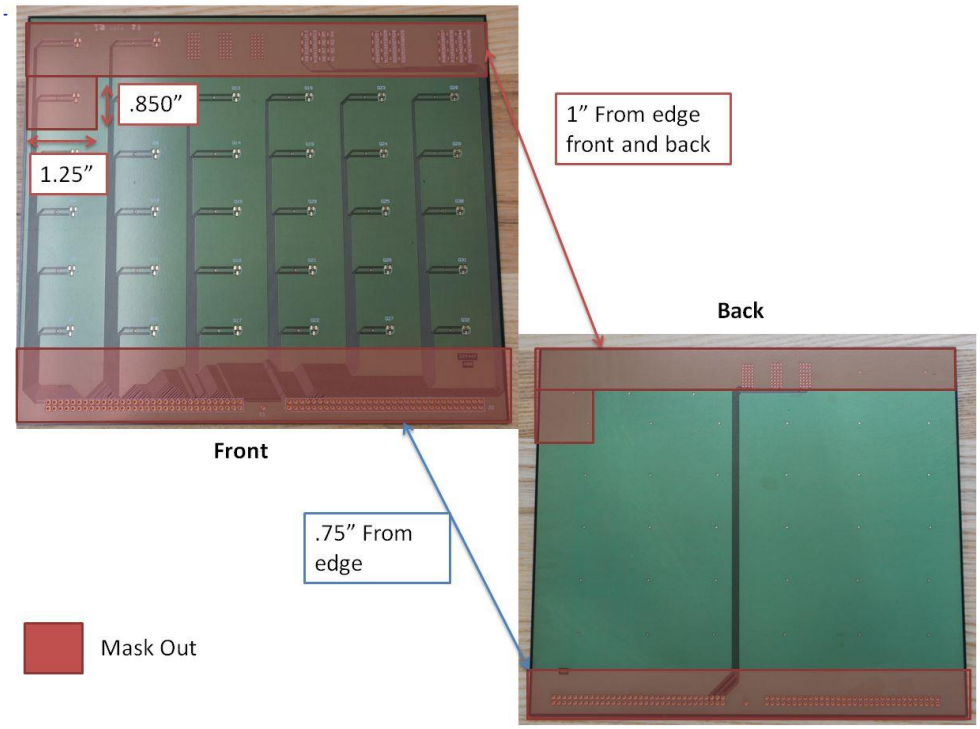

Figure 16. Masked out areas for board J27447

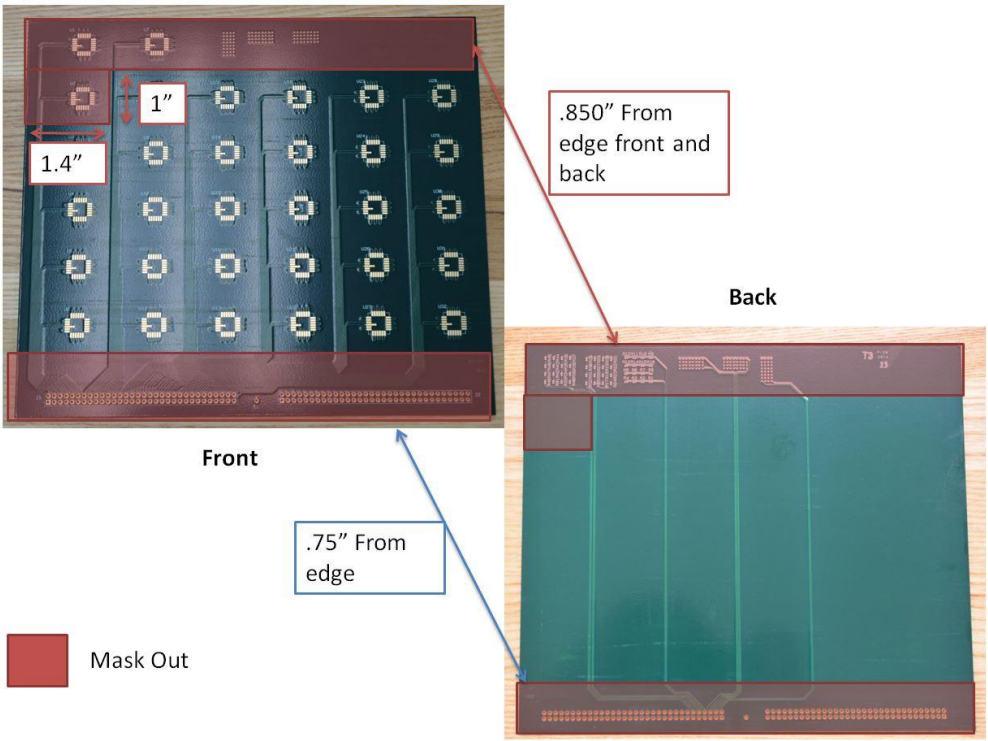

Figure 17. Masked out areas for board J27446

The electronics assembly was carefully inspected after they were received from the vendors. The underfilled components were verified with a microscope and the test points were inspected for no coated regions.

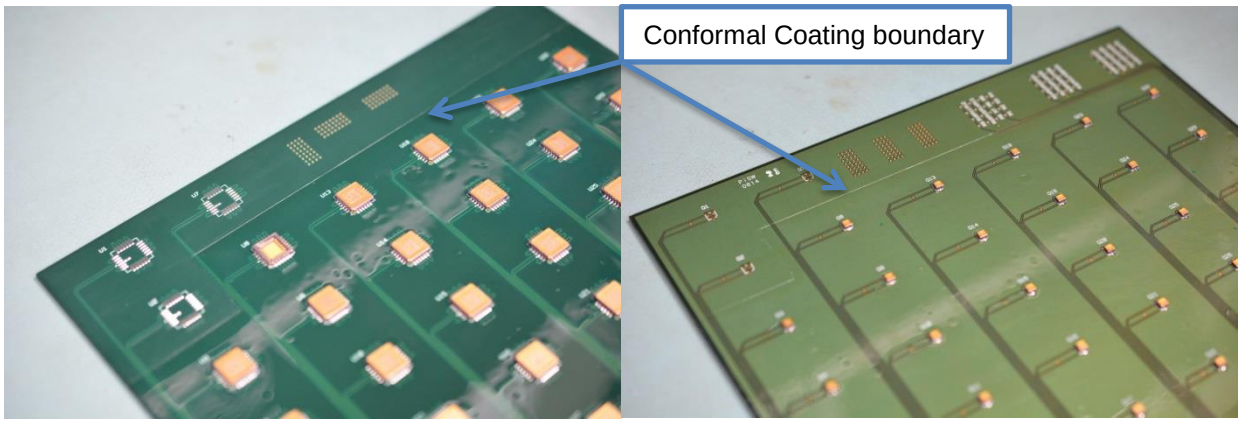

Figure 18. Arathane coated boards pretest

There were several steps taken to ensure that the testing was performed in the most optimal manner. To keep track each component, the rows and columns were labeled in a matrix orientation as illustrated in figure 18 and 19. This naming convention was used throughout the remainder of this report. Table 4 describes where the conformal coating and underfill was applied.

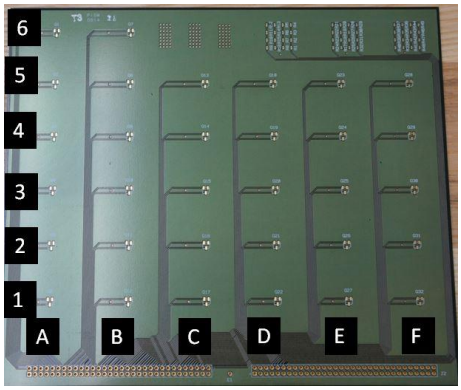

Figure 18.

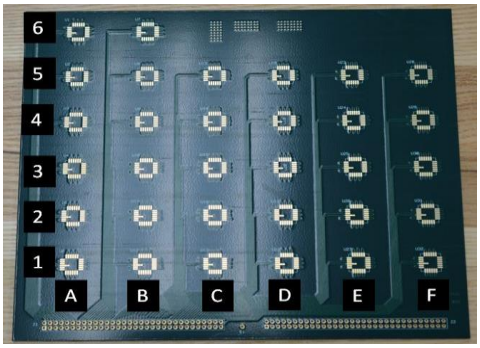

Figure 19.

Column	Conformal Coating	Almatis 20% Underfill
A	Arathane	Y
B	Arathane	Y
C	Arathane	N
D	Arathane	N
E	Arathane	N
F	Arathane	N

Table 4. PCB Coating and Underfill Layout

Experimental Setup & Test Equipment

It took approximately 1.5 hours to complete a full thermal cycle. 3 groups of 10 cycles were initially run during the evening and at night. After 30 cycles were complete, 60, 110 and 200 cycles were run. An electrical continuity check was performed after every test that would indicate a positive connection between the electronic device and the circuit board. This is a standard check when testing for an open circuit. X-ray scanning was also performed in the mornings. This was to ensure that even though there was continuity between the board and the device, the x-ray scanning would show there was no cracking in the solder that could still constitute a failure.

6.1 Thermal Chamber

The thermal chamber is manufactured by Thermotron. The model number is S-1.2-3200. The temperature ranges from -73 to 180°C with a control tolerance of ±1.1°C. The internal volume is 1.2 cubic feet. This chamber was convenient because the test could be run over night and on weekends. The chamber uses a chiller as the cooling agent instead of liquid nitrogen which has to be continuously monitored and replaced. This chamber has simple usability and its settings allow the user to write a profile and allow it to cycle the temperature automatically. It is standard procedure to write the profile as a check list for easy usability. When setting the ramp rate, the user pre-calculates how long it will take to reach one temperature extreme to another and programs it into the DAQ. A procedure on starting the test, as well as the checklist profile is listed in the appendix.

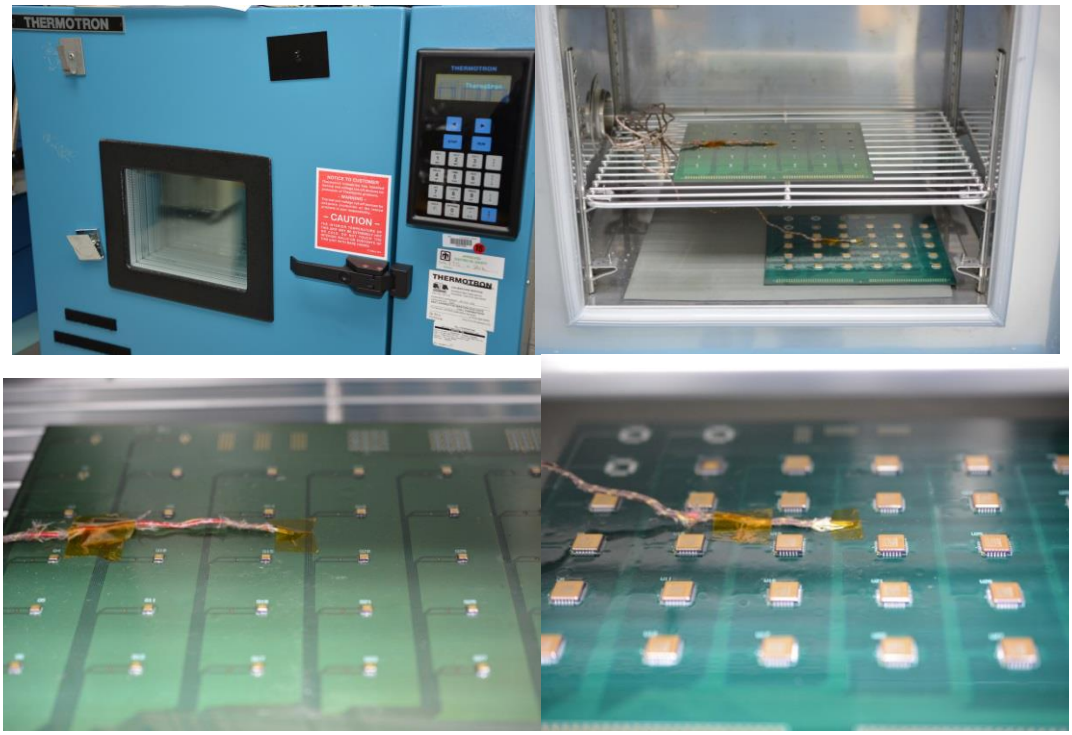

Figure 20. Environmental Chamber and Testing setup

6.2 Graphtec

K type Thermocouples (TCs) were placed on each board to measure the surface temperature while another was suspended in the air and used as the control sensor. Both PCB thermocouples were routed to a Graphtec that recorded the temperature cycles. The TC for board J27446 was channel 1 and TC J27227 was routed to channel 2 on the Graphtec. Kapton tape was used to secure the thermocouple to the board because of its wide temperature operating range.

Figure 21. [40]

The time per division on the Graphtec was set to 1 hour per division. The Graphtec was used to record the PCBs surface temperature and monitor the status of the number of cycles for the current test. It is able to record data for the large temperature cycle increments that took longer than 1 day to complete.

6.3 Fluke Digital Multimeter

Figure 22. [41]

One of the steps taken to verify that the solder is still making optimal contact is to see if there is still an electrical path from the device to the board. This can be done by either using a Digital Multimeter (DMM) or a continuity tester. A Fluke® DMM will be used for checking continuity for these tests. To check for continuity and measure the resistance, the following steps were taken:

1. Ensure that the black test probe is inserted in the COM jack, and the red probe is inserted in the Ω jack.
2. Turn the dial to Continuity Test mode ( ))))
3. If an electrical path has been made the DMM will measure the resistance. If there is no continuity the DMM displays "OL" on the screen.

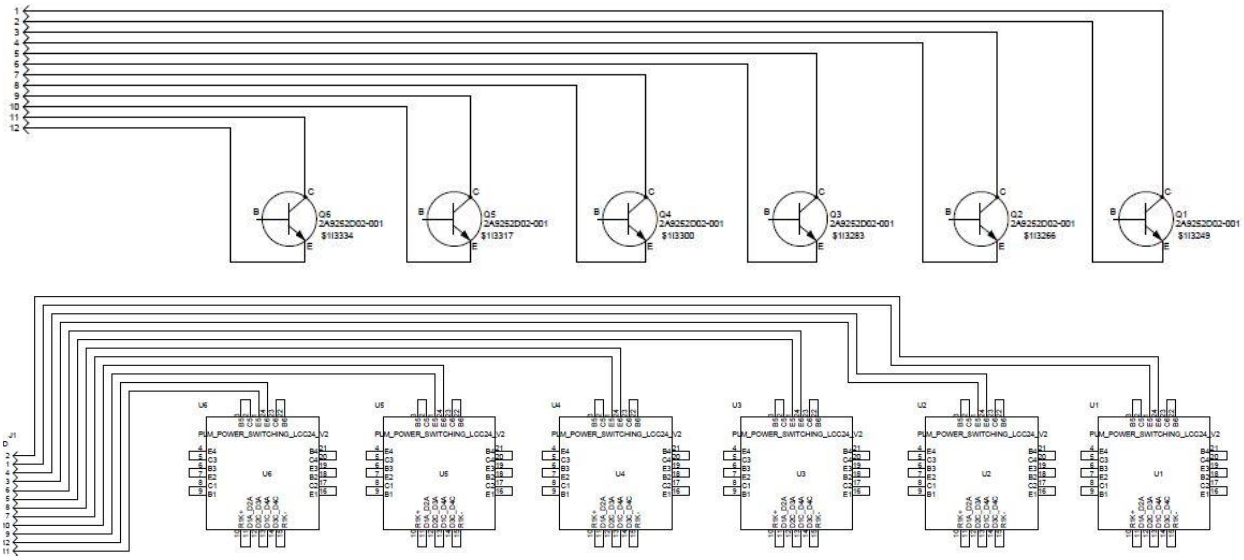

Figure 23. Board wiring diagram for J27447 (top) and J27446 (bottom)

The PCBs were manufactured in a manner where the path from the device leads to test points at the bottom of the board. The UUTs were daisy chained together which allowed for the current to flow throughout every contact point. With this electrical configuration the test probes from the Fluke were able to make contact with test points on the PCB and the resistance of the UUTs was measured thus signifying continuity.

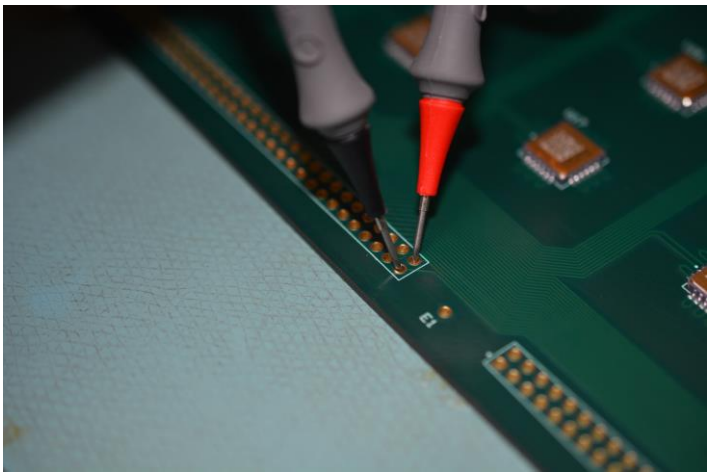

Figure 24.

6.4 X-Ray Screening

In some cases it had been reported that there might still be continuity in the circuit even though the solder is fractured or voids exist. An X-ray scan can be performed to verify that the 63Sn37Pb eutectic solder remains continuous throughout. This is a new technique and is an extra verification for the mechanical integrity of the joint. The North Star X50 x-ray system was used and it screens in 2D and 3D. Also, certain filters show voids easier than others when scanning for solder failure. Figure 25 shows an example of the same void but with two different filters on the North Star machine.

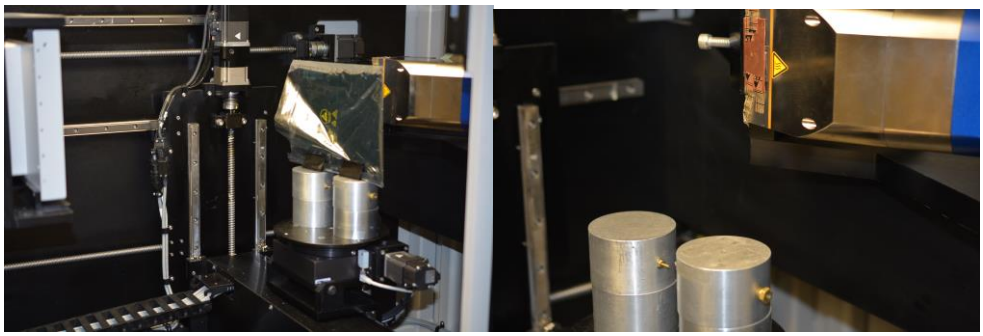

Figure 25. North Star X-Ray setup

There were three different kinds of filters used for the x-ray of each component. All three have their advantages and disadvantages. The first filter was a natural image of the device. To achieve a natural filter, the North Star would average the resolution of the image. The North Star used the natural image when its camera was in motion surveying each package. To view the component in more detail, the Wallis filter was used. The Wallis filter lowers the contrast in places where the contrast is high and vice versa. The contrast is increased in originally low contrast areas. Coloration can then be added to the Wallis filter. The third filter is a red Wallis filter which was added to emphasize impurities in materials such as voids, fractures, and lid seal

deformations. All three filters were variously used when scanning the UUTs. Examples of each are found on Figure 26.

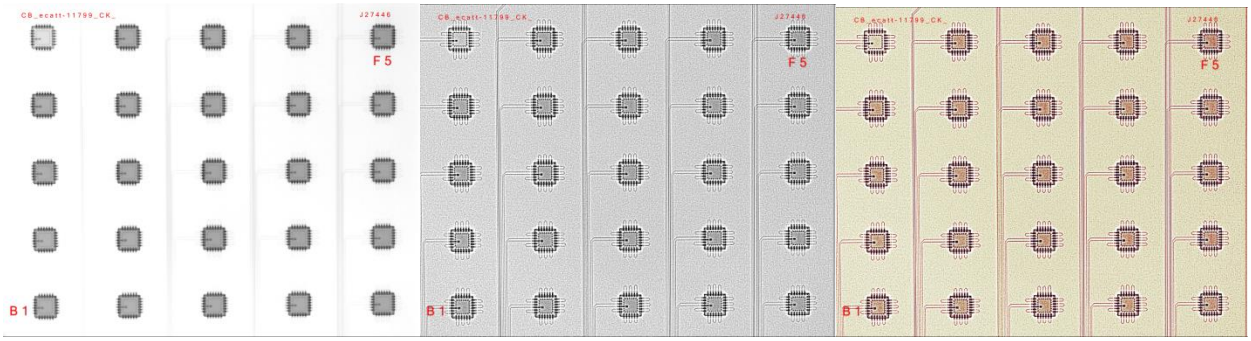

Figure 26. From left to right: natural image, Wallis filter, & red Wallis filter

Results

Temperature data was recorded from the Graphtec to verify that the program was set correctly. Both boards were able to reach each temperature extreme with in the allotted 20 minute dwell time, and set so that both PCBs changed temperature at the same rate. The second 10 cycles are shown in Figure 27.

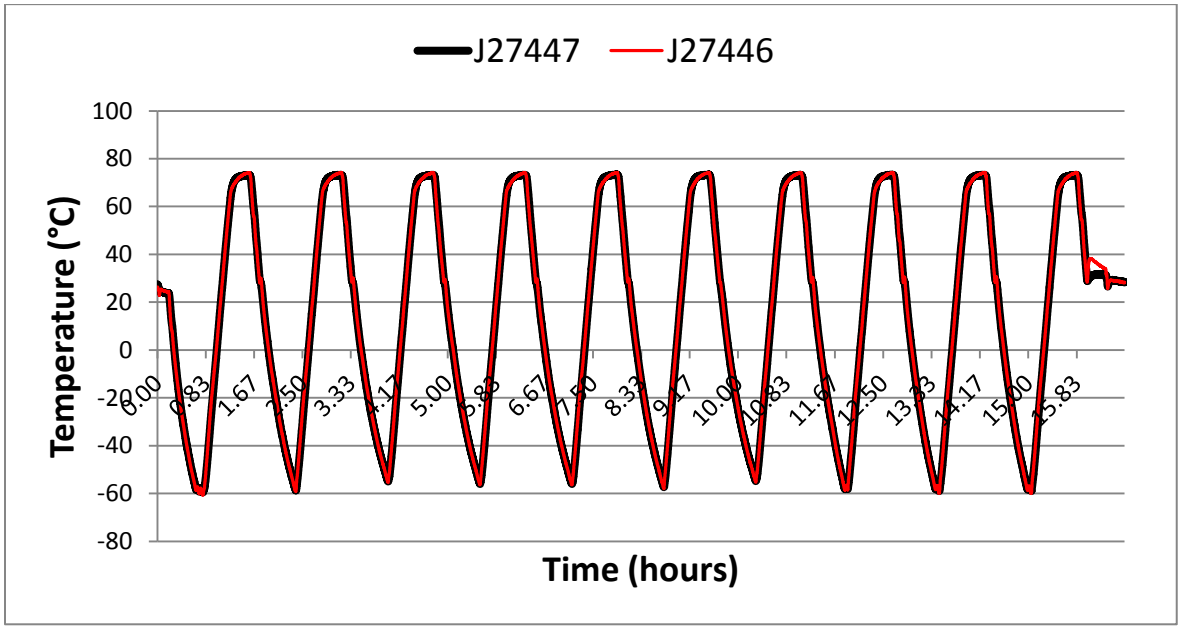

Figure 27. Board Mounted Thermocouple Reading for 10 Cycles

7.1 Initial Voids & Resistance

Resistance and X-rays were taken initially before testing and were used as a reference. Initial x-rays were saved for every device and were used as a comparison for future inspection after the other tests are completed. If the two x-rays looked the same pre- and post-test, the image was not saved.

There were a few interesting discoveries when initially x-raying the UUTs. The first was that there were a considerable amount of voids on the surface contact between the device and board. Some devices had more than others and they were found to be more common in 24LCC packages. These voids were formed during the manufacturing process and were closely monitored after each test. In a few instances there were voids around the wire bond.

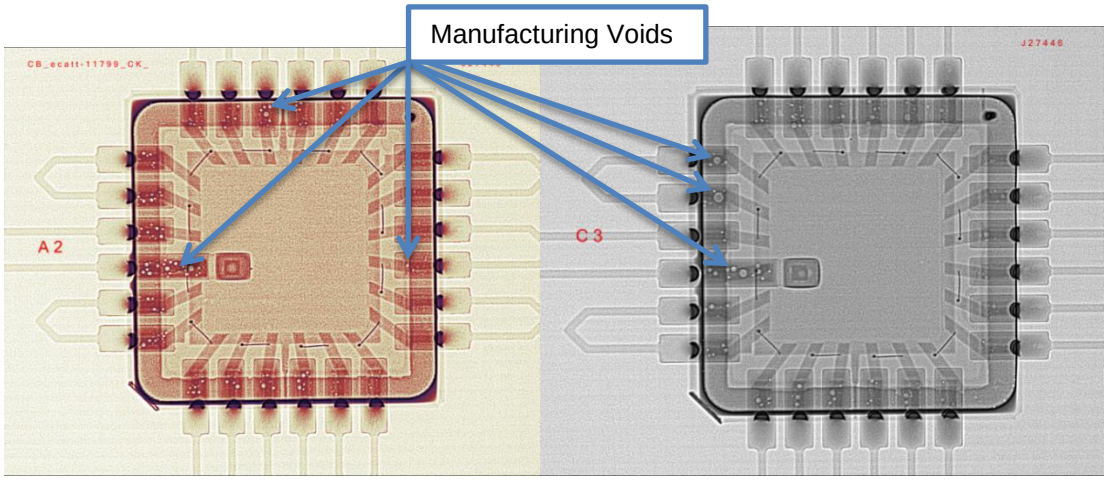

Figure 28. Manufacturing voids.

Another interesting finding was that many of the wire bonds used for daisy chaining the components were curved. On component B4 there was a missing tail on a wire bond. The curvature in the wire bonds varied component to component.

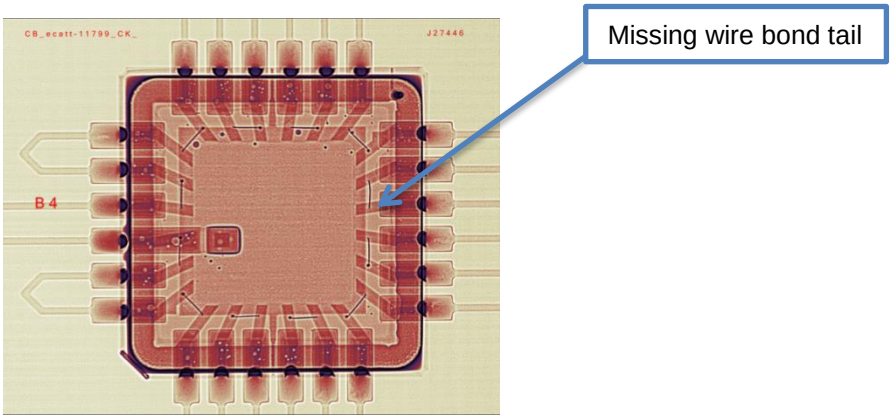

Figure 29. Missing tail on a wire bond.

For the 3LCC components, the most common manufacturing defects were curved wire bonds and voids along the housing. After inspecting the UUTs, there were no issues with any solder joints.

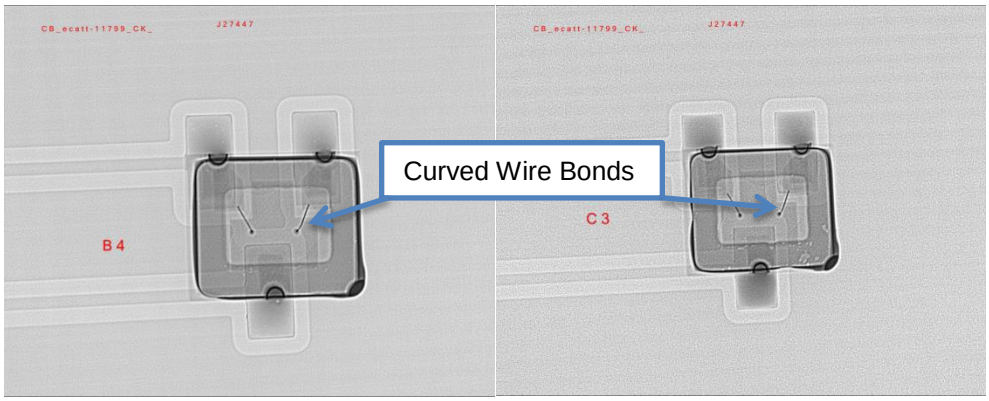

Figure 30. 3LCC curved wire bonds natural image (left) and Wallis filter (right)

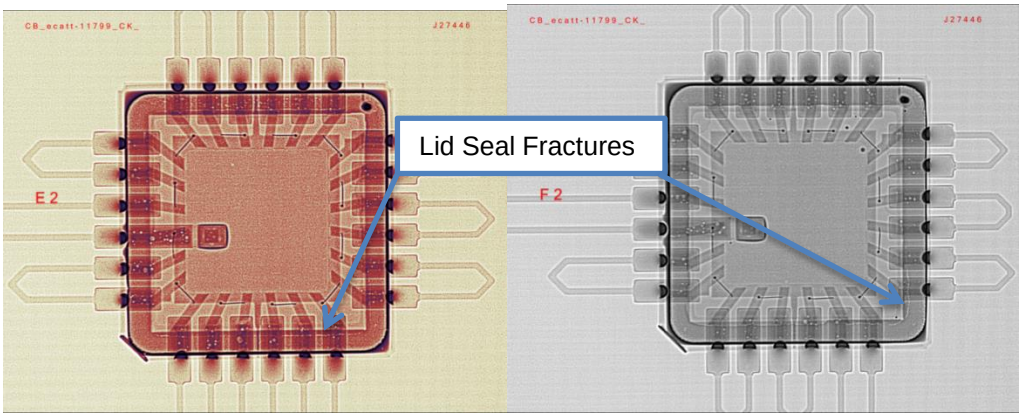

Figure 31. 24LCC Lid seal fractures red Wallis filter (left) and original Wallis filter (right)

Small fractures were also found on the lid seal on a few of the UUTs. These are also formed during component manufacturing and there was no abnormal behavior with the interconnect features upon initial inspection. Initial resistance values for each component are listed in table 5 and Table 6.

5	OL	2.21	2.21	2.25	2.24	2.35
4	2.16	2.15	2.15	2.1	2.18	2.37
3	2.06	1.94	2.16	2.12	2.18	2.27
2	2.01	2.09	2.07	2.08	2.13	2.15
1	1.94	1.91	1.94	2.08	2.1	2.2
	A	**B**	**C**	**D**	**E**	**F**

Table 5. 24LCC Initial Resistance

5	OL	0.84	0.85	0.86	0.97	0.97
4	0.72	0.71	0.71	0.79	0.81	0.85
3	0.64	0.67	0.66	0.73	0.76	0.77
2	0.54	0.59	0.65	0.62	0.67	0.72
1	0.49	0.47	0.7	0.56	0.57	0.61
	A	**B**	**C**	**D**	**E**	**F**

Table 6. 3LCC Initial Resistance

7.2 Ten Cycles

It was decided prior to testing that the test should be run in small increments to check for any subtle changes in the system. Due to the fact that the first noticeable number of cycles to failure was 22.2, the boards were inspected after 10 thermal cycles. After 10 cycles, the UUTs looked very similar to the initial x-ray scans. There were no voids that visually grew, even upon zooming in with the X-TEK. Wire bonds didn't change, and neither did the amount of FOD present. Due to the similarities, no x-ray images were saved, only a live inspection was performed. Resistance was also taken for each device and the values were also similar to the initial measurements.

5	OL	0.77	0.77	0.82	0.85	0.89
4	0.72	0.73	0.71	0.79	0.79	0.94
3	0.59	0.6	0.61	0.63	0.81	0.75
2	0.55	0.53	0.57	0.59	0.61	0.69
1	0.52	0.41	0.42	0.48	0.55	0.58
	A	**B**	**C**	**D**	**E**	**F**

Table 7. 3LCC Post 10 Cycles Resistance

5	OL	2.24	2.22	2.25	2.3	2.35
4	2.07	2.11	2.13	2.13	2.25	2.32
3	1.94	1.93	2.08	2.09	2.17	2.24
2	2.03	2.01	2.01	2.03	2.11	2.14
1	1.96	1.93	2.07	1.99	2.1	2.09
	A	**B**	**C**	**D**	**E**	**F**

Table 8. 24LCC Post 10 Cycles Resistance

7.3 Twenty Cycles

Thermal cycling was stopped right before the first theoretical number of cycles to failure at 22.2 for 24LCCs and 24.1 for 3LCCs. If there were any detectible changes or additional damage, there would be evidence of the UUTs behaving similar to the model of conformal coating in

between the device and the polyimide board. Extra time was taken investigating the 24LCC components. The packages were scanned live and screenshots were taken for any cases with evidence of any changes. The resistance changed only slightly compared to the post 10 cycle test.

5	OL	0.84	0.81	0.83	0.87	0.93
4	0.66	0.7	0.7	0.73	0.8	0.84
3	0.63	0.65	0.67	0.67	0.71	0.77
2	0.56	0.55	0.54	0.59	0.63	0.69
1	0.47	0.46	0.44	0.51	0.55	0.6
	A	**B**	**C**	**D**	**E**	**F**

Table 9. 3LCC Post 20 Cycles Resistance

5	OL	2.31	2.39	2.34	2.32	2.41
4	2.14	2.19	2.33	2.08	2.15	2.35
3	1.99	2	2.15	2.1	2.17	2.24
2	2.31	2.11	2.07	2.11	2.13	2.11
1	1.98	1.92	1.96	2.03	2.04	2.07
	A	**B**	**C**	**D**	**E**	**F**

Table 10. 24LCC Post 20 Cycles Resistance

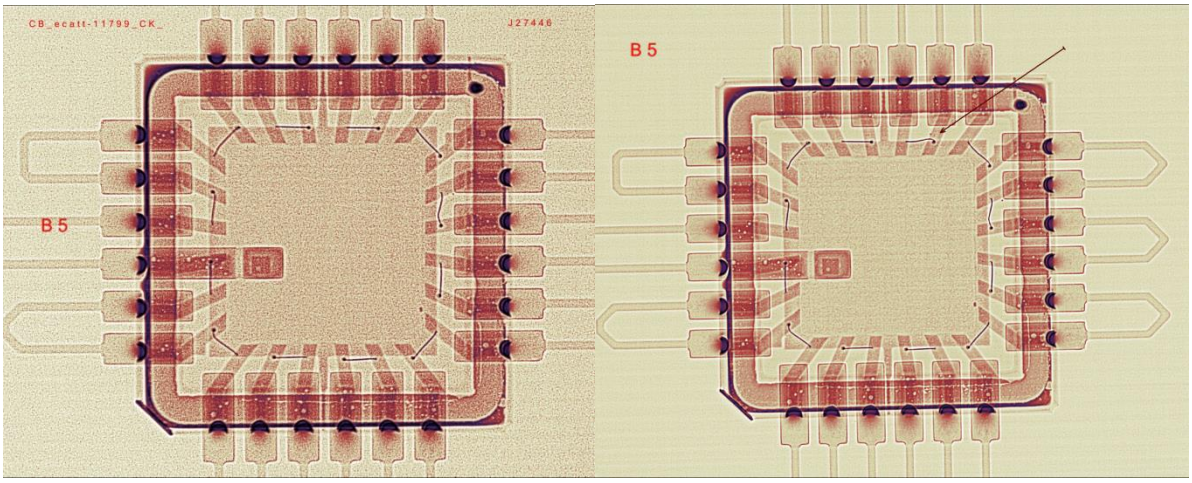

Figure 32. Curved Wire Bond on 24LCC component B4

After 20 complete cycles it was noticed that a wire bond on one of the 24LCC packages increased in curvature as shown in Figure 32. It was unusual because this device was part of the underfilled test specimens. The 3LCC components were drastically similar to the initial photos taken before testing. Evidence of this is displayed in Figure 33.

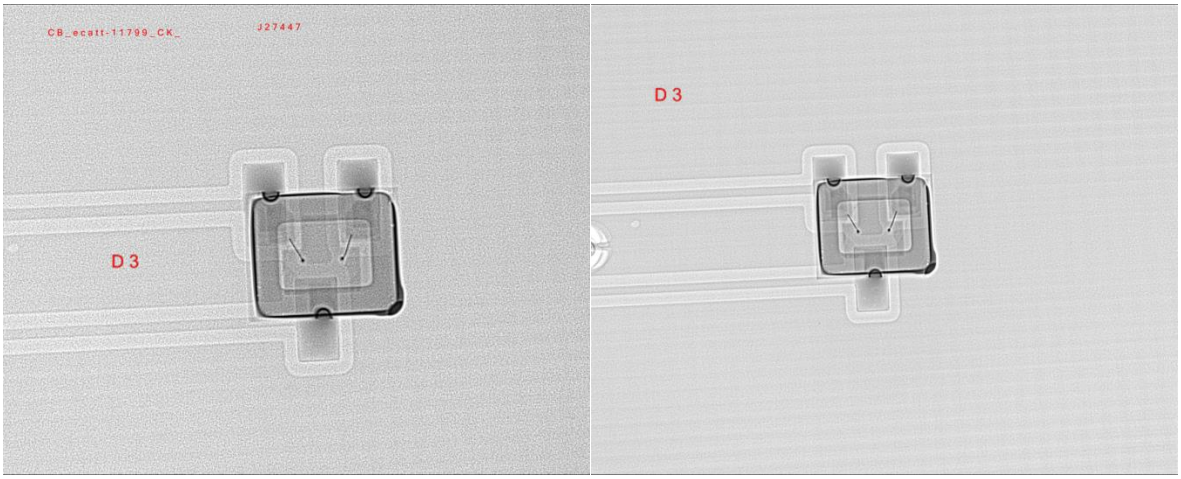

Figure 33. 3HSOT initial test (left) Post 20 cycle test (right)

7.4 Thirty Cycles

It was decided that another increment of 10 cycles would be done to surpass the first theoretical cycles to failure by 26% for 24LCCs and 13% for 3LCCs. There was no additional damage from any of the packages. Figure 34 shows package C5 with little to no change prior to testing to after 30 cycles. There was also no evidence of change for any of the 3LCC devices.

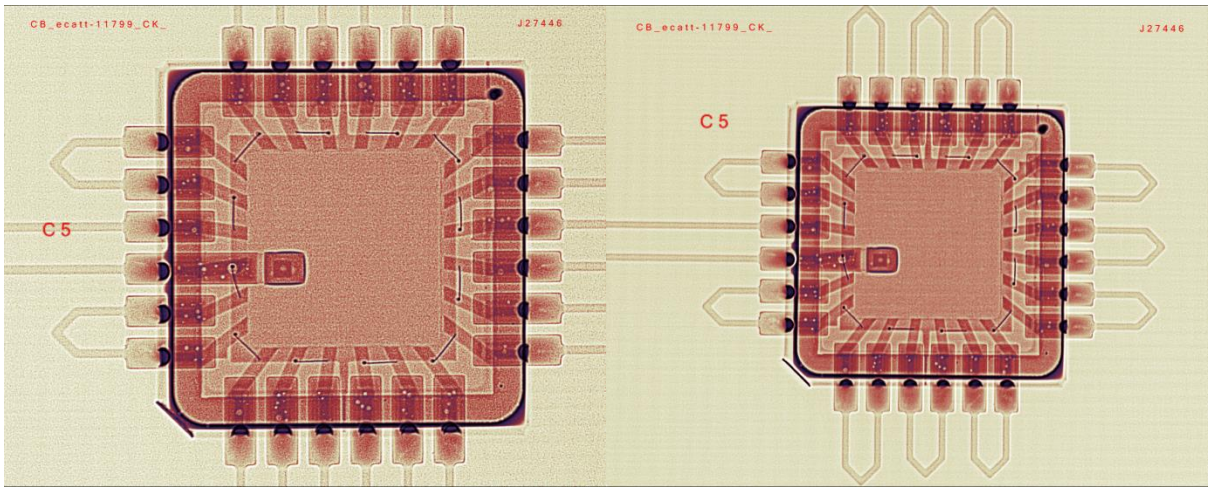

Figure 34. 24LCC initial x-ray scan (left) & post 30 cycles (right)

Resistance change was negligible compared to the previous measurements. It was concluded after the analysis after 30 temperature cycles that a model of conformal coating underneath the packages was inaccurate since the experimental data did not support the FEA data.

5	OL	0.74	0.81	0.81	0.88	0.93
4	0.68	0.65	0.73	0.76	0.81	0.87
3	0.5	0.6	0.62	0.67	0.73	0.74
2	0.53	0.49	0.6	0.61	0.65	0.68
1	0.47	0.42	0.47	0.5	0.56	0.6
	A	**B**	**C**	**D**	**E**	**F**

Table 11. 3LCC Post 30 Cycles Resistance

5	OL	2.2	2.21	2.23	2.28	2.35
4	2.12	2.14	2.15	2.09	2.14	2.32
3	1.94	2.01	2.11	2.13	2.18	2.22
2	1.98	2.02	2.06	2.06	2.12	2.11
1	1.92	1.92	1.95	2.03	2.06	2.07
	A	**B**	**C**	**D**	**E**	**F**

Table 12. 24LCC Post 30 Cycles Resistance

7.5 Sixty Cycles

The next phase of testing was to see evidence of change right up until the next failure mode. Since the FEA model of conformal coating above the device and a void underneath the component predicted cycles to failure 88.6 for 24LCCs and 457.6 for 3LCCs, it was decided to test and verify before that failure mode bringing the total number of cycles to 60. This was more significant for the 24 leadless packages. Up until 60 temperature cycles, no noticeable changes had been seen electrically or visually for most of the devices. The test took a total of 45.9 hours to run with the chamber running nonstop over the weekend.

5	OL	0.74	0.8	0.88	0.87	0.96
4	0.71	0.65	0.72	0.8	0.82	0.83
3	0.61	0.56	0.66	0.68	0.8	0.77
2	0.54	0.49	0.54	0.59	0.64	0.7
1	0.45	0.42	0.48	0.59	0.56	0.62
	A	**B**	**C**	**D**	**E**	**F**

Table 13. 3LCC Post 30 Cycles Resistance

5	OL	2.25	2.24	2.27	2.31	2.36
4	2.14	2.17	2.2	2.12	2.24	2.33
3	2.05	1.98	2.1	2.14	2.18	2.22
2	1.98	2.06	2.08	2.13	2.15	2.11
1	1.97	1.95	1.95	2.03	2.05	2.06
	A	**B**	**C**	**D**	**E**	**F**

Table 14. 24LCC Post 30 Cycles Resistance

Similar to the other test trails before it, there was no significant change in resistance measurements. The underfilled B4 24LCC unit that had initially shown increased curvature in one of the bond wires was also closely monitored for further damage and is compared below to the initial x-ray. As expected, the 3LCC packages showed no change due to not yet testing close enough to the next failure mode.

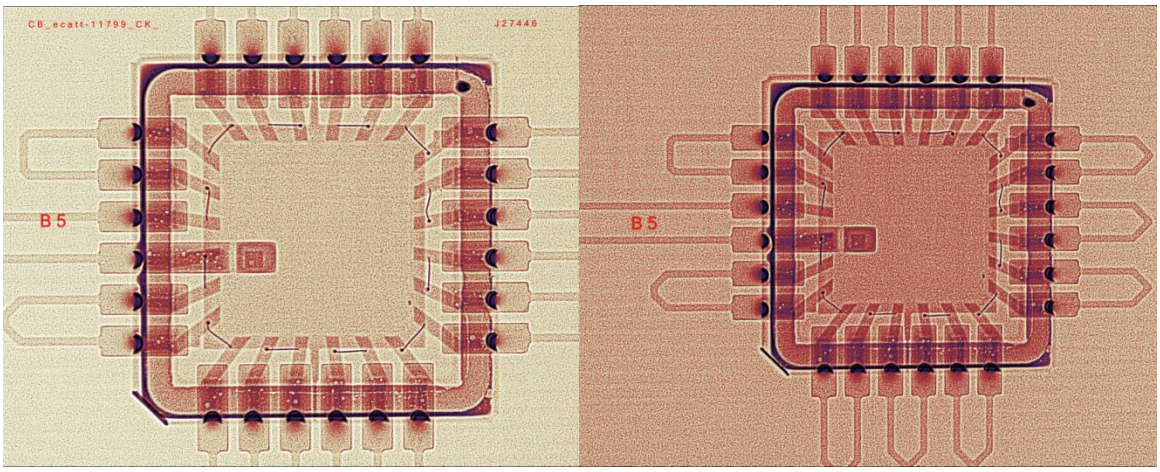

Figure 35. Component B5 24LCC initial testing (left) & post 60 cycles (right)

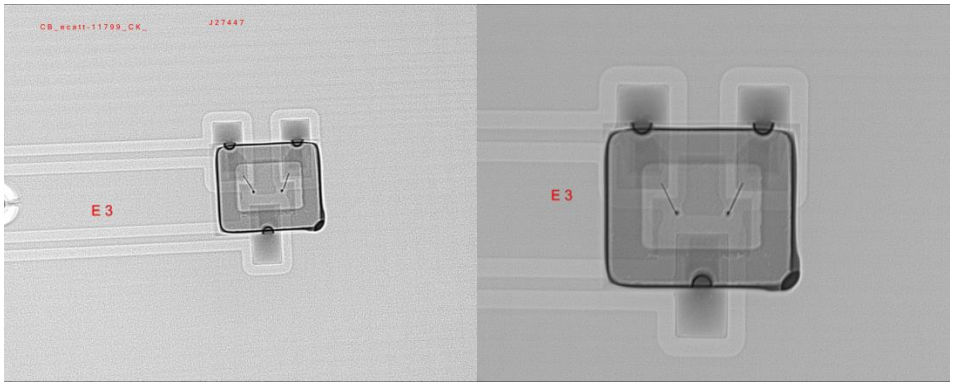

Figure 36. Component E3 3LCC initial testing (left) & post 60 cycles (right)

7.6 One Hundred and Ten Cycles

Thermal testing was then run for an additional 50 cycles bringing the total number of cycles tested to 110. The time allotted for 50 cycles was 3 days and 4.5 hours. The emphasis when performing post-test x-ray and continuity/resistance measurements was analyzing the 24LCC packages, because the 3LCC devices were still under the second failure scenario of 457.6 cycles to failure by 75%. The 24LCC UUTs were tested past the second failure mode with a margin of 19%.

5		0.77	0.8	0.87	0.93	0.99
4	0.72	0.69	0.74	0.79	0.82	0.85
3	0.57	0.61	0.65	0.71	0.77	0.77
2	0.53	0.52	0.57	0.64	0.65	0.72
1	0.45	0.44	0.5	0.58	0.57	0.62
	A	**B**	**C**	**D**	**E**	**F**

Table 15. 3LCC Post 110 Cycles Resistance

5	OL	2.27	2.28	2.23	2.24	2.38
4	2.19	2.22	2.17	2.1	2.16	2.36
3	2.03	1.98	2.13	2.1	2.16	2.27
2	2.15	2.03	2.09	2.09	2.19	2.16
1	1.99	1.94	1.94	2.01	2.06	2.11
	A	**B**	**C**	**D**	**E**	**F**

Table 16. 24LCC Post 110 Cycles Resistance

There was an interesting observation when x-raying one of the 24LCC UUTs. On component B2, on one of the lower pads indicated by the red arrow, the voids are more distinct after 110 cycles than the image taken prior to testing. The voids look as if they had come closer together.

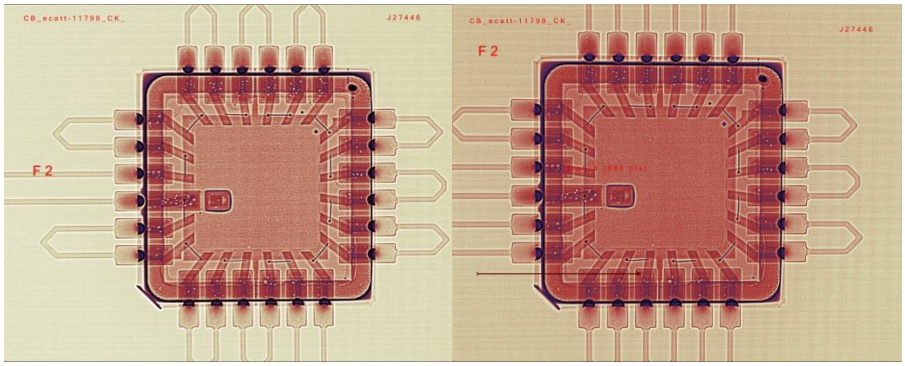

Figure 37. 24LCC component F2 void change in position before testing (left) to after 110 cycles (right)

A similar situation was observed for LCC unit B1. It can be seen that the void positioning and orientation is considerably different from zero cycles compared to 110 cycles. The smaller voids look to be moving closer to one another which could eventually combine and lead to fewer, larger voids.

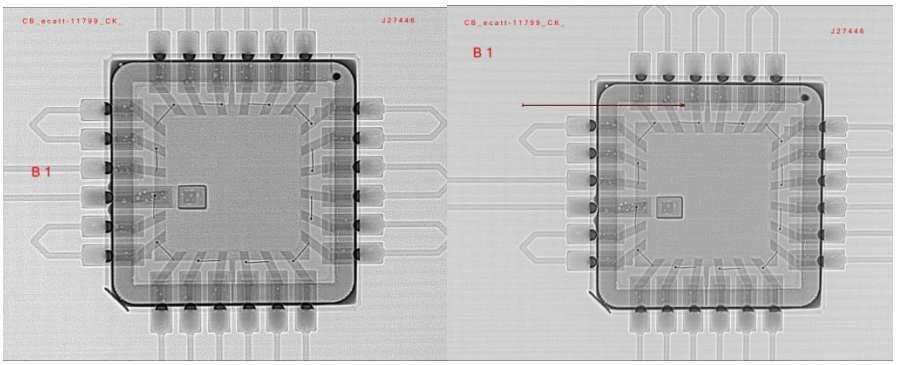

Figure 38. 24LCC component B1 before testing (left) to after 110 cycles (right)

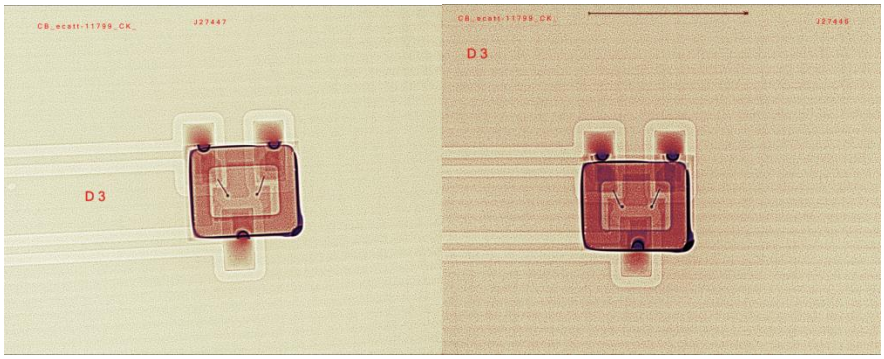

Figure 39. 3LCC component D3 before testing (left) to after 110 cycles (right) void formation

Again, the 3LCC UUTs remained similar to the results studied after 60 cycles. There were still a large number of cycles to be tested to get close enough to the conformal coat and void failure mode. For device D3, increase in void formations was observed near the left hand wall of the unit.

7.7 Two Hundred Cycles

Many of the units had little to no damage after 110 cycles were performed. To make use of additional time to test on nights and weekends, 90 more cycles were tested bringing the total number to 200. The test took 5 days, 17.6 hours to complete. Because of the remaining time for project submission and graduation deadlines, this was the last test performed. 200 cycles tested leads to a sense that the UUTs would be well on track to the 3rd and final failure mode for 24LCCs and about half way to the 2nd failure mode for 3LCCs.

5	OL	2.27	2.28	2.23	2.24	2.38
4	2.19	2.22	2.17	2.1	2.16	2.36
3	2.03	1.98	2.13	2.1	2.16	2.27
2	2.15	2.03	2.09	2.09	2.19	2.16
1	1.99	1.94	1.94	2.01	2.06	2.11
	A	**B**	**C**	**D**	**E**	**F**

Table 17. 3LCC Post 200 cycles resistance

5	OL	2.27	2.28	2.23	2.24	2.38
4	2.19	2.22	2.17	2.1	2.16	2.36
3	2.03	1.98	2.13	2.1	2.16	2.27
2	2.15	2.03	2.09	2.09	2.19	2.16
1	1.99	1.94	1.94	2.01	2.06	2.11
	A	**B**	**C**	**D**	**E**	**F**

Table 18. 24LCC Post 200 Cycles Resistance

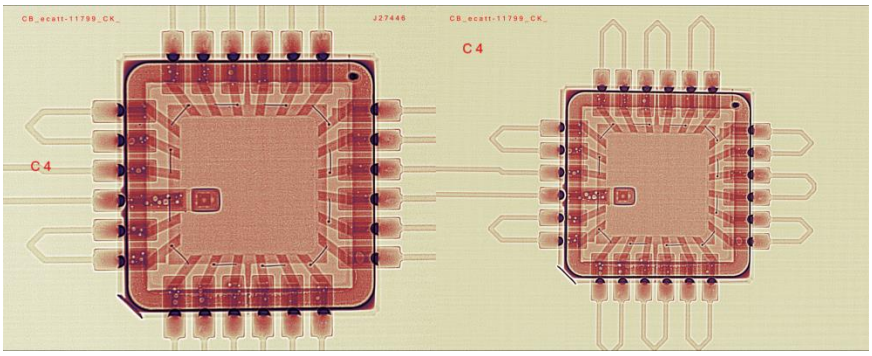

Figure 40. 24LCC UUT C4 before testing (right) and after 200 cycles (left)

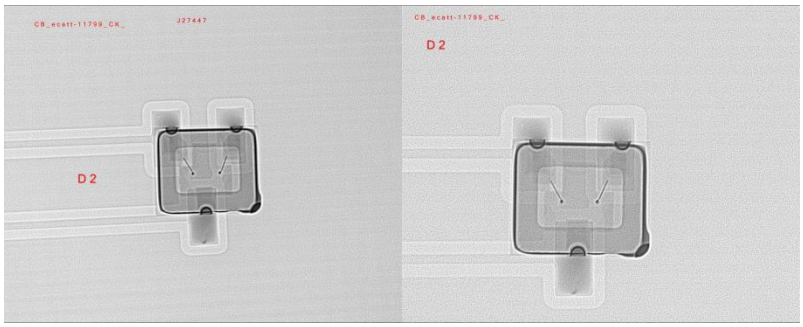

Figure 41. 3LCC component D2 before testing (right) and after 200 cycles (left)

X-raying and resistance measurements showed little to no change compared to 110 cycles and even 0 cycles for underfilled and not underfilled devices. 24LCC unit C4 and 3LCC unit D2 are examples of before and after images that show no noticeable damage.

Practicality and time were taken into consideration when deciding whether or not to perform more cycles. Theoretically the 24LCCs were 40% away from failure for an underfilled device and the 3LCCs still had more than twice the number of cycles needed to reach a failure for a device with a void underneath. All of the 24LCCs showed no to little damage whether or not they were underfilled. 3LCCs have 10% bottom surface of a 24LCC. The 3LCCs have a fewer number of contacts and can handle harsher environments compared to a 24LCC. With this knowledge, UUTs without underfill show and equivalent performance to UUTs with underfill.

Conclusion

Solder joint fatigue and ground pin connections are just a few examples of why thermal testing is so important today. Conformal coating can help protect the PCB from shock, vibration, humidity, and other harsh environments. However, it can pose a risk for the board and its components due to its high coefficient of thermal expansion. In this project, Arathane had a considerably higher CTE compared to other materials that composed of the other parts of the electronic assembly, such as 63SN37Pb solder, polyimide, and the LCC composite materials.

Having a large difference in CTE values can drastically affect the integrity of the solder connection mechanically and electrically. Voids can increase, cracks and fractures can form, which could lead to non-functional components in the circuit. There are many phenomena that take place in solder with large temperature fluctuations. Creep can be experienced if the temperature is held around 60% of the melting point. The materials can behave differently once the glass transition temperature is passed, and the solder exhibits different levels of stresses and strains as a function of distance away from the neutral plane. To help minimize the amount of damage a high CTE would have on a solder connection, underfill can be used. Almatis 20% is a common type of underfill for various types of surface mount packages. It has a relatively fast cure time, and is reliable. Adding underfill would also increase cost, turnaround time during the assembly phase, and might not be necessary if the environment is not harsh enough.

In manufacturing engineering, it can take a considerable amount of time to test the life of a product during the research and development phase. Acceleration testing is ideal for learning more about the product in a quick manner. FEA was performed on the solder failure of 3LCC and 24LCC devices for both daily use cycles and an accelerated profile. The daily use cycles to failure were in the hundreds of thousands and were not of every much significance from a component development stand point, and an acceleration profile was computed to increase the cycles to failure, making it easier to test. Three different scenarios were modeled. The first was Arathane above the package, and below which separates the device from the polyimide board, and makes contact with the solder. The second was a modeled scenario with conformal coating above the component, with a void between the component and board. The last analysis was similar with conformal coating on top, but had underfill added in between the board and package. The objective of this project was to experimentally verify the FEA data, and conclude which situation mostly resembled the actual assembly. To make the acceleration thermal profile a little more realistic, the temperature extremes were bounded by the glass transition temperature of the materials, and the ramp rate was increased to obtain more cycles in a shorter amount of time. Through a few acceleration factor equations, both acceleration profiles were very similar.

As found in the results, 3LCC and 24LCCs showed zero change in the first several cycles. Both packages did not match the first theory of 22 cycles to failure for 24LCCs and 24

cycles for 3LCCs. Both boards were analyzed before and after enough cycles were performed past the second scenario for 24LCCs at 88 cycles. While some small observations were noticed, mostly for 24LCCs, the majority again did not show any change. The UUTs were then tested to a total number of cycles of 200 and stopped due to time and practicality. While the 24LCCs had never made it to the 3rd stage, and the 3LCCs did not pass the second, testing showed that the devices without underfill were able to function without failure just as well as the devices with. The resistance showed no change across each test. This leads to the conclusion that underfill would not be necessary from a production and manufacturing standpoint, and the packages that are not underfilled will perform just as well as packages that are.

This project will help me in my engineering career as I plan to do other accelerated testing projects at an individual component level and at full assembly. There are several variables to account for and consider that overall test. Accelerated testing is an up and coming practice and there is much more to be understood in this field.

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Appendix

8.1 Matlab

```
% Acceleration Factor Calculations
clear,clc

t1_max = input('What is the test max temperature? (K)')
t1_min = input('What is the test min temperature? (K)')
time1 = input('What is the dwell time of the test?')
f1 = input('How many cycles per day?')

t2_max = input('What is the use max temperature? (K)')
t2_min = input('What is the use min temperature? (K)')
time2 = input('What is the dwell time of use?')
f2 = input('How many cycles per day?')

% Change in temperatures
dt2 = t2_max-t2_min;
dt1 = t1_max-t1_min;

% Dauksher Acceleration Factor Model
Dauksher = ((dt1/dt2)^1.75)*((time1/time2)^.25)*exp(1600*((1/t2_max)-
(1/t1_max)));

% Vasudevan Acceleration Factor Model
Vasudevan = ((dt1/dt2)^1.9)*((f1/f2)^.33)*exp(1414*((1/t2_max)-(1/t1_max)));

% Miremadi AF Model
%For a plastic ball grid array:
a = 1.26;
b = .02;
c = 3503;

Miremadi = ((dt1/dt2)^a)*((time1/time2)^b)*exp(c*((1/t2_max)-(1/t1_max)));

% Clech Acceleration Model
c1 =4.5654;
Clech = ((dt1/dt2)^2)*(((1-(c1*(dt1^-1)*(((time1^-
.19275)*exp(705.5/t1_min))+((time1^-.19275)*exp(705.5/t1_max))))))...
    /(1-(c1*(dt2^-1)*(((time2^-.19275)*exp(705.5/t2_min))+((time2^-
.19275)*exp(705.5/t2_max))))));

Z = (1-(c1*(dt2^-1)*(((time2^-.19275)*exp(705.5/t2_min))+((time2^-
.19275)*exp(705.5/t2_max)))));

% Coffin Manson
CM = (dt1/dt2)^.25;

N = f2^(1/3)
CM1 = (((t1_max-t1_min)/(t2_max-
t2_min))^1.9)*((90/20)^(1/3))*exp((.42/8.623*10-5)*(1/t2_max)*(1/t1_max))
```