Analysis of Circulating Harmonic Currents in Paralleled Three Level ANPC Inverters using SVM

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***Abstract*—In paralleled voltage source inverters (VSI), circulating current has both high frequency and low frequency components, and its spectrum highly depends on the modulation scheme. Previous research has mostly focused on the circulating current suppression for paralleled two-level VSIs. Little literature exists on similar analysis for paralleled three-level VSIs using space vector modulation. A detailed circulating current spectrum on full frequency range has not been well developed. This paper presents an improved analytical model for three-level space vector modulation (SVM), considering the impacts of regularly sampled reference and dead time. Then, circulating harmonic currents are determined across the full frequency range for various interleaving angles of two three-level ANPC inverters. The calculated harmonics are also verified by experimental results.**

Keywords—Space Vector Modulation, Parallel Three-level Inverters, Circulating Harmonics, Interleaving

I. INTRODUCTION

With the demand for higher power capability in a wide variety of power conversion applications, parallel operation of power electronics converters is gaining more attention especially with the limited power capabilities of commercially available semiconductor devices. In addition to increased power level, parallel operation of power electronics converters also gives reduced output harmonics [1], lower maintenance costs and improves system fault-tolerance capability and reliability [2]. However, when two voltage source converters are paralleled and share common dc/ac buses, a circulating loop due to unsynchronized switching action will result in undesired circulating current and consequently, lead to current distortion, increased device stress, and/or possible system failure. In such a system, there is no circulating current only when two paralleled converters are identically constructed and controlled with perfect synchronization, which is almost impossible to achieve in a practical implementation.

Fig. 1 shows the parallel connection of two three-level ANPC inverters, which is the studied topology in this paper. In fact, the analysis in the following sections is not only for three-level ANPC inverter, but also for other three-level voltage source inverters using space vector modulation. From Fig. 1, it is obvious that the direct cause of circulating current is V_{a1} unequal to V_{a2}, due to device parameter mismatches, imperfect synchronization and/or different switching sequence in two paralleled inverters.

To suppress or even eliminate circulating current, it is straightforward to use an isolated dc power supply and/or isolated transformer at the ac side to cut off the circulating path. However, they are quite bulky and expensive and significantly increase the size and cost of system.

Alternatively, other methods to suppress circulating current have been proposed in various research papers, and they can be categorized into two groups according to their control objectives. The first group deals with the low frequency circulating current by adjusting the placement of zero voltage vectors for SVM [3] or adding a zero-axis PI controller to conventional dq0 coordinate control for SPWM [4]. Many modified modulation schemes [5,6] are also proposed to reduce the difference of zero sequence voltages in paralleled converters.

The second group deals with the high frequency circulating current by inserting impedance in the circulating loop [7], for which a coupling inductor is usually preferred because it provides high loop impedance without significantly influencing the fundamental current. It is worth mentioning that the design of coupled inductor is highly related to converter topology and modulation scheme [8,9]. Only a few papers provide a detailed circulating current spectrum for full frequency range, which is important to both controller design and passive components design. In addition, when an interleaving technique is applied in paralleled converters, the system intrinsically has circulating current regardless of non-ideal factors. However, the relationship between circulating current and interleaving operation has been analyzed only for two-level voltage source inverters [10].

Furthering previous work in [13], which provided an analytical model for dc/ac side voltage spectrum of three-level VSI using space vector modulation, this paper improves the model considering the impacts of regularly sampled reference and dead time that are common in practical operation of power converters. Also, this paper presents the relationship between circulating harmonics currents and interleaving angle in two three-level VSIs operated in parallel. Simulation and

experimental results validate the improved analytical models, and the calculation of circulating harmonic currents at various interleaving angle.

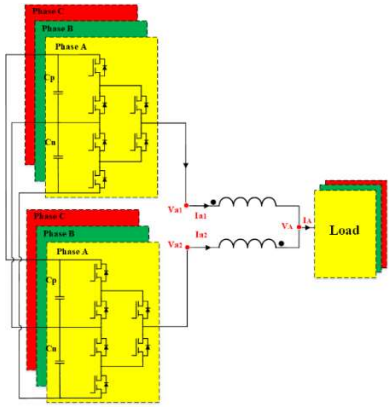


Fig. 1. Parallel connection of two three-level, three-phase ANPC inverters.

II. Analytical Calculation of Circulating Harmonics

A. Definition of Circulating Current

The circulating current is the undesired current that flows between two paralleled converters and does not flow to the load side, a common definition for circulating current in equal load sharing case is:

$$I_{cir\_x} = \frac{I_{x1} - I_{x2}}{2}, x = \{a, b, c\} \tag{1}$$

where I_{x1} and I_{x2} denote phase x output current of inverter 1 and inverter 2, respectively. Take phase A for example, as shown in Fig.1, they can be expressed by:

$$V_{a1} - V_A = L_s \frac{dI_{a1}}{dt} - L_m \frac{dI_{a2}}{dt} \tag{2}$$

$$V_{a2} - V_A = L_s \frac{dI_{a2}}{dt} - L_m \frac{dI_{a1}}{dt} \tag{3}$$

where V_{a1} and V_{a2} are phase A output voltage of inverter 1 and inverter 2, L_s and L_m are self-inductance and mutual inductance, they are assumed identical in inverter 1 and inverter 2. V_A is phase A common node voltage connected with load. Combining (1)~(3), the following expression for circulating current can be obtained:

$$V_{a1} - V_{a2} = 2(L_s + L_m) \frac{dI_{cir\_a}}{dt} \tag{4}$$

Eq. (4) discloses that the only excitation source for circulating current is phase voltage difference of inverter 1 and inverter 2. The difference can result from non-ideal factors (e.g. control delay and device threshold voltage difference), or different switching sequence (e.g. interleaving operation). If the harmonics spectrum of V_{a1} and V_{a2} can be calculated, the harmonics spectrum of I_{cir_a} can be easily obtained as well.

B. Analytical Model for Three Level SVM

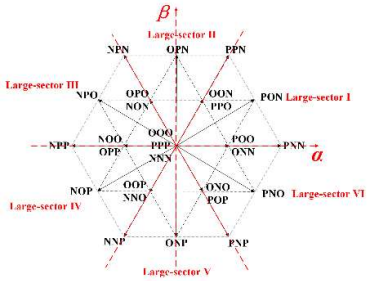
The complete analytical model for three-level SVM in all modulation index range is presented in [13]. To support and illustrate the model improvement considering regular sampling process and dead time, and calculation of circulating harmonic currents, the model is briefly presented here.

To calculate the harmonics spectrum of phase voltage, the starting point is the double Fourier series method presented in [11]. For any pulse width modulated phase leg, the voltage spectrum coefficient can be expressed in complex form:

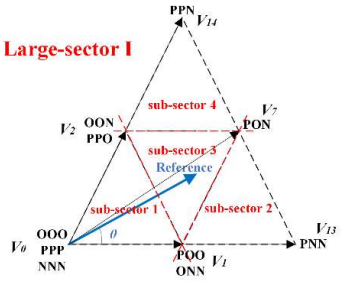
$$\overline{C_{mn}} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{y_s}^{y_e} \int_{x_r}^{x_f} f(x,y) e^{j(mx+ny)} dxdy \tag{5}$$

where $f(x,y)$ is output phase voltage, m and n are index for switching frequency band harmonics and fundamental frequency band harmonics, the inner and outer integral objects x and y represent the angle variation of switching frequency modulating wave and fundamental frequency modulated wave, respectively.

To solve (5), the key is to find the inner and outer integral limits x_r, x_f and y_s, y_e. Ref. [11] identified these limits for two level SVM by decomposing (5) into six sectors across a complete fundamental cycle, referring to the conventional sector division method. Compared with two level SVM which has 7 switching vectors (8 switching states), three level SVM has 19 switching vectors (27 switching states) in total and the sector division becomes more complicated, as shown in Table I and Fig. 2. More detailed introduction for three level SVM can be found in [12]. The modulation concept is the same for two level and three level SVM, that is using nearest three switching vectors to synthesize the reference vector. Therefore, the decomposing method in [11] can be extended to three level SVM. Following the switching vector definition and sector division in Table I and Fig. 2, here is the identifying process for the integral limits of (5) in large-sector I, similar derivation can be applied to other large-sectors.



(a)



(b)

Fig. 2. Sector division for three level SVM (a): large-sector division (b): sub-sector division for large sector I

Table I. Switching vector definition for three level SVM

Note: P,O,N represent that output terminal connects with positive, neutral, negtive DC bus (e.g, PON means $V_a = +V_{dc}, V_b = 0, V_c = -V_{dc}$)

Vector Classification	Switching States	Vector Magnitude
Zero vector:V_0	OOO;PPP;NNN	0
Small vector:$V_1, V_2, V_3, V_4, V_5, V_6$	POO/PNN;OON/PPO;OPO/NON NOO/OPP;OOP/NNO;ONO/POP	$\frac{2}{3}V_{dc}$
Medium vector: $V_7, V_8, V_9, V_{10}, V_{11}, V_{12}$	PON;OPN;NPO;NOP;ONP;PNO	$\frac{2\sqrt{3}}{3}V_{dc}$
Large vector: $V_{13}, V_{14}, V_{15}, V_{16}, V_{17}, V_{18}$	PNN;PPN;NPN;NPP;NNP;PNP	$\frac{4}{3}V_{dc}$
Reference vector:	---	MV_{dc} (M is modulation index)

As shown in Fig. 2(b), the reference vector locates in sub-sector 3 and the synthesizing vectors are V_1, V_2 and V_7. From volt-second balancing principle:

$$T_{sw}V_{ref}\cos\theta = T_1V_1 + T_2V_2\cos\frac{\pi}{3} + T_7V_7\cos\frac{\pi}{6} \quad (6)$$

$$T_{sw}V_{ref}\sin\theta = T_2V_2\sin\frac{\pi}{3} + T_7V_7\sin\frac{\pi}{6} \quad (7)$$

$$T_{sw} = T_1 + T_2 + T_7 \quad (8)$$

where T_{sw} is the switching period, T_1, T_2 and T_7 are dwell time for vectors V_1, V_2 and V_7, θ is the reference angle which is actually the integral object y and will be replaced with y in following derivation. Using the vector magnitudes from Table I, (6)~(8) can be solved:

$$T_1 = (1 - \sqrt{3}M\sin y)T_{sw}, \quad (9)$$

$$T_2 = \left(1 + \frac{\sqrt{3}}{2}M\sin y - \frac{3}{2}M\cos y\right)T_{sw} \quad (10)$$

$$T_7 = \left(\frac{\sqrt{3}}{2}M\sin y + \frac{3}{2}M\cos y - 1\right)T_{sw} \quad (11)$$

Based on conventional seven-segment placement for a centrally symmetrical switching sequence, the resulting output voltage waveform is shown in Fig. 3.

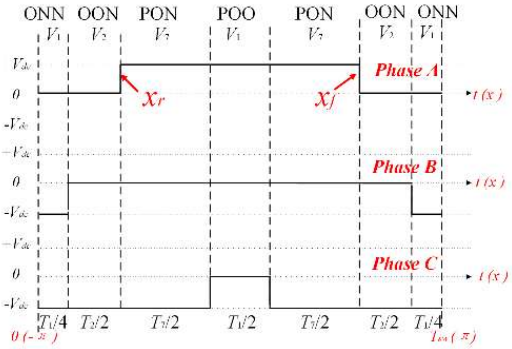


Fig. 3. Output phase voltage in sub-sector 3, large-sector I.

The label in Fig. 3 is in time domain which ranges from 0 to T_s, to fit with (5), it is remapped to angle domain, which ranges from – π to π. Again, take phase A as example, the rising edge angle and falling edge angle, x_r and x_f, can be calculated as:

$$x_r = -\pi\left(\frac{T_1}{2T_{sw}} + \frac{T_7}{T_{sw}}\right) = -\pi\left(\frac{3M\cos y}{2} - \frac{1}{2}\right), \quad (12)$$

$$x_f = \pi\left(\frac{T_1}{2T_{sw}} + \frac{T_7}{T_{sw}}\right) = \pi\left(\frac{3M\cos y}{2} - \frac{1}{2}\right) \quad (13)$$

$f(x, y)$ is zero when x is from $-\pi$ to x_r and x_f to π and consequently, the integration is non-zero only when x is from x_r to x_f. In other words, x_r and x_f are the lower and upper limits of inner integration of (5) for phase A output voltage. Similar analysis can be carried out to identify the limits in other sub-sectors of large-sector I, and for phase B and phase C. The results of phase A are shown in Table II.

Table II. Inner integral limits in large-sector I

Sub-sector	x_r	x_f	$f(x,y)$
1	$-\pi\left(\frac{3M\cos y}{4} - \frac{\sqrt{3}M\sin y}{4}\right)$	$\pi\left(\frac{3M\cos y}{4} - \frac{\sqrt{3}M\sin y}{4}\right)$	$+V_{dc}$
2	$-\pi\left(\frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})\right)$	$\pi\left(\frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})\right)$	$+V_{dc}$
3	$-\pi\left(\frac{3M\cos y}{2} - \frac{1}{2}\right)$	$\pi\left(\frac{3M\cos y}{2} - \frac{1}{2}\right)$	$+V_{dc}$
4	$-\pi\left(\frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})\right)$	$\pi\left(\frac{\sqrt{3}M}{2}\cos(y - \frac{\pi}{6})\right)$	$+V_{dc}$

The next step is to identify outer integral limits of (5), which is actually to identify the starting and ending points of each sub-sector. Furthermore, they are the interactions of reference vector trajectory and sub-sector boundaries. As shown in Fig. 4, the reference vector trajectory is a circle with radius M and the interactions are simple to calculate. Eq. (14) gives the solution (θ_1, θ_2) for $\frac{2}{3} < M < \frac{2\sqrt{3}}{3}$ (reference vector does not go to sub-sector 1). (θ_1, θ_2) for other modulation indexes can be calculated in a similar way.

$$\theta_1 = \frac{\pi}{3} - \sin^{-1}\frac{1}{\sqrt{3}M},\ \theta_2 = \sin^{-1}\frac{1}{\sqrt{3}M} \quad (14)$$

Hence, a complete integral limits identification of (5) in large-sector I is done, and the result is shown in Table III.

Applying the same process to other large-sectors, then a complete analytical solution for phase A output voltage can be obtained. Phase B and Phase C can be analyzed in the same way.

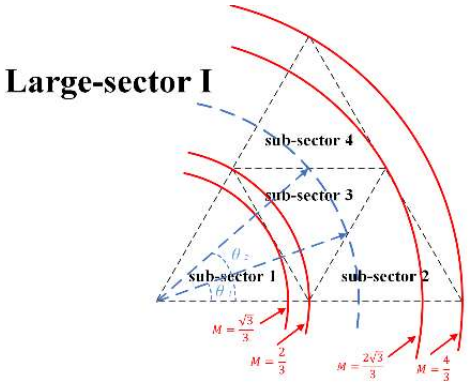


Fig. 4. Reference vector trajectory and sub-sector boundaries.

Table III. Outer and inner integral limits of Eq. (5) in large-sector I, for phase A, $\frac{2}{3} < M < \frac{2\sqrt{3}}{3}$

y_s	y_e	x_r	x_f	$f(x,y)$
0	θ_1	$-\pi\left(\frac{\sqrt{3}M}{2}\cos(y-\frac{\pi}{6})\right)$	$\pi\left(\frac{\sqrt{3}M}{2}\cos(y-\frac{\pi}{6})\right)$	$+V_{dc}$
θ_1	θ_2	$-\pi\left(\frac{3M\cos y}{2}-\frac{1}{2}\right)$	$\pi\left(\frac{3M\cos y}{2}-\frac{1}{2}\right)$	$+V_{dc}$
θ_2	$\frac{\pi}{3}$	$-\pi\left(\frac{\sqrt{3}M}{2}\cos(y-\frac{\pi}{6})\right)$	$\pi\left(\frac{\sqrt{3}M}{2}\cos(y-\frac{\pi}{6})\right)$	$+V_{dc}$

C. Modification to the Model

The assumption of the analysis in Section B is that the reference is an ideal three-phase sinusoidal wave, which means the variation of y is continuous across any fundamental cycle. However, it is not always true in a practical implementation. In most digital control systems for SVM modulated VSIs, the synthesizing space vectors are calculated once in each switching cycle, which means the reference angle keeps constant within one switching cycle. Hence, the variation of y is not necessarily continuous from 0 to 2π but a staircase from 0 to 2π, with stair number depending on the ratio of switching frequency and fundamental frequency, as shown in Fig. 5.

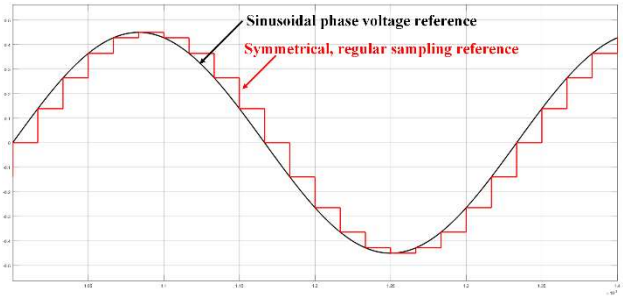
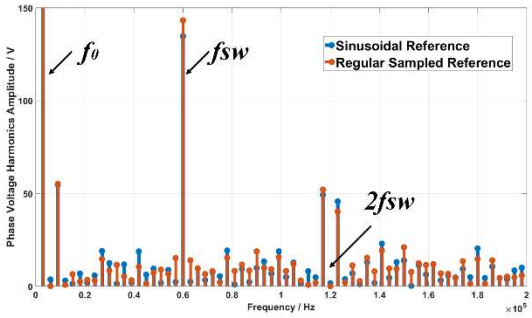
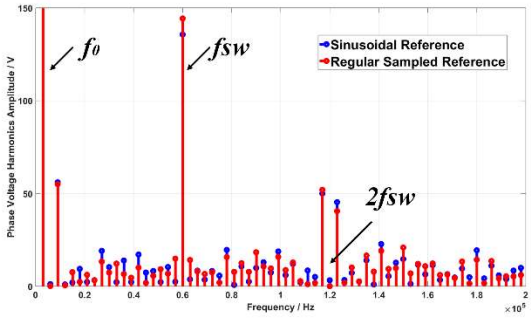


Fig. 5. Regular sampling process of phase voltage reference

In others words, SVM intrinsically is a regular sampled PWM strategy. Regular sampled PWM strategy can be further categorized to be symmetrical or asymmetrical. Symmetrical sampling is usually more common because it is easier for implementation, especially for modulations that require complex computation. Ref. [11] points out that for regular sampled PWM, the switching band index m in (5) should be replaced by $q = m + n\omega_0/\omega_{sw}$, where ω_0 and ω_{sw} are fundamental and switching angular frequency. Appling the modification to the model in Section B, Fig. 6 shows the calculation and simulation results. Be aware that the simulation parameters are identical with the experimental set up in Section III.



(a)



(b)

Fig. 6. Phase voltage harmonics spectrum with a sinusoidal reference and regular sampled reference. (a): Calculated results based on modified model. (b) Simulation results

As can be seen in Fig. 6, the replacement of factor q introduces small components in the fundamental frequency band of phase voltage spectrum, which agrees with the conclusion in [11]. For inverter paralleling, this may cause low frequency circulating current because the loop impedance is small at low frequency. Also, the regularly sampling process slightly distort the symmetry of the sidebands, with switching frequency sideband energy shifting between the lower and higher side band harmonics.

Another consideration is dead time. For a classical edge-delay based dead-time generation, the rising edge of each PWM signal is delayed for a certain time t_d. Therefore, the lower integral limit x_r in Table III should be modified to $x_r' = x_r + 2\pi\frac{t_d}{T_{sw}}$ when a dead-band is adopted. Fig. 7 shows the calculated results of the phase voltage harmonics spectrum with and without dead time. In fact, with setting a dead time of 500 ns (3% of switching cycle), the phase voltage harmonics do not change much but at the high frequency range. However, the impedance in the circulating loop is high because of the coupling inductor, which means the dead time will not introduce much extra circulating current.

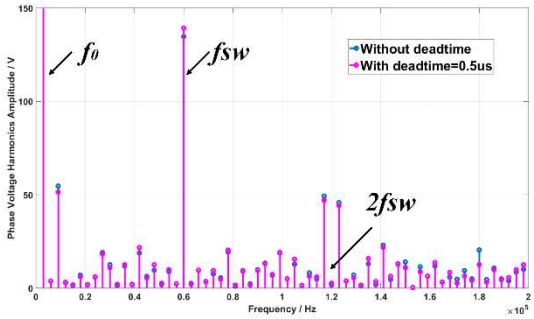


Fig. 7. Calculated phase voltage harmonics spectrum with and without dead time.

D. Impact of Interleave Angle

As aforementioned, the only excitation source for circulating harmonics is the difference of phase output voltage in paralleled VSIs. Interleave operation artificially introduces different switching sequence to inverter 2 if interleaved by angle θ, as the example ($\theta = 180°$) shown in Fig. 5. This consequently changes both the lower and upper limits of inner integration of (5). Considering the influence of dead time, the final integral limits for inverter 2's phase voltage spectrum calculation in large-sector I is given in Table IV. Then the circulating harmonics can be calculated with (4).

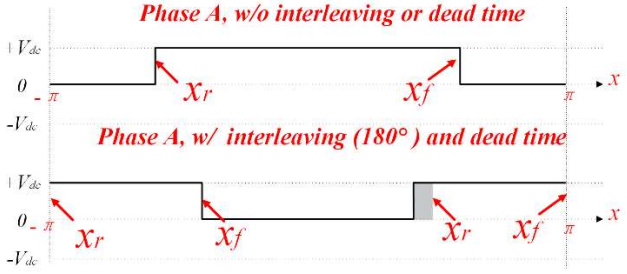
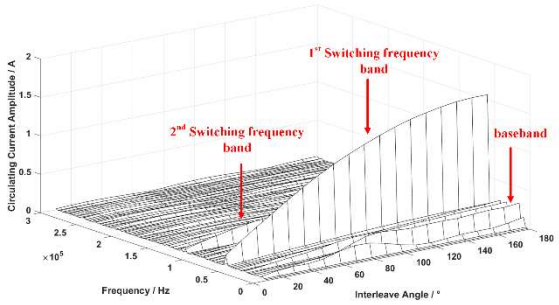


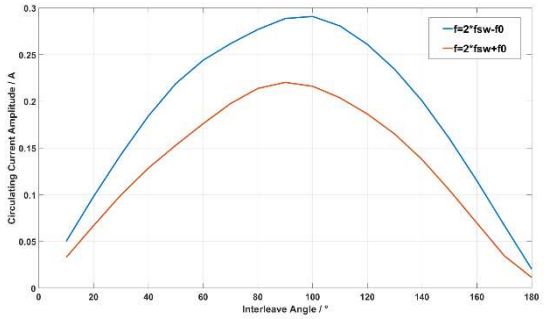
Fig. 5. Output phase A voltage of inverter 2(interleaved 180 °) in sub-sector 3, large-sector I.

Table IV. Integral limits for interleaving 180° with dead time, in large-sector I, for phase A, $\frac{2}{3} < M < \frac{2\sqrt{3}}{3}$

y_s	y_e	x_r	x_f	f
0	θ_1	$-\pi$	$-\pi\left(1-\frac{\sqrt{3}M}{2}\cos(y-\frac{\pi}{6})\right)$	$+V_{dc}$
		$\pi\left(1-\frac{\sqrt{3}M}{2}\cos\left(y-\frac{\pi}{6}\right)+\frac{t_d}{T_{sw}}\right)$	π	$+V_{dc}$
θ_1	θ_2	$-\pi$	$-\pi\left(-\frac{3M\cos y}{2}+\frac{3}{2}\right)$	$+V_{dc}$
		$\pi\left(-\frac{3M\cos y}{2}+\frac{3}{2}+\frac{t_d}{T_{sw}}\right)$	π	$+V_{dc}$
θ_2	$\frac{\pi}{3}$	$-\pi$	$-\pi\left(1-\frac{\sqrt{3}M}{2}\cos(y-\frac{\pi}{6})\right)$	$+V_{dc}$
		$\pi\left(1-\frac{\sqrt{3}M}{2}\cos(y-\frac{\pi}{6})+\frac{t_d}{T_{sw}}\right)$	π	$+V_{dc}$



(a)



(b)

Fig. 8. Circulating harmonic currents at various interleaving angle. (a): Across full frequency range (b) 2nd switching frequency band

Fig. 8 shows the calculated results of circulating harmonic currents at different frequency, as a function of interleaving angle. As shown in Fig. 8(a), the dominant components of circulating harmonic currents fall in the 1st and 2nd switching frequency band. The circulating current at switching frequency, reaches peak at 180° while the circulating current at 2nd switching frequency reaches peak at around 90°. There are also circulating current at fundamental frequency band, mainly due to the regular sampling process, and mixing with 1st switching band because of high ω_0/ω_{sw}.

III. Experimental Results

To validate the correctness of above derivation, a laboratory prototype with two paralleled three-level, three-phase ANPC inverters are constructed for experimental verification. Table V lists the key electrical parameters. The DC side input is +/-300 V and an RL load is used. In fact, according to the circulating current definition in Section II, the load condition will not effect the circulating current spectrum. The switching frequency is selected as 60 kHz while the fundamental frequency is 3 kHz. Coupling inductor has 190 uH self-inductance and 140 uH mutual inductance, to limit the circulating current amplitude to an acceptable range without saturating the cores.

Table V. Electrical parameters for experiments

V_{dc}	+/-300 V	M	0.9
f_0	3 kHz	f_{sw}	60 kHz
L_s	190 uH	L_m	140 uH
R_{load}	20 Ω	L_{load}	320 uH

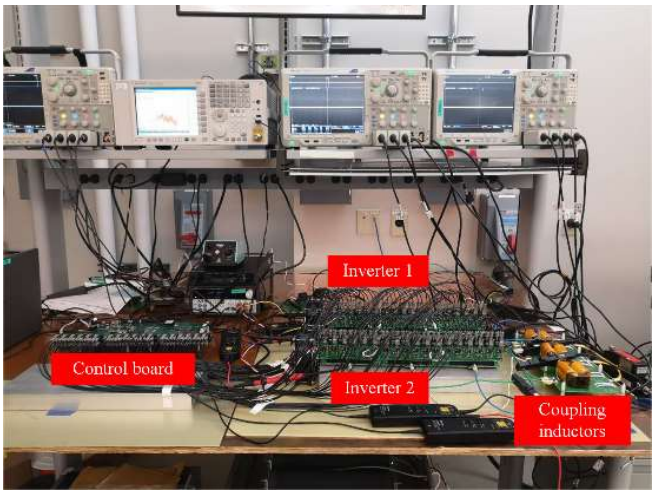
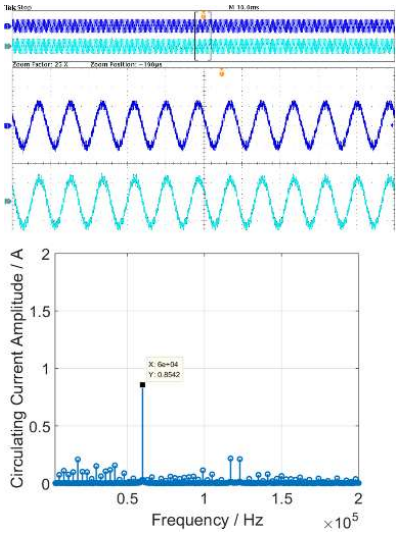
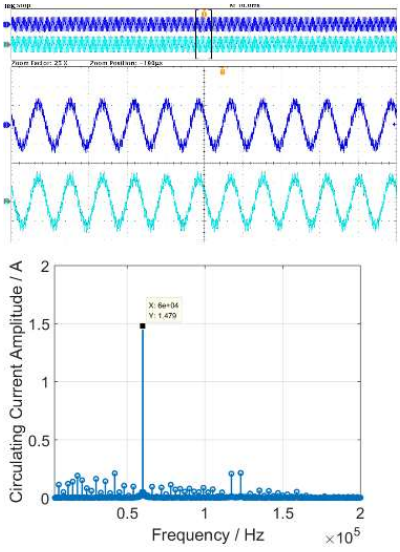


Fig. 9. Experimental set-up for parallel testing of two ANPC inverters.



(a)



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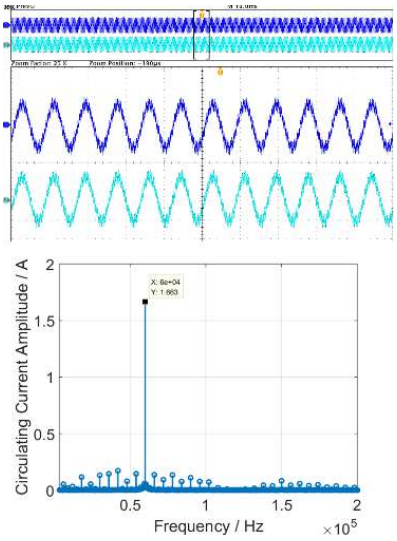

(c)

Fig. 10. Inverter 1 and Inverter 2 phase A current (5A/div); Circulating current calculated by (1) and its spectrum (a): 60° interleaving, (b): 120° interleaving, (c): 180° interleaving.

Fig. 9 shows the hardware platform. Two inverters are paralleled at interleaving angle of 60°, 120° and 180°. Then the measured phase currents are fed to (1) to obtain the circulating current. Tested results are shown in Fig. 10. It can be seen that circulating current not only includes high frequency components, but also some at fundamental frequency range, which agrees with the discussion in previous sections.

Table VI gives a comparison of calculated circulating current harmonics and experimental results, for the major components in first and second switching frequency band. The results in Table VI have shown a good agreement between tested and calculated harmonics, also a same relationship between interleaving angle and circulating current as discussed in Section II.

Table VI. Comparison of calculated circulating harmonics and experimental results

Harmonic / A	$\theta = 60°$		$\theta = 120°$		$\theta = 180°$	
	Cal.	Exp.	Cal.	Exp.	Cal.	Exp.
$f_{sw} - 2f_0$	0.070	0.066	0.126	0.109	0.204	0.127
f_{sw}	0.756	0.823	1.344	1.381	1.599	1.565
$f_{sw} + 2f_0$	0.075	0.046	0.126	0.079	0.110	0.133
$2f_{sw} - f_0$	0.243	0.244	0.254	0.261	0.02	0.02
$2f_{sw} + f_0$	0.194	0.176	0.276	0.187	0.022	0.01

IV. Conclusions

This paper analyzes the three-level SVM process and introduces an analytical model for circulating current harmonics calculation, in two paralleled three level voltage source inverters. Considering the influence of regular sampling process, the model is further modified for a more accurate calculation Using this model, results in Table VI have shown good

agreement for major components in 1st and 2nd switching frequency band, which are important to coupling inductor design.

In addition, the relationship between circulating current harmonics and interleaving angle is analytically calculated and demonstrated with experimental results. This relationship helps to select an optimal interleaving angle when designing a system with paralleled converters. Test results also validate previous discussion that the regular sampling process introduces circulating harmonics in the fundamental frequency band. In fact, due to the overlap of fundamental and switching frequency band (because of high ω_0/ω_{sw}), it becomes more difficult to accurately calculate low order circulating harmonics. Usually in high power applications, the ratio ω_0/ω_{sw} can be even higher than the set-up in this paper, due to low switching frequency. The future work will further discuss its impact on circulating harmonics.

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REFERENCES

[1] Miller, Stephanie KT, Troy Beechner, and Jian Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase VSCs," *IEEE Power Electronics Specialists Conference*, pp. 29-35, 2007.

[2] Yu, Xiaoxiao, and Ashwin M. Khambadkone, "Reliability analysis and cost optimization of parallel-inverter system," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3881-3889, 2012.

[3] Ye, Zhihong, Dushan Boroyevich, Jae-Young Choi, and Fred C. Lee, "Control of circulating current in two parallel three-phase boost rectifiers," *IEEE Transactions on Power Electronics* vol. 17, no. 5, pp. 609-615, 2002.

[4] Pan, Ching-Tsai, and Yi-Hung Liao, "Modeling and coordinate control of circulating currents in parallel three-phase boost rectifiers," *IEEE Transactions on Industrial Electronics* vol. 54, no. 2, pp. 825-838. 2007

[5] Li, K., Wang, X., Dong, Z., Wang, X., Guerrero, J.M., Vasquez, J.C. and Wang, Q, "Elimination of zero sequence circulating current between parallel operating three-level inverters," *IEEE Industrial Electronics Society Annual Conference,* pp. 2277-2282, Octorber, 2016.

[6] Zhu, Rongwu, Marco Liserre, Zhe Chen, and Xiaojie Wu, "Zero-Sequence Voltage Modulation Strategy for Multiparallel Converters Circulating Current Suppressio," *IEEE Transactions on Industrial Electronics,* vol. 64, no. 3, pp: 1841-1852,2017

[7] Cho, Un-Kwan, Jung-Sik Yim, and Seung-Ki Sul, "Parallel operation of PWM inverters for high speed motor drive system," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1561-1567. 2010.

[8] Gohil, Ghanshyamsinh, Lorand Bede, Remus Teodorescu, Tamas Kerekes, and Frede Blaabjerg, "Comparative evaluation of modulation schemes for grid-connected parallel interleaved inverters," *IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1-8. 2016.

[9] Zhang, Di, Fei Wang, Rolando Burgos, and Dushan Boroyevich, "Total flux minimization control for integrated inter-phase inductors in paralleled, interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Transactions on Power Electronics* vol. 27, no. 4, pp: 1679-1688. 2012.

[10] Xueguang, Zhang, Li Weiwei, Yi Xiao, Gaolin Wang, and Dian Guo Xu, "Analysis and Suppression of Circulating Current Caused by Carrier Phase Difference in Parallel Voltage Source Inverters with SVPWM," *IEEE Transactions on Power Electronics* 2018.

[11] Holmes, D. Grahame, and Thomas A. Lipo. *Pulse width modulation for power converters: principles and practice*. Vol. 18. John Wiley & Sons, 2003.

[12] Wu, Bin, and Mehdi Narimani. *High-power converters and AC drives*. Vol. 59. John Wiley & Sons, 2017

[13] R. Chen, J. Niu, H. Gui, Z. Zhang, F. Wang, Leon M. Tolbert, B. J. Blalock, D. J. Costinett and B. B. Choi, " Analytical analysis of AC and DC side armonics of three-lvel active neutral point clamped inverter with space vector modulation," *IEEE Applied Power Electronics Conference and Exposition*, 2019, in press