Investigation of Fourth-leg for Common-mode Noise Reduction in Three-level Neutral Point Clamped Inverter Fed Motor Drive

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***Abstract*—The four-leg topology has been applied to two-level inverters for common-mode (CM) noise elimination. To achieve zero common-mode voltage (CMV), the zero vector typically used in the two-level inverter is not allowed. As a result, the reference cannot be synthesized by nearest three vectors, which introduces a penalty in dc voltage utilization and current THD. This paper applies the fourth-leg to three-level neutral point clamped (NPC) inverter fed motor drives. Unlike the case in the two-level inverter, the reference can be synthesized by the nearest three vectors while zero CMV can be achieved at the same time in a three-level inverter with the fourth-leg. The topology and modulation are presented. The fourth-leg filter structures are investigated, and a fourth-leg filter structure which decouples the fourth-leg from the main circuit power level is proposed for high power applications. The experiment results on a three-level NPC inverter show that with the fourth-leg and presented modulation applied, the CM noise has been significantly reduced, and around 25 dB attenuation can be observed at the first noise peak in the electromagnetic interference (EMI) frequency range.**

Keywords—Three-level NPC converter; motor drive; fourth-leg; EMI noise.

I. INTRODUCTION

CM noise generated by the switching action of power semiconductor devices cause practical issues such as conducted and radiated emissions, bearing and leakage current for motor drive systems. To reduce the CM noise current in motor drive systems, extensive research work has been conducted. The traditional approach is to use passive CM filters. LC type filters are inserted into the power converter to block or bypass CM noise. However, passive filters are usually bulky and lossy, which significantly reduce the converter system efficiency and power density [1] - [2]. Other approaches include active filters involving transistors or amplifiers [3] - [4], pulse width modulation (PWM) techniques [5] - [10], and inverter topologies which reduce the CMV [11] – [19].

The fourth-leg topology was first used by Julian et al. [13] to reduce CMV and CM noise. A fourth-leg and a fourth phase LC filter are inserted into the two-level inverter. The zero vector is not used in the modulation to achieve zero CMV. Compared to two-level inverters, little attention has been paid to the fourth-leg for three-level inverters. An auxiliary leg is added to the NPC inverter to produce the compensating voltage for CMV reduction through a four-winding transformer in [17]. However, an additional dc source and a CM transformer are required. A multi-level fourth-arm circuitry is used and connected to the induction motor neutral point through an isolation capacitor to eliminate the bearing current in NPC inverter based motor drive in [18]. The CMV reduction of four-leg T-type grid-tied inverter is illustrated in [19]. However, the PWM method is carrier based, and the control strategy cannot achieve zero CMV.

Furthering previous research, this paper investigates the fourth-leg for CM noise reduction in three-level NPC inverter fed motor drives. Unlike the case in two-level inverters, the nearest three vectors can be maintained to synthesize the reference while achieving zero CMV in three-level inverters with the fourth-leg. The modulation scheme for the three-level inverter and the fourth-leg are illustrated. The fourth-leg connected filter structures are investigated and a fourth-leg filter structure is proposed for high power applications. A lab prototype is established for experiment verification.

II. FOURTH-LEG FOR CM NOISE REDUCTION IN THE THREE-LEVEL NPC INVERTER

A. Topology and Modulation

The three-level ANPC inverter with the fourth-leg topology is shown in Fig. 1. Similar to the two-level inverter illustrated in [13], the fourth-leg is connected to the three main phases through a fourth phase LC filter. To achieve zero CMV, the summation of the four phase-legs voltages should be zero as (1), and the fourth phase LC filter parameters should be identical to the three phase LC filter as (2).

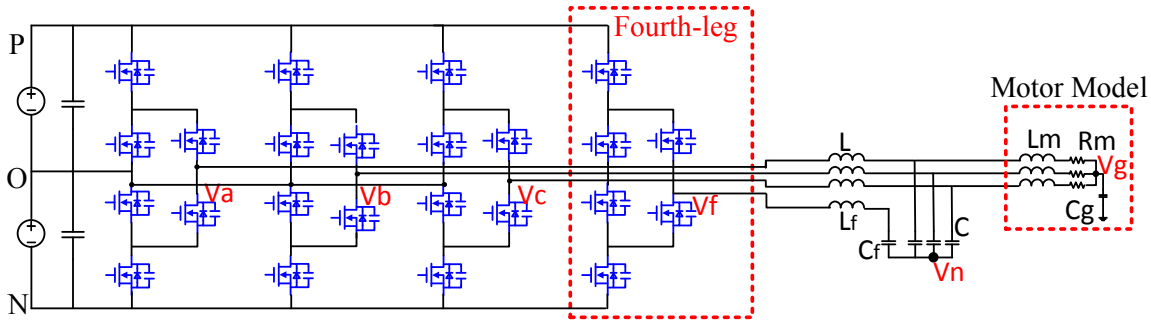


Fig. 1. Three-level ANPC inverter with the fourth-leg.

$$V_a + V_b + V_c + V_f = 0 \quad (1)$$

$$L_f = L, C_f = C \quad (2)$$

In a two-level inverter, when the zero vector - PPP and NNN as shown in Fig. 2 - are applied, a two-level fourth-leg output voltage, which only has two states P or N, cannot compensate the voltage summation of three phases and meet (1). However, the situation in the three-level inverter is different. Fig. 3(a) shows the space vectors for three-level SVM. There are 19 vectors (27 switching states), which are grouped into six large sectors. The small and zero vectors have redundant switching states. By appropriately selecting the redundant switching states, (1) can be met in all the sectors.

Fig. 3(b) shows the vector details of large sector 1. The space vector arrangement of large sector 1 for the three main phases and the fourth-leg are illustrated as shown in Fig. 4. The space vector arrangement of large sector 2 to large sector 6 are similar and will not be repeated here. In order to meet (1), the redundant switching state with lower CMV will always be selected (for example, POO is selected instead of ONN). Therefore, the modulation scheme of the three main phases is actually the same as the scheme illustrated in [9] for CMV reduction. Three nearest space vectors are used to synthesis the reference, and the max modulation index is the same as conventional SVM. One phase has no switching action in every switching circle, so the switching loss will be reduced compared to the conventional SVM. For the fourth-leg, it has four switching actions in every switching circle. The dwell time of vectors for the fourth-leg follows the three main phases. No extra calculation is need in the digital controller for the gating control of the fourth-leg.

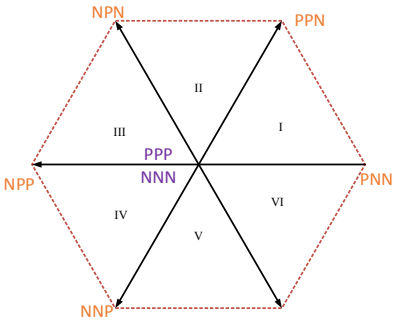
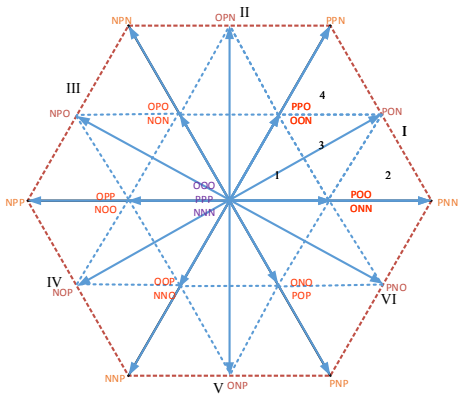
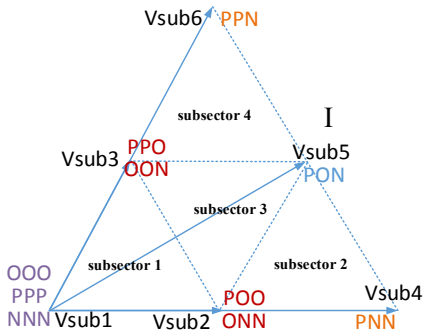


Fig. 2. Space vectors for a two-level inverter.

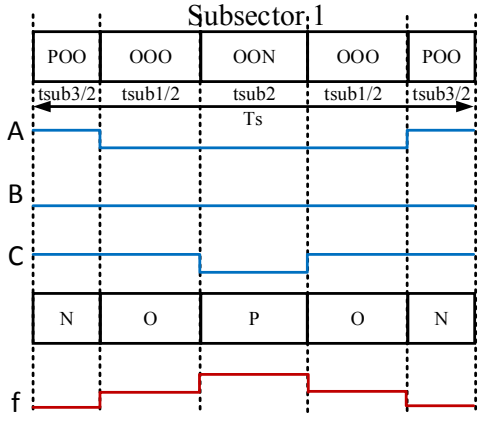


(a)



(b)

Fig. 3. (a) Space vectors a for three-level inverter, (b) vectors of large sector 1.



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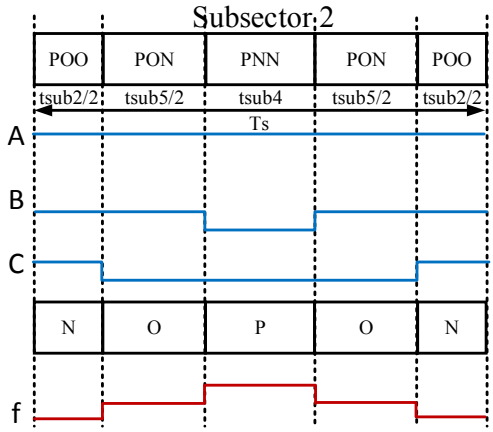

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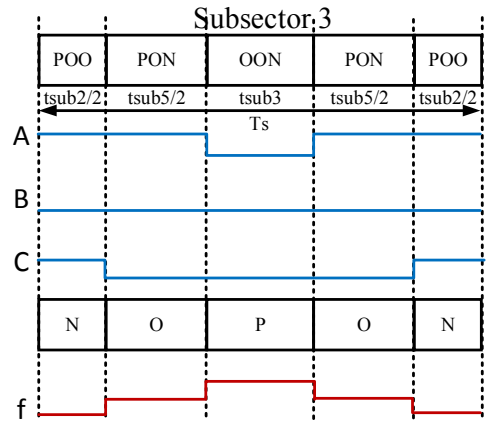

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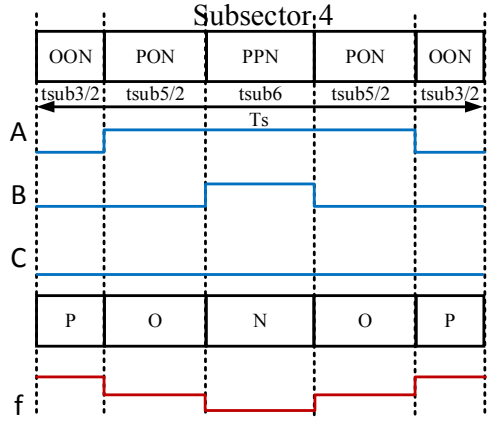


(d)

Fig. 4. Space vector arrangement for three main phase legs and the fourth-leg in large sector 1, (a) subsector 1, (b) subsector 2, (c) subsector 3, (d) subsector 4.

B. CM Noise Attenuation Performance Evaluation

The CM noise attenuation performance of the four-leg topology is investigated. With the fourth-leg added, based on the basic circuit theory, the transfer function from the motor neutral point voltage V_g to the fourth-leg output voltage V_f can be derived as (3).

$$
\begin{aligned}
G1 &= \frac{V_g}{V_f} = \frac{-4}{C_g}\frac{1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \\
b_4 &= 4LCL_m + 3CL^2 \\
b_3 &= 4R_m LC + 4RCL_m + 6RCL \\
b_2 &= 12LC / C_g + 4RCR_m + 4(L + L_m) + 3CR^2 \\
b_1 &= 12RC / C_g + 4(R + R_m) \\
b_0 &= 12 / C_g
\end{aligned}
\tag{3}
$$

Without the fourth-leg,

$$
\begin{aligned}
V_g &= \frac{V_a + V_b + V_c}{3} = \frac{-V_f}{3} \\
G2 &= \frac{V_g}{V_f} = -\frac{1}{3}
\end{aligned}
\tag{4}
$$

Hence, the insertion gain IG can be defined as

$$
IG = \left|\frac{G1}{G2}\right| = \frac{12}{C_g}\frac{1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{5}
$$

The insertion gain amplitude is plotted as shown in Fig. 5. In the EMI frequency range (150 kHz to 30 MHz), the amplitude of the insertion gain is significantly reduced, which means V_g and CM noise current will be significantly reduced when the fourth-leg is applied.

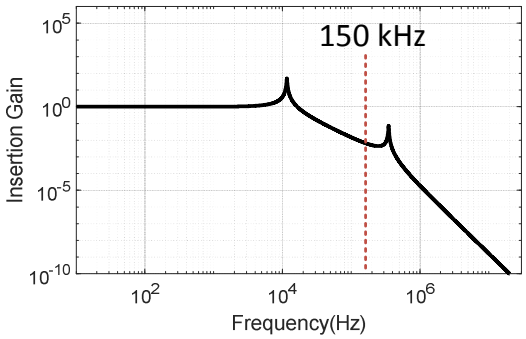


Fig. 5. Insertion gain amplitude versus frequency.

III. Investigation on Alternative Fourth-Leg Filter Structures

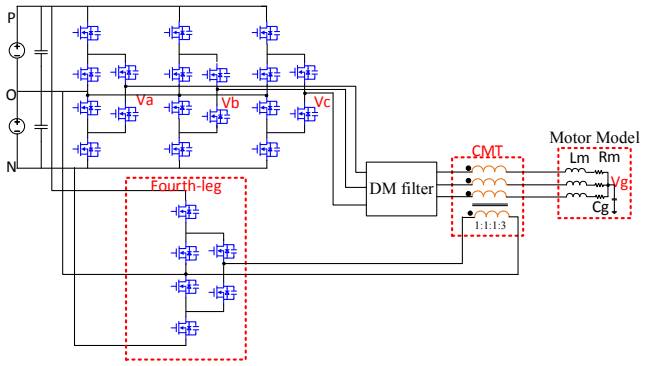
As discussed above, the fourth-leg of three-level NPC inverter can compensate the CMV generated by the three main phase legs. The voltage generated by the fourth-leg needs to be injected to the main circuit through a certain filter network.

The first fourth-leg filter structure considered is LC type differential-mode (DM) filter. As shown in Fig. 1, both the three main phase legs and the fourth-leg need a single stage LC filter to be connected together. The benefit of this filter structure is that it can make use of the DM filters existing in the main circuit when DM filters are necessary. For example, for motor drive in aircraft application, the inverter ac output is connected to the motor through long cables and needs to

meet DO-160 EMI standards. DM LC filters are required to suppress the DM EMI noise. Hence, the main circuit LC filters are not dedicated filters for the implementation of the fourth-leg circuitry.

However, two limitations exist with the DM filter structure. The first limitation is the limited DM filter type can be employed. For example, an LCL filter may be optimal for the three phase inverter DM noise reduction. But the fourth-leg is not able to be connected to the three main phase through a LCL filter. If the three main phases still use the LCL filters and the fourth-leg uses a LC filter, the CM noise reduction performance will be significantly reduced. The second limitation is that the fourth-leg is coupled with the main circuit power level. The fourth-leg filter parameters are exactly the same as the three main phase legs DM filters, which means that the current ripple of the fourth-leg is at the same level as the current ripple of the three main phases. For high power applications, the losses in the fourth-leg devices are high, and the size of the fourth-leg LC filter is large.

The second fourth-leg filter structure considered is a common-mode transformer (CMT). As shown in Fig. 6(a), the fourth-leg is connected to the main circuit through a CMT. Fig. 6(b) shows the simplified CM equivalent circuit. Compared to the first filter structure, this filter structure is independent of the main circuit DM filter structure. However, as the CMT is cascade in the main circuit, the fourth-leg is still coupled with the main circuit power level. Also, the CMT is complicated. For high power applications, the losses in the fourth-leg devices are high, and the size of the CMT is large.



(a)

(b)

Fig. 6. (a) Fourth-leg connected to three main phases through a CMT, (b) simplified CM equivalent circuit.

To decouple the fourth-leg from the main circuit power level, a filter structure is proposed as shown in Fig. 7. In Fig. 7(a), the voltage generated by the fourth-leg is connected to an impedance (R or RC, indicated by Z in Fig. 7) network. Point B is connected to the motor frame, which is usually grounded. Fig. 7(b) shows the CM equivalent circuit. When i_1 is much large than i_2, which can usually be satisfied as the CM current flowing through the motor is very small, voltage V_{BO} is almost one third of the voltage V_f generated by the fourth-leg. Then, the potential of point A and B is the same, no CM voltage is applied to the motor.

The fourth-leg with the impedance network is not directly connected to the main circuit, and the current of the fourth-leg is determined only by the impedance network. Hence, the proposed filter structure is independent of main circuit DM filter, and it decouples the fourth-leg from the main circuit power level. As the potential of point A and B is same as the ground and considered as zero, point O becomes a pulsating point, and a CM filter is needed in the dc side.

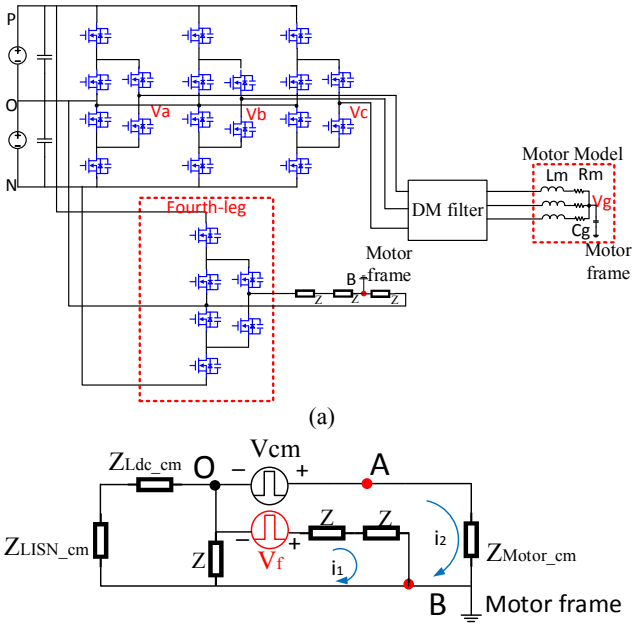


Fig. 7. (a) Proposed fourth-leg connected filter, (b) simplified CM equivalent circuit.

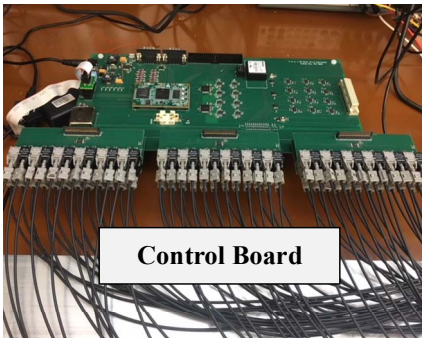
In conclusion, the first fourth-leg filter structure is suitable for a main circuit that DM filter exists and DM filter type can be implemented on the fourth-leg. The second fourth-leg filter structure can be employed to the main circuit where DM filter is not needed or DM filter type cannot be implemented on the fourth-leg. The proposed fourth-leg filter structure is independent of the main circuit DM filter and decouples the fourth-leg from the main circuit power level. Hence, it is suitable for high power applications. However, a CM filter in the dc side is required.

IV. Experiment Results

A SiC-based three-level ANPC inverter is constructed for experimental verification as shown in Fig. 8. The main parameters of the inverter are summarized in Table I.

Table I. Main parameters of the inverter.

DC input voltage	200V
Fundamental frequency	400 Hz
Carrier frequency	60 kHz
SiC MOSFETs	C3M0065100K
LC filters	L=390 uH, C=0.47 uF



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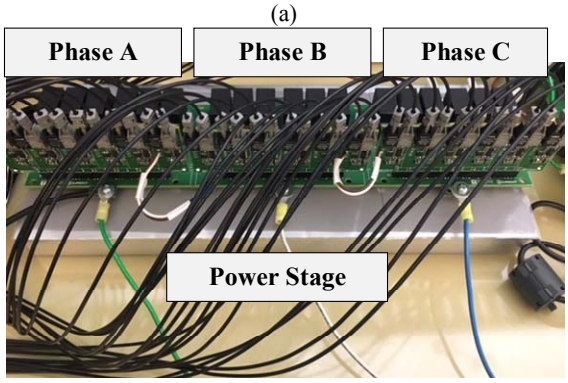

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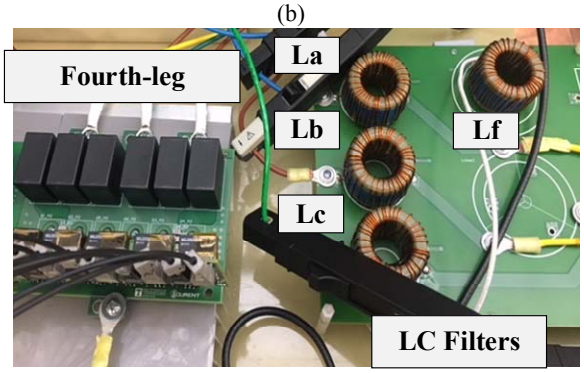


(c)

Fig. 8. The three-level ANPC inverter, (a) control board, (b) three phase main circuit, (c) fourth-leg and filters.

Fig. 9 shows the three-level ANPC inverter output line to line voltage and three phase currents, which is the operating point for EMI noise test.

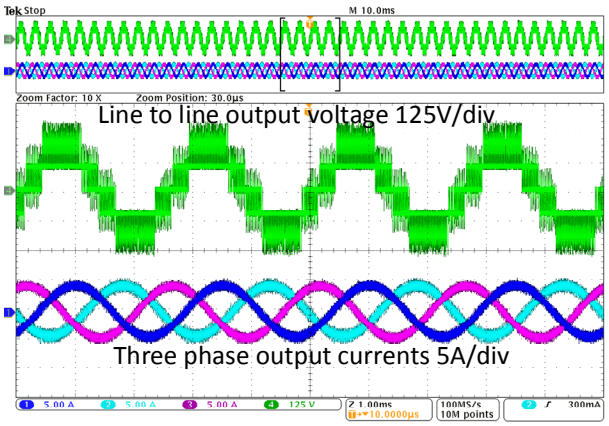
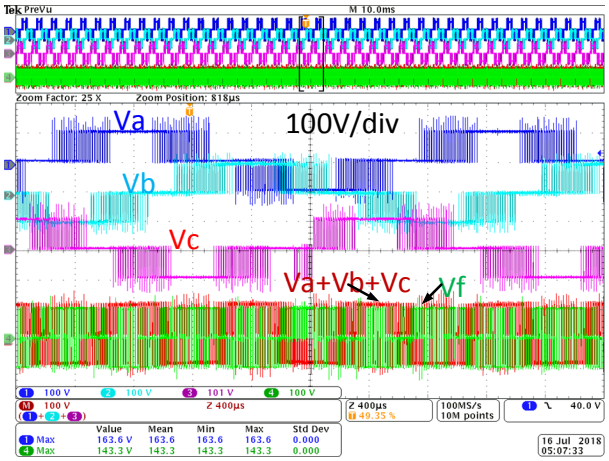
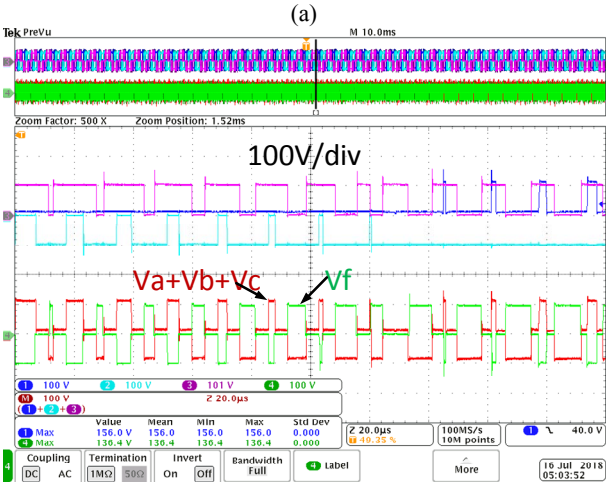


Fig. 9. Inverter output line to line voltage and three phases currents.

Fig. 10(a) shows the three phase output voltages Va, Vb, Vc, their summation $Va+Vb+Vc$, and the fourth-leg output voltage Vf. Fig. 10(b) is the zoom in waveforms. From Fig. 10(b), the voltage of the fourth-leg cancels out with the three phase voltages summation, so (1) is met.



(a)



(b)

Fig. 10. (a) Three phase output voltage, their summation, and the fourth-leg output voltage, (b) zoom in waveforms.

The comparison between the measured CM EMI noise without the fourth-leg and with the fourth-leg are shown in Fig. 11. It can be observed that the CM noise is significantly reduced with the fourth-leg applied. Specifically, at the first noise peak (3rd carrier harmonic, 180 kHz) in the EMI frequency range, the CM noise has been reduced by ~25 dB. In the ideal case, the CM noise current will be eliminated. However, as can be observed in Fig. 10(b), the rising/falling edge of the fourth-leg does not exactly overlap with the falling/rising edge of the three phase voltage summation. More accurate gate signal tuning method can be considered to improve the CM noise attenuation performance.

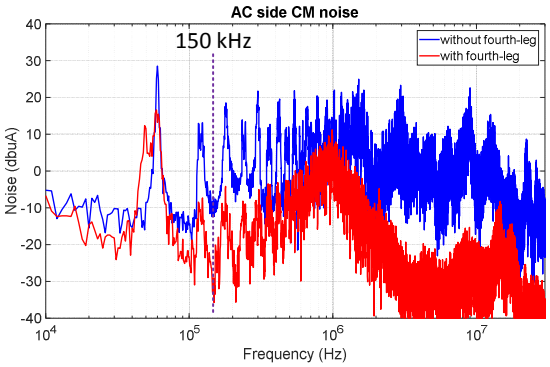


Fig. 11. Tested CM noise comparison w/ and w/o the fourth-leg.

V. Conclusion

This paper applies fourth-leg to the three-level NPC inverter fed motor drive for CM noise reduction. Unlike the case in two-level inverters, the nearest three vectors can be maintained to synthesize the reference while zero CMV can be achieved at the same time in the three-level inverter with fourth-leg by appropriately selecting the redundant space vectors. Alternative fourth-leg filter structures are investigated. A fourth-leg filter structure is proposed for high power applications which decouples the fourth-leg from the main circuit power level. The drawback of the filter structure is that a CM filter is required in the dc side.

Experiments conducted on a three-level ANPC inverter show that with the fourth-leg and presented modulation scheme applied, the CM noise has been significantly reduced, and ~25 dB attenuation can be observed at the first noise peak in the EMI frequency range. For future work, more accurate gate signal tuning method of the fourth-leg can be considered to improve the CM noise attenuation performance. More investigation on the fourth-leg filter structures can be conducted.

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