Coupled Inductor Design for Interleaved Three-level Active Neutral Point Clamped Inverters Considering EMI Noise Reduction

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***Abstract*—This paper presents the coupled inductor design for interleaved three-level active neutral point clamped (ANPC) inverter considering electromagnetic interference (EMI) noise reduction. Compared to two-level case, the scenarios involved in the three-level space vector modulation (SVM) are more complicated when analyzing the volt-seconds of the coupled inductor for paralleled three-level inverter. At system level, the purpose of converter interleaving is to reduce EMI noise and ripple current in most applications, and coupled inductor design should consider the needs of EMI noise reduction and EMI filter design. These issues are discussed in this paper. The relationship between circulating current and EMI noise is illustrated. EMI filter corner frequency as a function of interleaving angle is analytically derived, and optimal interleaving angle for maximum common-mode (CM) filter and differential-mode (DM) filter corner frequencies is discussed. Coupled inductor design methodology for interleaved three-level inverters with SVM is then presented. Experiments on two interleaved ANPC inverters are conducted. The results verify the coupled inductor design. With the derived optimal interleaving angle, the CM and DM EMI noise are significantly reduced.**

Keywords—Three-level NPC converter; paralleled inverters; coupled inductor; interleaving angle; EMI noise.

I. INTRODUCTION

Paralleling converters allows higher power rating or an increase in system reliability. Moreover, by shifting the phase angle of the carriers used for pulse width modulation (PWM) in paralleled inverters, the switching frequency related harmonics can be reduced, as a result, the size and weight of passive components such as the dc-link capacitors and EMI filters can be reduced [1] - [3].

However, interleaving also produces output voltage difference among paralleled inverters. Interphase inductors are needed to suppress the circulating current. Coupled inductors (CI), common-mode inductors (CMI), and differential-mode inductors (DMI) are used to suppress high frequency circulating current in two-level inverters [4] - [13]. A PWM scheme adding an optimal CM offset to the reference signal to reduce the flux linkage in the CI is proposed in [8]. A control method to minimize the total flux in the interphase inductor for paralleled inverters with discontinuous PWM is presented in [10]. The interphase inductor integration is discussed for different applications such as rectifiers [2], motor drives [12], and grid-tied inverters [13].

In prior work, however, the coupled inductor design are mainly for two-level converters. Compared to two-level converters, the scenarios involved in three-level converters with SVM are more complicated. The design of the coupled inductor for paralleled three-level ANPC inverters has not been discussed. Moreover, most prior work focus only on circulating current reduction, especially the zero sequence circulating current (ZSCC) reduction. However, at the system level, the purpose of interleaving is to reduce EMI noise and ripple current. The PWM scheme, interleaving angle, coupled inductor electrical and physical design should consider the needs of EMI noise reduction and EMI filter design, which has not been fully developed.

Furthering previous research, this paper presents the coupled inductor design for interleaved three-level ANPC inverters considering EMI noise reduction. The relationship between EMI noise and circulating current are illustrated. Optimal interleaving angle for maximum CM filter and DM filter corner frequency is analyzed. Coupled inductor design methodology for paralleled three-level ANPC inverters is presented. The maximum volt-second, ripple current selection, and physical design of the coupled inductor are discussed. Experimental verification is provided.

II. IMPACT OF INTERLEAVING ON EMI NOISE AND EMI FILTER

A. Relationship between Circulating Current and EMI Noise

For N paralleled inverters, assume symmetric interleaving is applied so the interleave angle $\gamma = 2\pi(k-1)/N, (k = 1, \dots, N)$, the phase output voltage of inverter k can be expressed as (1) [14].

$$V_{AN,k}=\frac{V_{dc}}{2}M\cos(\omega_0 t)+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{mn}\cos(m(\omega_c t+\frac{2\pi(k-1)}{N})+n\omega_0 t) \quad (1)$$

where m and n are the carrier and baseband integer indices, respectively. The modulation index is M, the harmonic coefficient is C_{mn}, ω_c and ω_0 represent the carrier angular frequency and the fundamental angular frequency, respectively. The phase output voltage of N interleaved inverters is described as (2), the summations are non-zero only if m is equal to N or its multiples.

$$V_{AN}=\frac{1}{N}\sum_{k=1}^{N}V_{AN,k}=$$
$$\begin{cases}\frac{V_{dc}}{2}M\cos(\omega_0 t)+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{mn}\cos(m\omega_c t+n\omega_0 t),(\forall m=kN,k=1,...\infty)\\ 0,(\forall others)\end{cases} \quad (2)$$

The CM voltage of inverter k can be expressed as (3). It is non-zero only if n is a triple multiple of an integer.

$$V_{CM,K}=\frac{1}{3}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{mn}\cos(m(\omega_c t+\frac{2\pi(k-1)}{N})+n\omega_0 t)(1+2\cos(n\frac{2\pi}{3}))=$$
$$\begin{cases}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{mn}\cos(m(\omega_c t+\frac{2\pi(k-1)}{N})+n\omega_0 t),(\forall n=3k,k=1,...\infty)\\ 0,(\forall others)\end{cases} \quad (3)$$

The CM voltage of N interleaved inverters can be described as (4), it is non-zero only if m is equal to N or its multiples and n is a triple multiple of an integer.

$$V_{CM}=\frac{1}{N}\sum_{k=1}^{N}V_{CM,k}=$$
$$\begin{cases}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{mn}\cos(m\omega_c t+n\omega_0 t),(\forall n=3k,m=kN,k=1,...,\infty)\\ 0,(\forall others)\end{cases} \quad (4)$$

The DM voltage of inverter k and N interleaved inverters can be determined as (5).

$$V_{DM,k}=V_{AN,k}-V_{CM,k},V_{DM}=\frac{1}{N}\sum_{k=1}^{\infty}(V_{AN,k}-V_{CM,k})=V_{AN}-V_{CM} \quad (5)$$

To visualize the equations above, Fig. 1 draws the spectrum of phase output voltage spectrum of a single inverter, and two interleaved inverters. The carrier frequency and fundamental frequency are 70 kHz and 3 kHz, respectively. The CM and DM components are indicated. According to Fig. 1, some conclusions can be made: (1) Compared to the phase output voltage spectrum of a single inverter, the output voltage of two interleaved inverters only have the second and second-multiples of carrier frequency components. Other harmonics actually convert to circulating components. Therefore, interleaving does not eliminate any harmonic, but it converts certain harmonics from the output into circulating components, and as a result, the output EMI noise and ripple current are reduced. (2) The circulating current has both the CM and DM components, and considering only the zero sequence circulating current in the coupled inductor design is not sufficient.

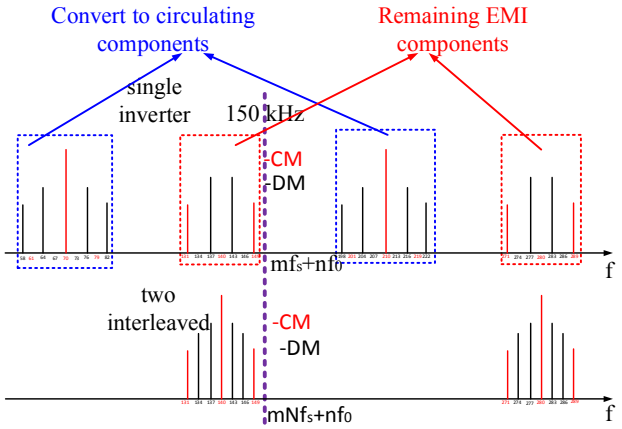


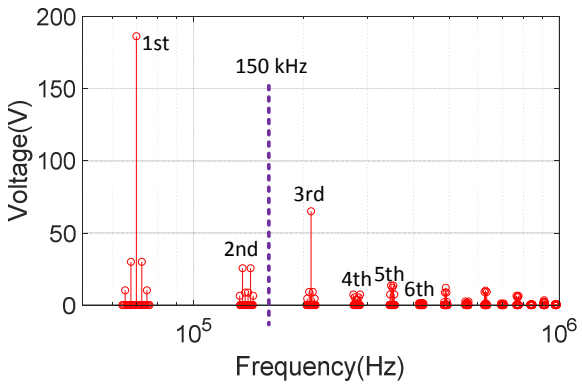
Fig. 1. Output voltage of a single inverter, and two interleaved inverters.

B. Optimal Interleaving Angle for Maximum CM and DM Filter Corner Frequency

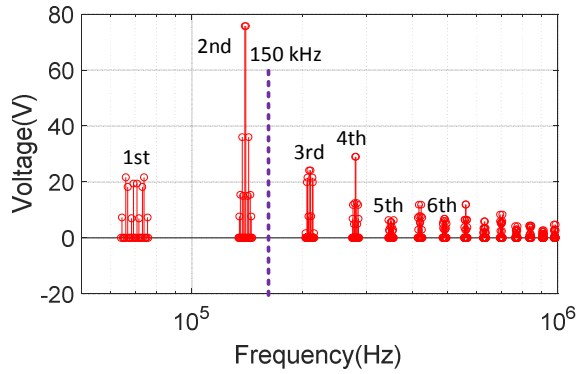
EMI filter corner frequency usually indicates EMI filter size and weight. The impact of interleaving on EMI filter corner frequency should be considered when selecting the interleaving angle.

When the objective is EMI noise and EMI filter reduction, symmetric interleaving may not be able to effectively reduce certain harmonics which actually determine the EMI filter corner frequency. For example, assume the carrier frequency is 70 kHz, the 1st and 2nd carrier harmonics are not in the EMI frequency (150 kHz ~ 30 MHz) range and the 3rd ~6th carrier harmonics are the potential candidates which may determine EMI filter corner frequency. Fig. 2(a) and Fig. 2(b) show a typical phase output CM voltage and DM voltage spectrum, respectively. The 3rd and 5th harmonics of the CM voltage are large and are desired to be reduced by interleaving, and the 4th and 6th harmonics of DM voltage are large and are desired to be reduced by interleaving. For two interleaved inverters, assume the interleaving angle of inverter 2 is γ with respect to inverter 1, the harmonic amplitude of two interleaved inverters output can be determined as (6). Then, the gain of 3rd ~6th carrier harmonics are calculated as shown in Fig. 3. For CM noise reduction, the interleaving angle can be selected as 36°~60° or around 180° as both 3rd and 5th harmonics have good attenuation. For DM noise reduction, the interleaving angle can be selected as 30°~45° or 135°~150° as both 4th and 6th harmonics have good attenuation.

$$C_{mn,avg}=\frac{1}{2}\left|(C_{mn,1}+C_{mn,2}e^{im\gamma})\right|=C_{mn}\left|\cos(m\gamma/2)\right| \quad (6)$$



(a)



(b)

Fig. 2. (a) CM voltage spectrum, (b) DM voltage spectrum.

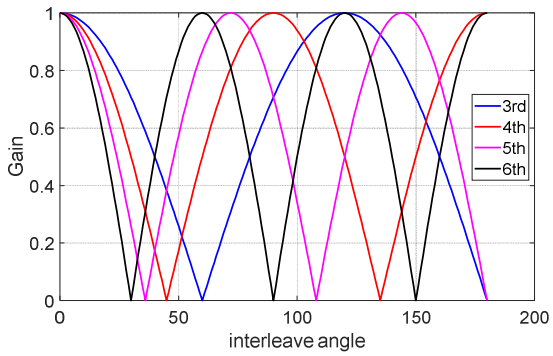


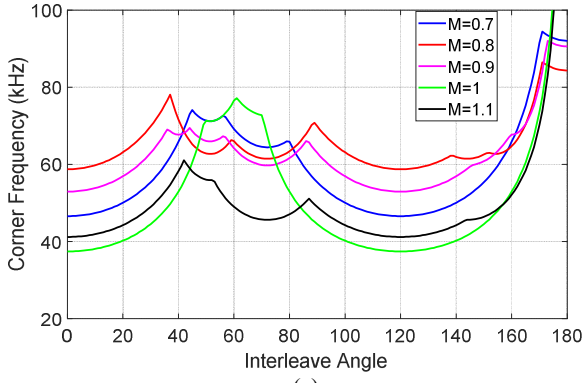
Fig. 3. The 3rd, 4th, 5th and 6th carrier harmonics and sidebands gain versus interleaving angle.

The relationship between EMI filter corner frequency and interleaving angle can be analytically derived. EMI filter corner frequency is determined by a certain noise peak [15]. With the method illustrated in [14], [16], the CM and DM voltage spectrum amplitude C_{mn} of a three-level inverter can be calculated. For the given load and specified EMI standards, the required noise attenuation can then be determined. The noise peak frequency f_{peak} which determines the EMI filter corner frequency can be identified with selected EMI filter type. Then, EMI filter corner frequency f_c can be calculated as (7).

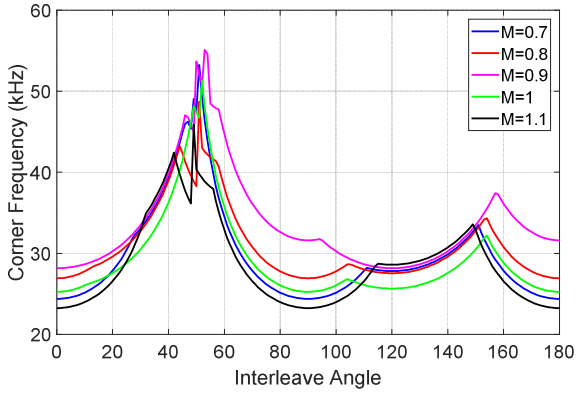
$$20\log_{10}(f_c) = 20\log_{10}(f_{peak}) + I_{std(f_{peak})} / k - 20\log_{10}\left(\frac{C_{mn(f_{peak})}\left|\cos(m\gamma/2)\right|\times 10^6}{Z_{(f_{peak})}}\right) / k \quad (7)$$

where $I_{std(f_{peak})}$ and $Z_{(f_{peak})}$ are the EMI standard defined noise current limit level and EMI noise propagation path impedance at f_{peak}, respectively. The filter type is indicated by k ($k = 2$ and $k = 4$ indicate single and two stage LC filters, respectively).

From (7), EMI filter corner frequency is a function of modulation index, interleaving angle, EMI filter type, load impedance, and carrier frequency. A specific case is calculated here which assumes 70 kHz carrier frequency, single stage LC filter and DO-160 EMI standards [17] applied. Fig. 4 summarizes the results when the modulation index (here the modulation index M is defined as the ratio between phase voltage amplitude and half of the dc bus voltage) is in the 0.7~1.1 range. From Fig. 4(a) and Fig. 4(b), the interleaving angle 40°~ 60° is preferred for both CM filter and DM filter design, and another good interleaving angle range for CM filter is around 180°. For other cases, the conclusion may be different but the method is the same.



(a)



(b)

Fig. 4. EMI Filter corner frequency versus interleaving angle, (a) CM filter, (b) DM filter.

Table I. Maximum Volt-seconds on Coupled Inductor of Phase A			
maximum volt-second	large sector 1 & large sector 4	large sector 2 & large sector 5	large sector 3 & large sector 6
subsector 1	$\frac{1}{2}V_{dc}\times\frac{1}{2}t_{sub2}$	$\frac{1}{2}V_{dc}\times\frac{1}{2}t_{sub2}$	$\frac{1}{2}V_{dc}\times(\frac{1}{2}t_{sub2}+\min(t_{sub1},t_{sub3}))$
subsector 2	$\frac{1}{2}V_{dc}\times\frac{1}{2}t_{sub2}$	$\frac{1}{2}V_{dc}\times(\frac{1}{2}t_{sub2}+\min(t_{sub4},t_{sub5}))$	$\frac{1}{2}V_{dc}\times\frac{1}{2}t_{sub2}$
subsector 3	$\frac{1}{2}V_{dc}\times(\frac{1}{2}t_{sub2}+\min(t_{sub3},t_{sub5}))$	$\frac{1}{2}V_{dc}\times\frac{1}{2}t_{sub2}$	$\frac{1}{2}V_{dc}\times\frac{1}{2}t_{sub2}$
subsector 4	$\frac{1}{2}V_{dc}\times\frac{1}{2}t_{sub3}$	$\frac{1}{2}V_{dc}\times(\frac{1}{2}t_{sub3}+\min(t_{sub5},t_{sub6}))$	$\frac{1}{2}V_{dc}\times\frac{1}{2}t_{sub3}$

III. Coupled Inductor Design for Interleved Three-level Inverters with SVM

Fig. 5 shows two paralleled three-level ANPC inverters with coupled inductors connecting the ac side.

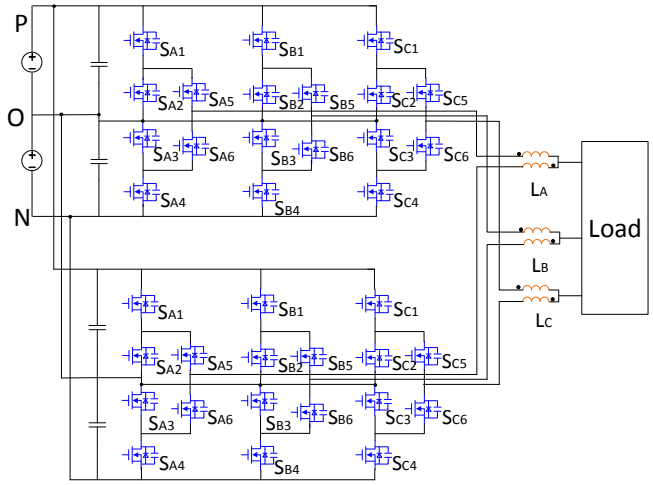
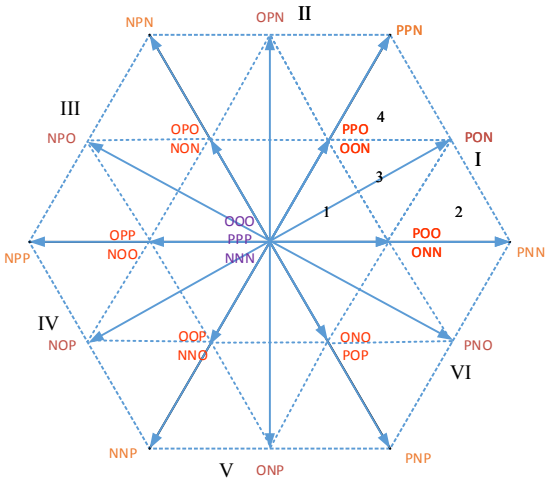


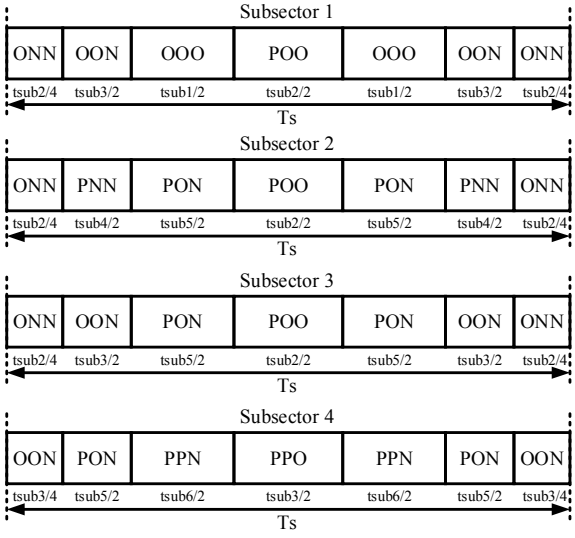
Fig. 5. Paralleled three-level ANPC inverters with coupled inductors.

The first step in the coupled inductor electrical design is to determine the maximum volt-seconds which is a function of the modulation scheme. Fig. 6(a) shows the space vectors in a three-level inverter, and Fig. 6(b) presents the switching sequence arrangement of a conventional center-aligned continuous SVM scheme in large sector 1. With the modulation scheme and interleaving angle selected, the volt-second on the coupled inductor can be derived. The worst case for volt-seconds is the symmetric interleaving.

Fig. 7 shows the ZSCC and circulating of different phases in one switching cycle in large sector 1 subsector 2 with symmetric interleaving. From Fig. 7(b), the coupled inductor maximum volt-second of three phases are different in different subsectors. In subsector 2 phase B has larger maximum volt-second value than phase A and phase C, while in other subsectors the scenarios can be different. The maximum volt-second on coupled inductor of phase A in all large sectors and subsectors are calculated and summarized in Table I. In Table I, V_{dc} represents the dc bus voltage, and the terms such as t_{sub2}, t_{sub4}, and t_{sub5} represents the dwell time of corresponding vector shown in Fig. 6(b). The dwell time calculation of space vectors in a three-level SVM is well known and will not be repeated here.

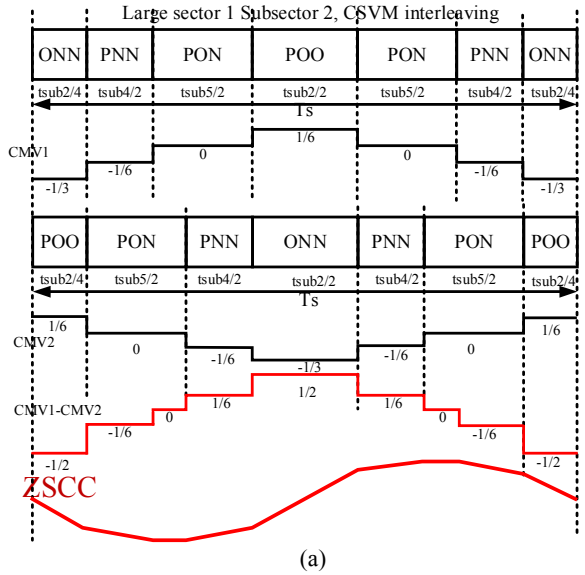


(a)

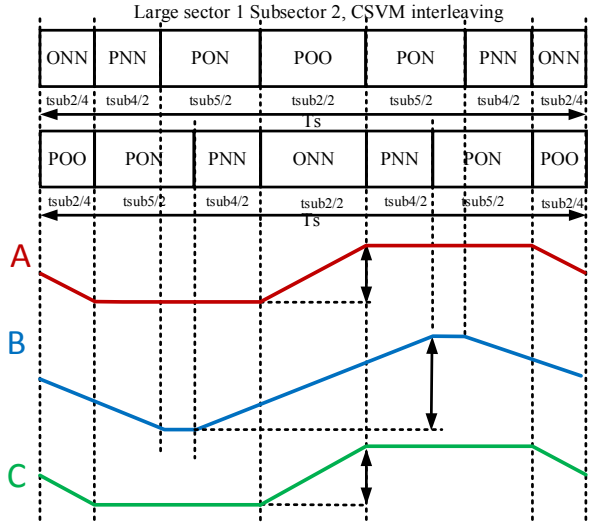


(b)

Fig. 6. (a) Space vectors of three-level SVM, (b) switching sequence of a conventional center-aligned continuous SVM in large sector 1.



(a)



(b)

Fig. 7. (a) ZSCC pattern in large sector 1 subsector 2, (b) circulating current of three phases in large sector 1 subsector 2.

In a three-level inverter with SVM, the subsectors are determined by both the reference amplitude and reference angle. When the modulation index changes, the subsectors and space vectors used to synthesize the reference will also be different, as a result, the maximum volt-seconds on the coupled inductor will be different. Considering the full modulation index range, the normalized maximum volt-seconds on the coupled inductor of phase A when the reference goes through a full circle at different modulation indexes is derived and summarized as shown in Fig. 8. The volt-seconds calculation of phase B and phase C is similar and will not be repeated here.

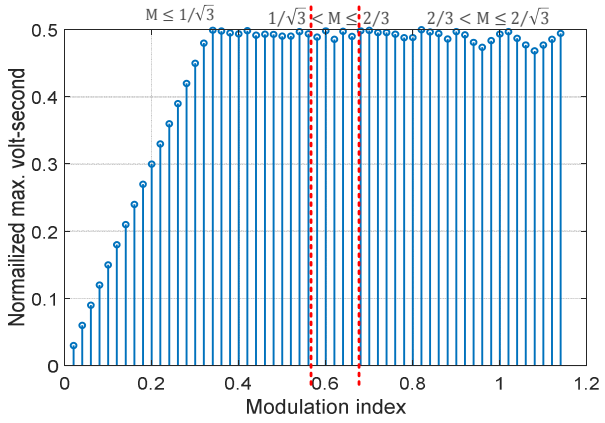


Fig. 8. Normalized maximum volt-second versus modulation index.

The second step in the coupled inductor electrical design is to select maximum current ripple. Then, as $L = \int vdt/\Delta i$, the required inductance of the coupled inductor can be determined. The minimum total losses of power devices and coupled inductor can be used as a criteria for maximum current ripple selection. The current ripple has complicated influence on both the devices loss and the coupled inductor loss, and it is difficult to derive an analytical formula. With the parameters and operating condition described in experiment results section, the total device loss and coupled inductor loss at different maximum current ripple are obtained based on simulation and summarized as shown in Fig. 8. According to Fig. 9, 10%~15% maximum current ripple level is preferred for the studied case.

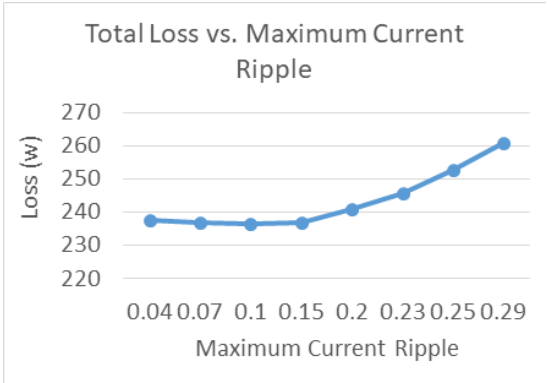


Fig. 9. Total power devices and coupled inductor losses versus current ripple.

Next step is the coupled inductor physical design. Integration of coupled inductor and DM inductor is considered for filter weight reduction [12]. If high permeability core material is applied, a little unbalance in the output current of two inverters may lead to coupled inductor core saturation. Hence, high permeability nanocrystalline core with air gap is preferred. The leakage inductance is used as the DM inductor for DM EMI noise suppression. By tuning the air gap length and the winding number of turns, both the

coupled inductance and the leakage inductance can achieve the desired value.

With the analysis presented above, Fig. 10 summarizes the coupled inductor design methodology.

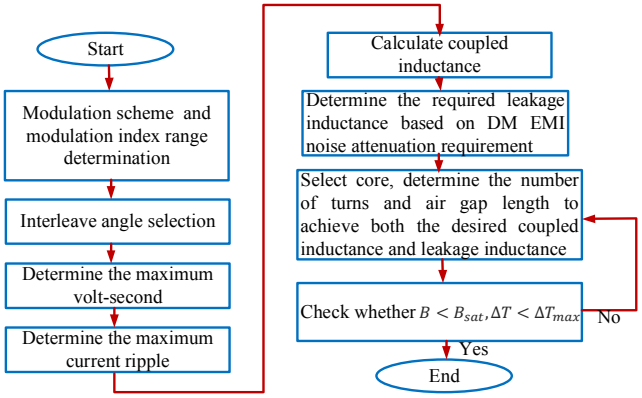


Fig. 10. Coupled inductor design methodology.

IV. Experiment Results

Two paralleled three-level ANPC inverters are constructed for experimental verification. Fig. 11 shows the experimental platform. The dc input voltage is 400 V. The ac output fundamental frequency is 3 kHz and the switching frequency is 60 kHz. The nanocrystalline Vitroperm 500F U-type cut core with air gap is chosen for the coupled inductors as shown in Fig. 11. The coupled inductor mutual inductance is 280 uH, and the leakage inductance is 30 uH based on the design requirements.

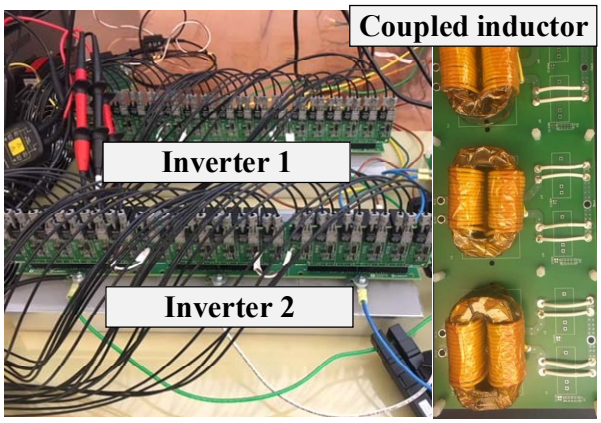


Fig. 11. Experiment platform.

Fig. 12 shows the experiment waveforms of paralleled three-level ANPC inverters with 180° interleaving angle. Fig. 12(a), Fig. 12(b), and Fig. 12(c) are the phase output voltage, three phase output currents and the ZSCC, and output currents of phase A of two inverters and the circulating current, respectively. The ZSCC and the circulating current patterns match theoretical analysis.

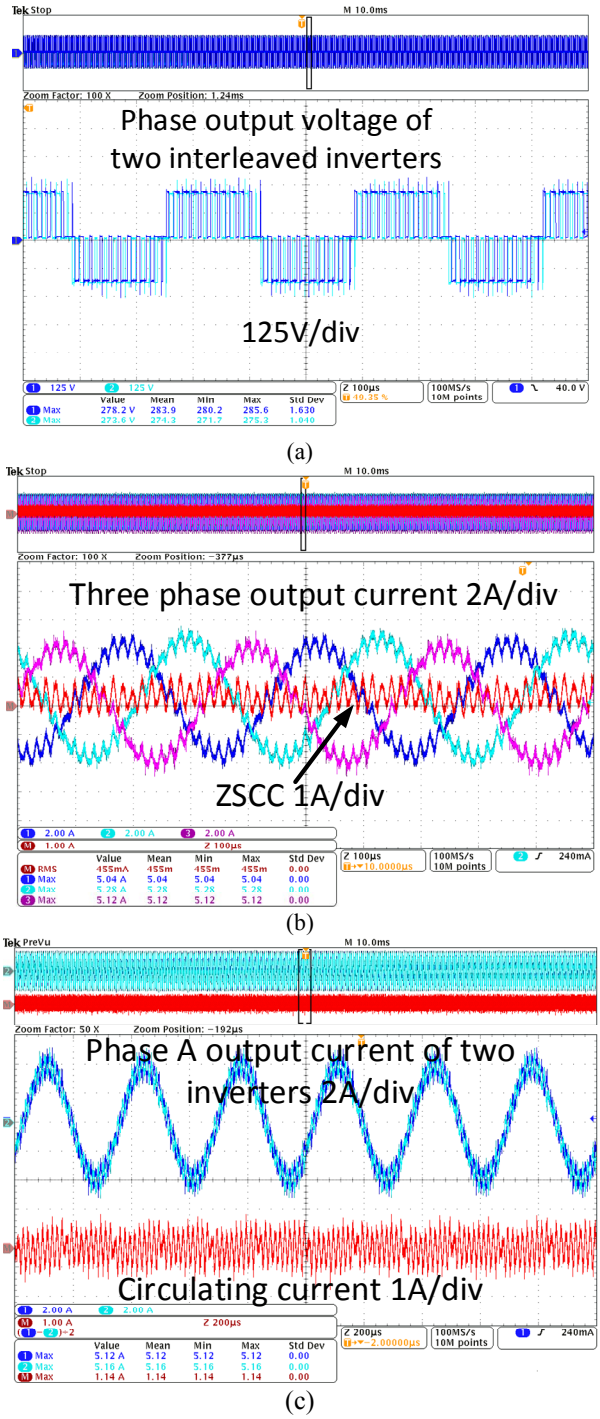


Fig. 12. Two inverters paralleled operation with 180° interleaving angle, (a) phase output voltage, (b) three phase current and ZSCC, (c) phase A currents of two inverters and circulating current.

An interleaving angle in the range of 40°~ 60° is preferred for both CM and DM filter design based on the studies presented. The comparison experiments on EMI noise test are conducted. Fig. 13 shows the tested CM noise with 0° and with 60 ° interleaving angle. From Fig. 13, in the EMI frequency range, compared to 0° interleaving angle, the 3rd carrier harmonic (180 kHz) noise reduced around 25 dB, and

the 4th carrier harmonic (240 kHz) reduced around 5 dB with 60° interleaving angle. Fig. 14 shows the tested DM noise with 0° and with 60° interleaving angle. Similar trend can be observed. The required EMI filter electrical parameters can be significantly reduced with the 40°~ 60° interleaving angle.

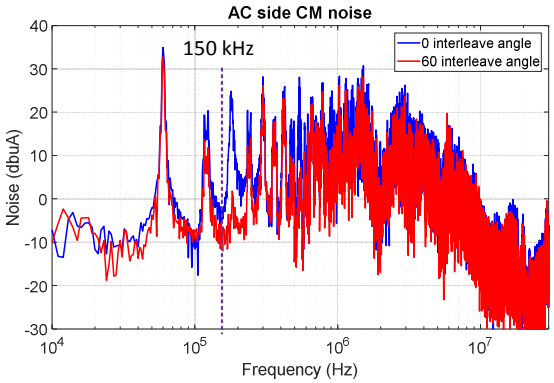


Fig. 13. CM noise test results with 0° and 60° interleaving angle.

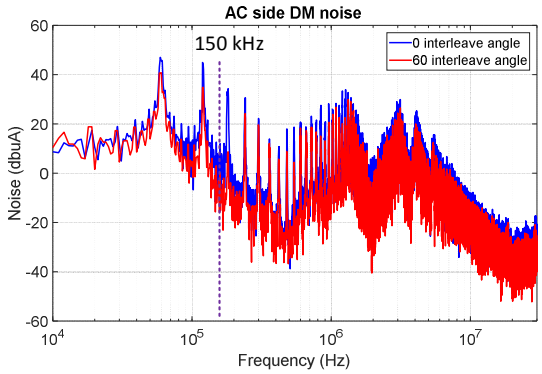


Fig. 14. DM noise test results with 0° and 60° interleaving angle.

V. Conclusion

This paper presents the coupled inductor design for interleaved three-level active neutral point clamped inverters considering EMI noise reduction. The analysis shows that interleaving converts part of the output harmonics into circulating current and thus reduces the EMI noise in the output. The relationship between EMI filter corner frequency and interleaving angle is analytically derived, interleaving angle in the range of 40°~ 60° is preferred for both CM and DM filter design in the studied case. Then, the coupled inductor design methodology is illustrated considering three-level SVM scheme. The maximum volt-seconds, ripple current selection, and physical design of the coupled inductor are discussed.

Experiment results on two interleaved three-level ANPC inverters with the designed coupled inductor are presented, which verifies the coupled inductor design. Experiment results show that, with 60° interleaving angle, the 3rd carrier harmonic noise reduces around 25 dB, and the 4th carrier harmonic reduces around 5 dB for both the CM and DM noise current, which will significantly reduce the required EMI filter size.

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