# Analytical Analysis of Ac and Dc Side Harmonics of Three-level Active Neutral Point Clamped Inverter with Space Vector Modulation

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***Abstract*—This paper presents a comprehensive analytical analysis of the ac and dc side harmonics of the three-level active neutral point clamped (ANPC) inverter with space vector modulation (SVM) scheme. An analytical model to calculate the harmonics of a three-level converter with SVM is developed. The ac side output voltage harmonics and dc side current harmonics characteristics are calculated and analyzed. With the developed models, the impact of interleaving on both sides harmonics are studied which considers the modulation index, interleaving angle, and power factor. The analysis provides guideline for interleaving angle optimization to reduce the ac side power filter and dc side dc-link capacitor. The relationship between electromagnetic interference (EMI) filter corner frequency and switching frequency is also analytically derived which provides guideline for switching frequency and EMI filter design optimization. Two paralleled three-level ANPC inverters are constructed and experimental results are presented to verify the analytical analysis.**

***Keywords—Three-level NPC converter; SVM; harmonics; interleaving angle; EMI filter.***

## I. INTRODUCTION

Pulse width modulation (PWM) generates undesired harmonics, and passive components are usually required at both ac and dc sides of a power converter to suppress the switching frequency related harmonics to meet power quality requirements and pass EMI standards. Identification of the harmonics is important for passive components design and reduction. Although time domain simulation can be used to investigate the harmonics, an analytical approach is more time-efficient, accurate and provides insightful views for understanding in most cases. Also, it is good or even necessary for the trade study where several cases need to be investigated.

Harmonics generated by a PWM method can be determined using double Fourier integral analysis [1], and extensive study has been conducted on the harmonic analysis of single and interleaved two-level converters. The ac output side voltage harmonics of two-level voltage source converter (VSC) with both carrier based PWM and space vector based PWM have been calculated in [1]. The dc side input current spectrum of two–level VSC with sine-triangle modulation is calculated in [2] - [3]. The impact of interleaving on harmonic voltages and currents on the ac side and dc side of two-level VSI are analyzed in [4] - [6].

Compared to two-level converters, the scenarios involved in three-level inverters are more complicated. The ac output voltage spectral analysis of cascaded two two-level inverters with SPWM is presented in [7]. The dead time introduced harmonics in the output voltage of three-level NPC inverter is analyzed in [8]. The line current harmonics of a three-level rectifier with SPWM is illustrated in [9]. All prior work on harmonic analysis of three-level inverters are for carrier based PWM schemes, especially SPWM.

Space vector based PWM are more flexible and popular in three-level converters. With redundant vectors in three-level converters, multiple control objectives such as balancing the neutral-point voltage, reducing EMI noise , and reducing switching loss can be achieved by selecting different redundant vectors of three-level SVM [10]. Popular SVM schemes such as nearest three space vector (NTSV) [11], common-mode reduction (CMR) [12] and common-mode elimination (CME) [13] are developed. However, no literature is found to develop the analytical models for harmonic calculation of these SVM based three-level converters. Moreover, in previous work regarding three-level NPC inverters, the dc-link capacitor current harmonics characteristics has not been discussed, and the impact of interleaving angle on both ac and dc side harmonics of paralleled three-level NPC inverters has not been investigated. Hence, this paper will present new results in these areas.

This paper presents comprehensive analytical analysis of both ac and dc side harmonics of three-level ANPC inverters with SVM. An analytical model to calculate the harmonics of three-level SVM is developed. The ac side output voltage harmonics and dc side input current harmonics characteristics are calculated and analyzed. The impact of interleaving on ac side output voltage harmonics and dc side input ripple current rms value considering modulation indexes, interleaving angle, and power factors are investigated. The relationship between EMI filter corner frequency and switching frequency is also analytically derived.

## II. Analytical Model for Ac and Dc Side Harmonics

### A. SVM in Three-level Inverter

Fig. 1(a) shows the space vectors for three-level SVM. There are a total of 27 switching states which can be grouped into six long vectors, six medium vectors, six small vectors, and one zero vectors. The small and zero vectors have redundant switching states. The three-level vector hexagon is divided into six large triangles. Each of them is further divided into four small triangles. The reference location and duty cycle calculation method is illustrated in [10], which will not be repeated here.

The NTSV scheme uses all the redundant switching states of small vectors, which can achieve minimal harmonic distortion and neutral point voltage balancing. Fig. 2 shows the vector arrangement of NTSV in all four sub-sectors of large-sector 1. NTSV is used as an example to develop the analytical models in this paper.

The main difference between two-level and three-level modulation is that the sector is determined by both the reference angle and amplitude in a three-level modulation while the sector is only determined by the reference angle in a two-level modulation. To better illustrate the harmonic calculation of three-level SVM, three regions are defined based on the modulation index (here the modulation index M is defined as the ratio between phase voltage amplitude and half of the dc bus voltage).

$$\text{Region 1}: M \le 1/\sqrt{3}$$
$$\text{Region 2}: 1/\sqrt{3} < M \le 2/3$$
$$\text{Region 3}: 2/3 < M \le 2/\sqrt{3}$$

The three regions are shown in Fig. 3. When the reference is in Region 1, it will only go through sub-sector 1 of large-sector 1. When the reference is in Region 2, it will go through large-sector 1 from sub-sector 1 to sub-sector 3 and then back to subsector 1. When the reference is in Region 3, it will go through large-sector 1 from sub-sector 2 to sub-sector 3 and then to sub-sector 4. The cases in other large-sectors are the same. In both Region 2 and Region 3, the reference will go through different sub-sectors. Fig. 4 shows the case in large-sector 1. For calculation purposes, the two sub-sector boundary angles are defined as $\theta_1$ and $\theta_2$ as shown in Fig. 4. The boundary angles in Region 2 and Region 3 are calculated as (1) and (2), respectively.

$$\theta_1 = \arcsin(\frac{1}{\sqrt{3}M}) - \frac{\pi}{3}, \theta_2 = \frac{2\pi}{3} - \arcsin(\frac{1}{\sqrt{3}M}) \quad (1)$$

$$\theta_1 = \frac{\pi}{3} - \arcsin(\frac{1}{\sqrt{3}M}), \theta_2 = \arcsin(\frac{1}{\sqrt{3}M}) \quad (2)$$

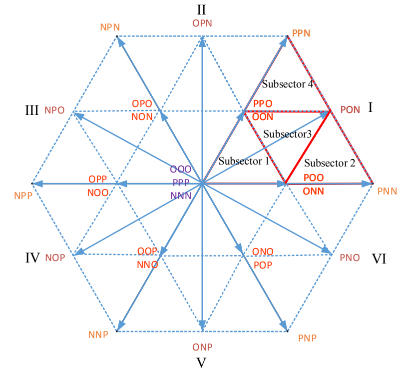



Fig. 1. Space vectors for three-level SVM.

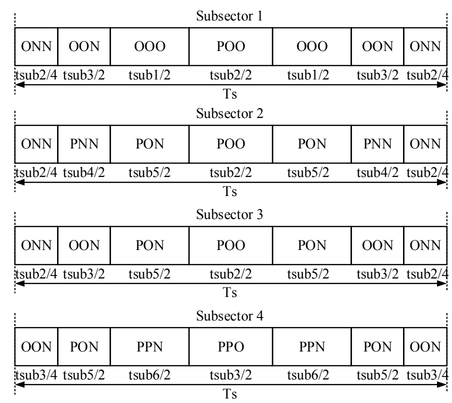



Fig. 2. Vector arrangement of NTSV in large-sector 1.

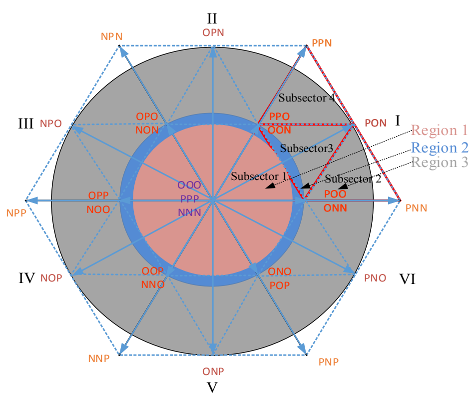




Fig. 3. Three regions defined by the modulation index.

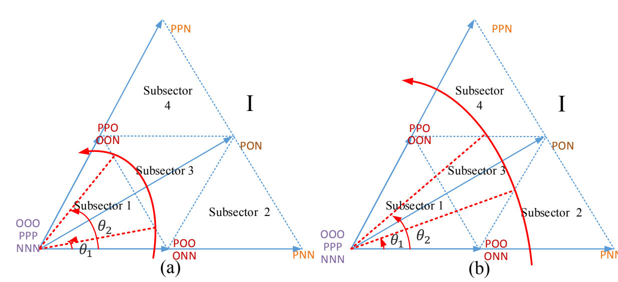



Fig. 4. Two sub-sector boundary angles in large-sector 1. (a) Region 2. (b) Region 3.

$$f(t)=\frac{A_{00}}{2}+\sum_{n=1}^{\infty}[A_{0n}\cos(ny)+B_{0n}\sin(ny)]+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}[A_{mn}\cos(mx+ny)+B_{mn}\sin(mx+ny)]$$
$$A_{mn}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}f(x,y)\cos(mx+ny)dxdy, B_{mn}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}f(x,y)\sin(mx+ny)dxdy, C_{mn}=A_{mn}+jB_{mn}, x=\omega_c t, y=\omega_0 t, \forall m,n=1,\ldots,\infty \quad (3)$$

$$C_{mn}=\frac{1}{2\pi^2}[\int_{-\pi}^{-\frac{\pi}{2}}\int_{-\pi}^{-\pi(1+M\cos y)}(-\frac{V_{dc}}{2})e^{j(mx+ny)}dxdy+\int_{-\pi}^{-\frac{\pi}{2}}\int_{\pi(1+M\cos y)}^{\pi}(-\frac{V_{dc}}{2})e^{j(mx+ny)}dxdy$$
$$+\int_{\frac{\pi}{2}}^{\pi}\int_{-\pi}^{-\pi(1+M\cos y)}(-\frac{V_{dc}}{2})e^{j(mx+ny)}dxdy+\int_{\frac{\pi}{2}}^{\pi}\int_{\pi(1+M\cos y)}^{\pi}(-\frac{V_{dc}}{2})e^{j(mx+ny)}dxdy+\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\int_{-\pi M\cos y}^{\pi M\cos y}(\frac{V_{dc}}{2})e^{j(mx+ny)}dxdy] \quad (4)$$

*B. Analytical Solution for Ac Side Output Voltage Harmonics*

The spectrum of pulse width modulated phase leg voltage can be expressed as (3) [1]. Here, $m$ and $n$ are carrier and baseband integer indices, respectively. Harmonic coefficient is represented by $C_{mn}$. Carrier and fundamental angular frequency are represented by $\omega_c$ and $\omega_0$, respectively.

The unit cell contour plot for the three-level naturally sampled PD PWM is shown in Fig. 5 when the sinusoidal reference is $f(y) = Mcosy$. Then, the harmonic coefficient $C_{mn}$ can be determined as (4).

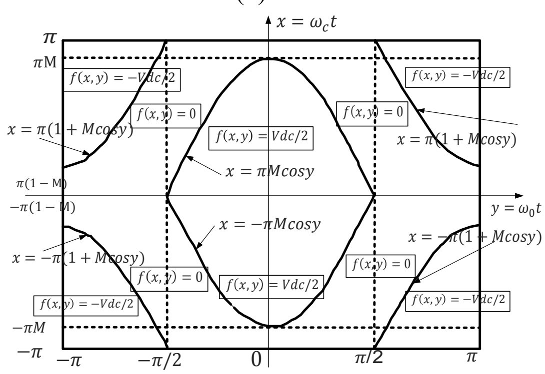



Fig. 5. Contour plot for a three-level naturally sampled PD PWM.

SVM is functionally equivalent to carrier based PWM [14]. The basic idea to derive the analytical solution for three-level SVM scheme is to re-define the integral limits in (4) by taking account of the fact that the phase leg reference is no longer continuous sinusoidal but is now made up of several segments across a full fundamental cycle.

Take large-sector 1 sub-sector 2 as an example, the equivalent reference can be calculated as (5) and the inner integral limits can be determined as (6). The integral limits in other sub-sectors can be determined similarly.

$$V_{ref(1,2)}=\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}) \quad (5)$$

$$x_{r(1,2)}=-\pi[\frac{\sqrt{3}}{2}M\cos(\theta-\frac{\pi}{6})], x_{f(1,2)}=\pi[\frac{\sqrt{3}}{2}M\cos(\theta-\frac{\pi}{6})] \quad (6)$$

For different regions, as the reference will go through different sub-sectors, the equivalent reference and double Fourier integral limits will be different. Table I summarizes the integral limits of large-sector 1, large-sector 2, and large-sector 3 in Region 1. Table II and Table III summarize the integral limits of large-sector 1 in Region 2 and Region 1, respectively. The calculation for other large-sectors are similar and will not be repeated here.

Table I. Double Fourier Integral Limits in Region 3 (Large-sector 1, large-sector 2, and large-sector 3)

| $y_s$ | $y_e$ | $x_r$ | $x_f$ | $f(x,y)$ |
|---|---|---|---|---|
| $0$ | $\theta_1$ | $-\pi[\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$ | $\pi[\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$ | $\frac{V_{dc}}{2}$ |
| $\theta_1$ | $\theta_2$ | $-\pi[\frac{3}{2}M\cos(y)-\frac{1}{2}]$ | $\pi[\frac{3}{2}M\cos(y)-\frac{1}{2}]$ | $\frac{V_{dc}}{2}$ |
| $\theta_2$ | $\frac{\pi}{3}$ | $-\pi[\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$ | $\pi[\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$ | $\frac{V_{dc}}{2}$ |
| $\frac{\pi}{3}$ | $\frac{\pi}{3}+\theta_1$ | $-\pi[\frac{3}{2}M\cos y]$ | $\pi[\frac{3}{2}M\cos y]$ | $\frac{V_{dc}}{2}$ |
| $\frac{\pi}{3}+\theta_1$ | $\frac{\pi}{3}+\theta_2$ | $-\pi[\frac{1}{2}+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\pi[\frac{1}{2}+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\frac{V_{dc}}{2}$ |
| $\frac{\pi}{3}+\theta_2$ | $\frac{2\pi}{3}$ | $-\pi$ | $-\pi[1+\frac{3}{2}M\cos y]$ | $\frac{-V_{dc}}{2}$ |
| | | $\pi[1+\frac{3}{2}M\cos y]$ | $\pi$ | |
| $\frac{2\pi}{3}$ | $\frac{2\pi}{3}+\theta_1$ | $-\pi$ | $-\pi[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\frac{-V_{dc}}{2}$ |
| | | $\pi[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\pi$ | |
| $\frac{2\pi}{3}+\theta_1$ | $\frac{2\pi}{3}+\theta_2$ | $-\pi$ | $-\pi[\frac{1}{2}+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$ | $\frac{-V_{dc}}{2}$ |
| | | $\pi[\frac{1}{2}+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$ | $\pi$ | |
| $\frac{2\pi}{3}+\theta_2$ | $\pi$ | $-\pi$ | $-\pi[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\frac{-V_{dc}}{2}$ |
| | | $\pi[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\pi$ | |

Table II. Double Fourier Integral Limits in Region 2 (Large-sector 1)

| $y_s$ | $y_e$ | $x_r$ | $x_f$ | $f(x,y)$ |
|---|---|---|---|---|
| $0$ | $\theta_1$ | $-\pi[\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\pi[\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\frac{V_{dc}}{2}$ |
| $\theta_1$ | $\theta_2$ | $-\pi[\frac{3}{2}M\cos(y)-\frac{1}{2}]$ | $\pi[\frac{3}{2}M\cos(y)-\frac{1}{2}]$ | $\frac{V_{dc}}{2}$ |
| $\theta_2$ | $\frac{\pi}{3}$ | $-\pi[\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\pi[\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\frac{V_{dc}}{2}$ |

Table III. Double Fourier Integral Limits in Region 1 (Large-sector 1)

| $y_s$ | $y_e$ | $x_r$ | $x_f$ | $f(x,y)$ |
|---|---|---|---|---|
| $0$ | $\frac{\pi}{3}$ | $-\pi[\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\pi[\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$ | $\frac{V_{dc}}{2}$ |

$$I_{dc\_a}(\omega) = s_{1H\_a}(\omega) \otimes I_o(\omega) = I_0 / 2 \times (e^{j\phi} s_{1H\_a}(\omega - \omega_0) + e^{-j\phi} s_{1H\_a}(\omega + \omega_0)) \tag{7}$$

$$I_{dc\_a}(t) = A_{00\_a} / 2 + \sum_{n=1}^{\infty} [A_{0n\_a} \cos(ny) + B_{0n\_a} \sin(ny)] + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [A_{mn\_a} \cos(mx + ny) + B_{mn\_a} \sin(mx + ny)] \tag{8}$$

$$\begin{aligned} A_{00\_a} &= \frac{I_0}{2}(A_{01} \cos\phi + B_{01} \sin\phi), A_{mn\_a} = \frac{I_0}{2}[(A_{m,n-1\_1a} + A_{m,n+1\_1a})\cos\phi + (B_{m,n-1\_1a} - B_{m,n+1\_1a})\sin\phi] \\ B_{mn\_a} &= \frac{I_0}{2}[(B_{m,n-1\_1a} + B_{m,n+1\_1a})\cos\phi - (A_{m,n-1\_1a} - A_{m,n+1\_1a})\sin\phi] \end{aligned} \tag{9}$$

$$I_{dc}(\omega) = s_{a1}(\omega) \otimes I_{0a}(\omega) + s_{b1}(\omega) \otimes I_{0b}(\omega) + s_{c1}(\omega) \otimes I_{0c}(\omega), C_{mn} = C_{mn\_a}(1 + 2\cos(n\frac{2\pi}{3})) \tag{10}$$

$$I_{DC} + i_{C1}(t) = i_p(t), I_{DC} + i_{C2}(t) = i_n(t), i_{neutral}(t) = i_{C1}(t) - i_{C2}(t) = i_p(t) - i_n(t) \tag{11}$$

### *C. Analytical Solution for Dc Side Current Harmonics*

Fig. 6(a) depicts the switching pattern of a three-level ANPC inverter, and Fig. 6(b) shows the current paths of the two dc-link capacitors.

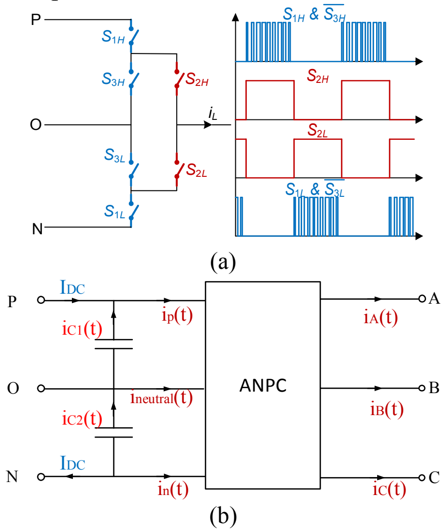



Fig. 6. (a) Switching pattern of three-level ANPC inverter, (b) current path.

The positive line current $i_p(t)$ of the ANPC inverter is a combination of ac output currents and the uppermost switch $S_{1H}$. Usually the ac output current can be considered as pure sinusoidal if the THD is small. The frequency domain expression of switched current of phase A can be derived as (7). Here, $s_{1H\_a}$ represents the switching function of the switch $S_{1H\_A}$. $I_0$ and $\emptyset$ are the amplitude of the phase output current and the power factor, respectively. Let $C_{mn\_1a} = A_{mn\_1a} + jB_{mn\_1a}$ to be harmonic coefficient of switching function $s_{1H\_a}$. The double Fourier integral limits of $C_{mn\_1a}$ is similar as the derived phase output voltage model in section B. The difference is that $f(x, y) = 1$ for the positive half cycle and $f(x, y) = 0$ for the negative half cycle. Table IV summarizes the integral limits for $C_{mn\_1a}$ of large-sector 1, large-sector 2, and large-sector 3 in Region 3. Then, transforming (7) back to the time domain, the Fourier series is represented in (8) with the harmonic coefficients denoted in (9). The contribution of phase B and phase C can be calculated similarly. The harmonic coefficient $C_{mn}$ of $i_p(t)$ is derived by summing the three phases as (10). The harmonic spectrum of $i_n(t)$is similar as $i_p(t)$ due to the symmetry, and neutral-line current $i_{neutral}(t)$ harmonics can be calculated based on (11).

Table IV. Double Fourier Integral Limits for $C_{mn\_1a}$ in Region 3 (Large sector 1, 2, and 3)

| $y_s$ | $y_e$ | $x_r$ | $x_f$ | $f(x,y)$ |
|---|---|---|---|---|
| 0 | $\theta_1$ | $-\pi[\frac{\sqrt{3}}{2} M \cos(y - \frac{\pi}{6})]$ | $\pi[\frac{\sqrt{3}}{2} M \cos(y - \frac{\pi}{6})]$ | 1 |
| $\theta_1$ | $\theta_2$ | $-\pi[\frac{3}{2} M \cos(y) - \frac{1}{2}]$ | $\pi[\frac{3}{2} M \cos(y) - \frac{1}{2}]$ | 1 |
| $\theta_2$ | $\frac{\pi}{3}$ | $-\pi[\frac{\sqrt{3}}{2} M \cos(y - \frac{\pi}{6})]$ | $\pi[\frac{\sqrt{3}}{2} M \cos(y - \frac{\pi}{6})]$ | 1 |
| $\frac{\pi}{3}$ | $\frac{\pi}{3} + \theta_1$ | $-\pi[\frac{3}{2} M \cos y]$ | $\pi[\frac{3}{2} M \cos y]$ | 1 |
| $\frac{\pi}{3} + \theta_1$ | $\frac{\pi}{3} + \theta_2$ | $-\pi[\frac{1}{2} + \frac{\sqrt{3}}{2} M \cos(y + \frac{\pi}{6})]$ | $\pi[\frac{1}{2} + \frac{\sqrt{3}}{2} M \cos(y + \frac{\pi}{6})]$ | 1 |
| $\frac{\pi}{3} + \theta_2$ | $\pi$ | Not needed as $f(x,y)=0$ | | 0 |

To illustrate the difference in the dc side current harmonics between a three-level ANPC inverter and a two-level inverter, the dc side current characteristics of the two-level inverter is briefly illustrated. Based on the principle illustrated in [3], the dc side current spectrum in a two-level inverter with SVM is calculated and the main components are shown in Fig. 7. The dc side input current spectrum only have a dc component, $(2m - 1)f_c \pm 3(2n - 1)f_0$components for odd order carrier harmonics and sidebands, and $2mf_c \pm 3(2n)f_0$ components for even order carrier harmonics and sidebands. Since the 1st carrier harmonic is eliminated, the 2nd carrier harmonic becomes the dominant high frequency component.

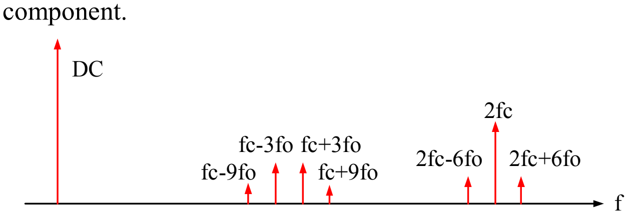
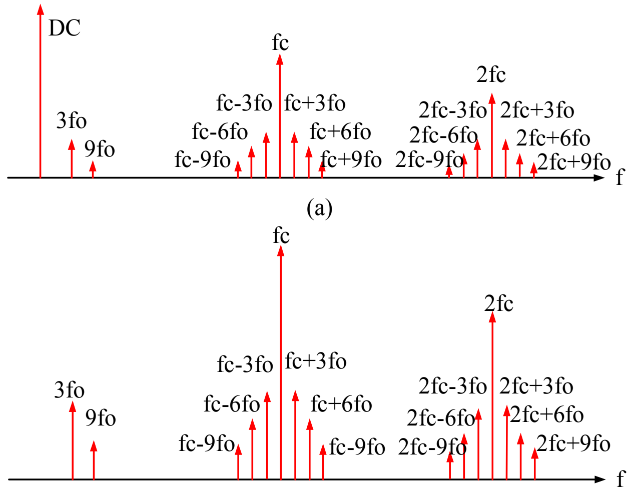



Fig. 7. Dc side current spectrum of a two-level inverter with SVM when power factor PF=1.

Then, based on the derived dc side current harmonic model for three-level ANPC inverter, the current spectrum is calculated and the main components are shown in Fig. 8. Fig.

8(a) shows the positive/negative line current ($i_p(t)$ or $i_n(t)$) spectrum, and Fig. 8(b) is the neutral line current $i_{neutral}(t)$ spectrum. It can be observed that, unlike the spectrum of the two-level inverter, the positive/negative line current has dc components, the third order harmonics, $mf_c \pm 3nf_0$ carrier harmonics and sidebands. The neutral line current does not have a dc component, but it also has the third harmonics and all the carrier harmonics and sidebands with the amplitude doubled. The 1st carrier harmonic becomes the dominant high frequency component.



(b)

Fig. 8. Dc side current spectrum of a three level ANPC inverter with NTSV when power factor PF=1, (a) Positive/negative line current, (b) neutral line current.

## III. Impact of Interleaving on Ac and Dc Side Harmonics

The impact of interleaving for paralleled three-level ANPC inverters is investigated. For two interleaved inverters, if the interleaving angle of inverter 2 is $\gamma$ with respect to inverter 1, the harmonic amplitude of two interleaved inverters output can be determined as (12). From (12), it is obvious that interleaving can reduce the amplitude of the harmonics.

$$C_{mn,avg} = \frac{1}{2}\left|(C_{mn,1} + C_{mn,2}e^{im\gamma})\right| = C_{mn}\left|\cos(m\gamma/2)\right| \qquad (12)$$

WTHD is a useful figure of merit to size the power filter requirements in the ac output side [1]. With the developed models in section II and (12), the ac side line to line voltage harmonics WTHD0 is calculated as a function of interleave angle and modulation index. Fig. 9 shows the results. It can be observed that WTHD0 achieved minimum value when interleaving angle is around 90° for different modulation indexes. This can be explained by investigating the ac side voltage harmonic characteristics. Fig. 10 shows the main components of ac side voltage spectrum of a three-level ANPC inverter with NTSV. From Fig. 10(b), the dominant high frequency components in the line to line voltage are the 2nd carrier harmonic sidebands $2f_c \pm f_0$, and 90° interleaving angle will eliminate the 2nd carrier harmonic and its sidebands.

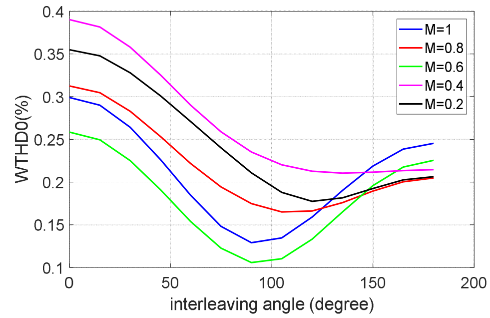
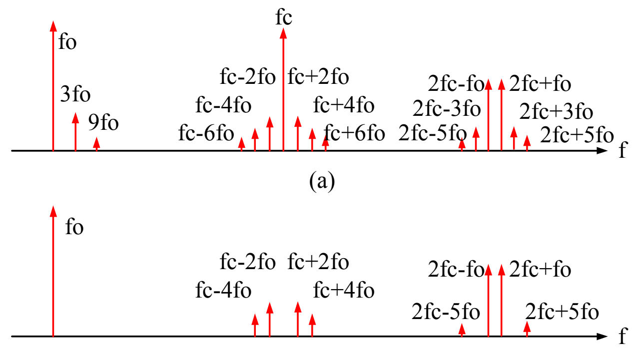


Fig. 9. Ac side line to line voltage WTHD0 versus interleaving angle ($f_0 = 400\ Hz, f_c = 20\ kHz$).



(b)

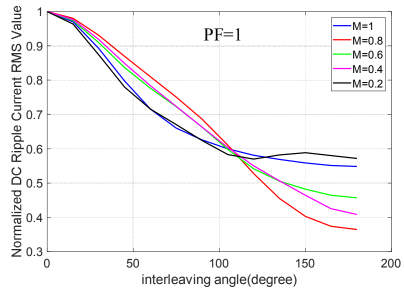
Fig. 10. Ac side voltage spectrum a three-level ANPC inverter with NTSV, (a) phase voltage, (b) line to line voltage.

Ripple current rms value can be used to evaluate the dc side dc-link capacitor requirements. With the developed models in section II and (12), the normalized dc-link capacitor ripple current rms value is calculated as a function of interleave angle, modulation index, and power factor.

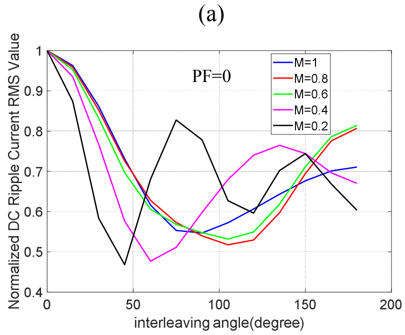
The results are shown in Fig. 11. It can be found that the dc-link capacitor ripple current rms value is highly dependent on converter operation condition. Also, the results show different trends compared to the interleaved two-level inverters analyzed in [7]. For interleaved three-level ANPC inverter, when the modulation index is high and power factor is high, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle is around 180°. This can be expected as the 1st carrier harmonic exists and is the dominant high frequency component in the dc-link capacitor current, and 180° interleaving angle will totally eliminate the 1st carrier harmonic and its sidebands. When the modulation index is high and power factor is low, the minimum dc-link capacitor ripple current rms value can be achieved when the interleaving angle is around 90°. This is because the 2st carrier harmonic sidebands becomes the dominant high frequency components with low power factor, and 90° interleaving angle will eliminate the 2nd carrier harmonic and its sidebands. When the modulation index is low (in Region 1), both the 1st and 2nd and high order carrier harmonic sidebands are dominant, so the dc-link capacitor ripple current rms value shows a complicated variation trend when the interleaving angle varies.

$$V_{CM}=\frac{V_{AN}+V_{BN}+V_{CN}}{3}=\frac{1}{3}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{mn}\cos(mx+ny)[1+2\cos(n\frac{2\pi}{3})],V_{DM\_A}=V_{AN}-V_{CM} \quad (13)$$

$$20\log_{10}(f_c)=20\log_{10}(f_{peak})+I_{std(f_{peak})}/k-20\log_{10}(\frac{C_{mn(f_{peak})}(1+2\cos(n\frac{2}{3}\pi))\times 10^6}{Z_{CM(f_{peak})}})/k \quad (14)$$



(a)



(b)

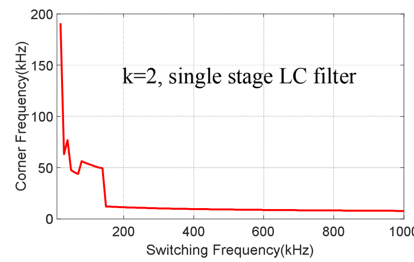
Fig. 11. Dc side dc-link capacitor ripple current RMS value versus interleaving angle ($f_0 = 400\ Hz$,$f_c = 20\ kHz$), (a) PF=1, (b) PF=0.

## IV. Relationship between EMI Filter Corner Frequency and Switching Frequency

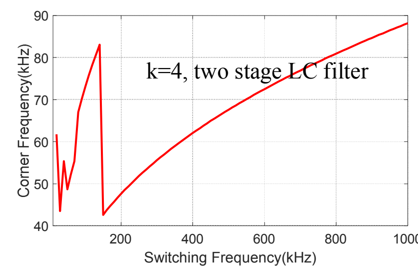
In addition to power filters and dc-link capacitor, EMI filter is also one of the main passive components in power converters. The size and weight of an EMI filter can usually be indicated by the EMI filter corner frequency. With the developed models in section II, the relationship between EMI filter corner frequency and switching frequency can be analytically derived.

The harmonic spectrum of phase voltage is calculated in section B. Then, the EMI noise source for both common-mode (CM) and differential-mode (DM) voltages can be determined as (13). EMI filter design methodology is illustrated in [15]. EMI filter corner frequency is determined by a certain noise peak. As the CM and DM noise source are calculated, the load and EMI standards are given, the required noise attenuation can be determined. After the EMI filter type is selected, the noise peak frequency $f_{peak}$ which determines the EMI filter corner frequency can be identified. Take CM noise as an example, the motor drive system for aircraft application is studied, and the ac output EMI noise currents need to meet DO-160 standards [16]. Then, the CM filter corner frequency can be calculated as (14). In (14), $I_{std(f_{peak})}$ and $Z_{CM(f_{peak})}$ are the EMI standard defined noise current limit level and the CM noise propagation path impedance at $f_{peak}$, respectively. The filter type is indicated by $k$ ($k = 2$ and $k = 4$ indicate single and two stage LC filters, respectively).

The relationship between filter corner frequency $f_c$ and switching frequency $f_s$ is summarized as shown in Fig.12. From Fig. 12, several findings are observed: When 20 kHz< $f_s$<150 kHz, $f_c$ and $f_s$ have a non-linear relationship, some preferred $f_s$ exists such as 140 kHz. When 150 kHz< $f_s$<2 MHz, if single stage LC filter is applied, $f_c$ has slight change as $f_s$ increases. If two or multiple stage LC filters are applied, $f_c$ will quickly increase as $f_s$ increases. This provides a guideline for switching frequency and EMI filter type selection. Fig. 13 shows the design results in [17] with two stage filter applied. It shows a similar trend as the calculation results above.



(a)



(b)

Fig. 12. Calculated corner frequency versus switching frequency, (a) single stage LC filter applied, (b) two-stage LC filter applied.

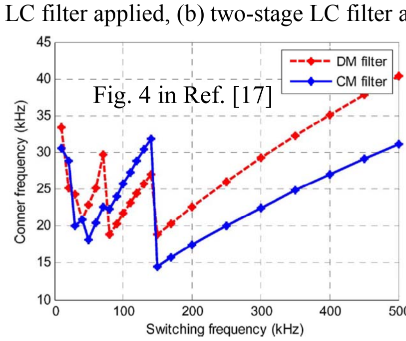
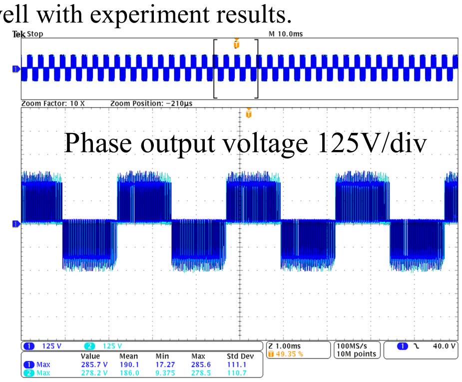


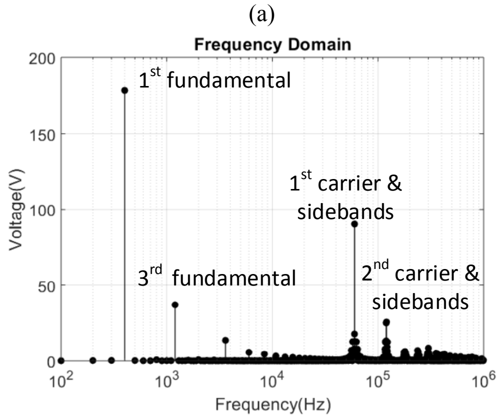

Fig. 13. Design results of corner frequency versus switching frequency in Fig. 4 of [17].

## V. EXPERIMENT RESULTS

Two three-level ANPC inverters are constructed to verify the presented models and analysis. The dc input voltage is 400 V. The ac output fundamental frequency is 400 Hz and carrier frequency is 60 kHz. The NTSV scheme shown in Fig. 2 is applied. Modulation index is 0.9 and load power factor is 0.99. Fig. 14(a) shows the phase output voltage, and Fig. 14(b) is the harmonic spectrum of this voltage. Fig. 15 is the calculated harmonic spectrum. Comparing Fig. 14(b) and Fig. 15, all the calculated harmonics frequency and amplitude match well with experiment results.




(a)




(b)

Fig. 14. (a) Phase output voltage, (b) harmonic spectrum of the experimental phase output voltage.

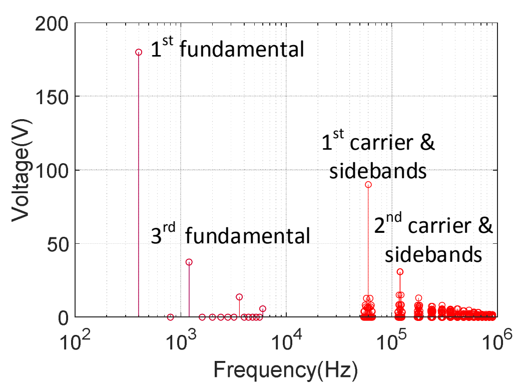
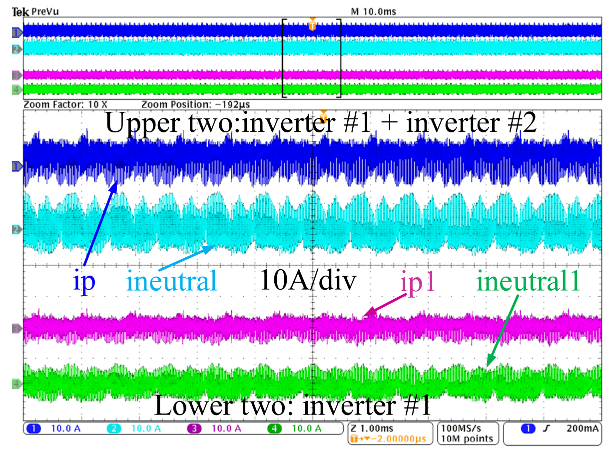
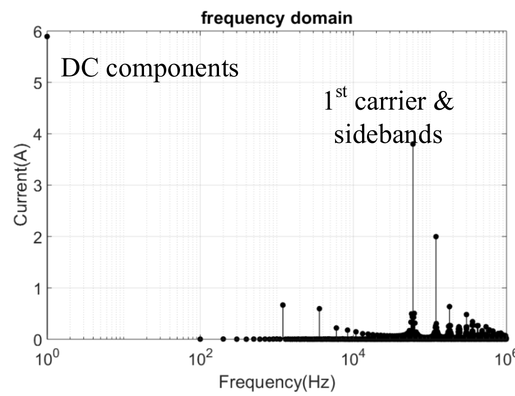



Fig. 15. Calculated voltage harmonic spectrum.

Fig. 16(a) shows the positive and neutral line input currents, and Fig. 16(b) is the harmonic spectrum of positive line input current. Fig. 17 is the calculated harmonic spectrum, which matches well with the results in Fig. 16(b). Fig. 18 summarizes the dc-link capacitor ripple current rms value for different interleaving angles. This trend also matches the theoretical analysis in Fig. 11(a) for high modulation index high power factor and case.




(a)




(b)

Fig. 16. (a) Positive and neutral line input currents, (b) harmonic spectrum of the experimental positive line input current.

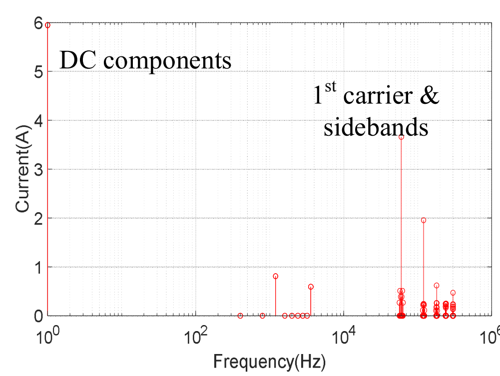



Fig. 17. Calculated positive line current harmonic spectrum.

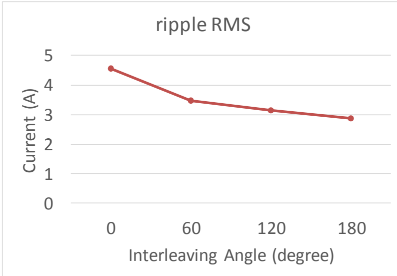



Fig. 18. Current RMS value vs. interleaving angle.

## VI. Conclusion

A comprehensive analytical analysis of the ac and dc side harmonics of three-level ANPC inverters with SVM scheme is presented. The analytical model to calculate the harmonics of three-level converter with SVM is developed. The ac output voltage harmonics and dc side input current harmonics characteristics are calculated and analyzed. Both the positive/negative line current and neutral line current have third order harmonics and also have richer carrier harmonics and sidebands components than a two-level inverter.

The impact of interleaving on ac side output voltage harmonics and dc side input ripple current rms value considering modulation indexes, interleaving angle and power factors are investigated. Ac side line to line voltage minimum WTHD0 is achieved when interleaving angle is around 90°. The dc-link capacitor ripple current rms value is highly dependent on converter operation condition. For high modulation index and high power factor case, the optimal interleaving angle is around 180°. For high modulation index and low power factor case, the optimal interleaving angle is around 90°. For low modulation index case, the dc-link capacitor ripple current rms value shows a complicated variation trend when the interleaving angle varies.

The EMI filter corner frequency as a function of switching frequency is analytical derived. EMI filter corner frequency of single stage LC filter shows different trend compared with that of multi-stage LC filters when the switching frequency varies in the 150 kHz to 2 MHz range.

Two three-level ANPC inverters are constructed for experimental verification. The harmonics analytical results matches well with experimental results.

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