

## Investigation of effects of ns, high intensity ion pulses on defect creation using a nuclear microprobe and Deep Level Transient Spectroscopy (DLTS)

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Ion beam irradiation creates defects in semiconductors that affect the operation of microelectronic devices by reducing carrier lifetime. Generally, the number of defects is considered to be linearly proportional to the ion fluence, but there are indications that ultra high flux radiation can deviate from this linearity. We used the Lawrence Berkeley National Laboratory's (LBNL) NDCX-II accelerator (high flux) and Sandia National Laboratories' (SNL) accelerator facilities to irradiate Si PIN and PN diodes. The SNL nuclear microprobe was used to analyze the irradiated devices and determine their charge collection efficiency (CCE). In addition, DLTS, C-V, and I-V measurements were performed to determine the difference between high and low flux irradiations.

### Irradiations: 1.1 MeV He, up to $2 \cdot 10^{12}$ ions/cm<sup>2</sup>



SNL Pelletron:



LBNL NDCX-II:

- beam rastered over the device
- fluence <<  $10^{11}$  ions/cm<sup>2</sup>
- Scanned over 1"xl" for uniform irradiation

- $10^{11}$  ions/cm<sup>2</sup>/shot in 10 ns ( $10^{10}$  ions/cm<sup>2</sup>/s)
- several shots to achieve required fluence
- much larger area is irradiated

### Analysis/defect characterization

#### IBIC

2 MeV He

Tandem microbeam: ~1  $\mu$ m beam size

Pelletron: ~3  $\mu$ m beam size

Scan size: 200x200  $\mu$ m (device is ~1 mm)

CCE measurement: bias scan from 0 V to ~50 V

Ions per bias point: ~1000-8000 (no damage)

CCE sensitivity: CCE ~ 1-k fluence ~ defects

Measures local damage

#### I-V

Very sensitive,  $I_{leakage}$  ~ fluence ~ defects

ASTM (80 C, two hours) annealing makes sure that all transient defects are removed

Measures global damage

#### C-V

Measures the number and profile of defects that can capture carriers

Cannot measure defects inside the built-in depletion layer

Measures global damage

#### DLTS

Determines the types and number of defects

Does not see defects in the built-in depletion layer

In heavily damaged devices it probes different positions and thicknesses depending on fluence.

In Si the major defects are

Vacancy oxygen complex (shallow)

- Carbon interstitial (shallow)

- Di-vacancy (shallow and deep)

- Divacancy like cluster related defects (deep)

Measures global damage

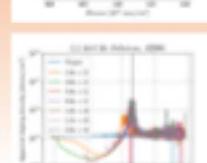


Less damage for high flux shots

Leakage current ~ number of defects



Although the CCE is larger for high flux shots, it is difficult to interpret it quantitatively. Depletion depth dependence on bias varies with damage.

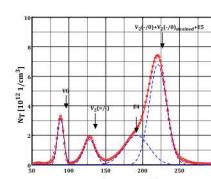


During the high flux pulse a lot of heat is deposited in a very short time. Can it cause annealing?

Simulation:

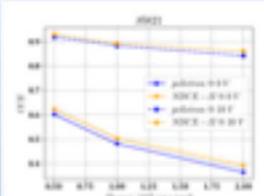
- 20 mA current into the device ( 1mm)
- 10 ns pulse
- Back of device is kept at room temperature

- On defect migration scale it takes long time to cool to cool down
- Temperature down not seem to be high enough to cause the observed annealing
- Several amps of beam is hitting the surroundings of the device which can increase temperature or modify the cooling process.

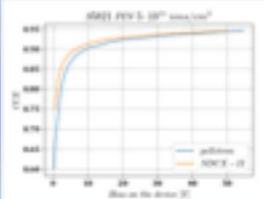


### S5821 PIN diode

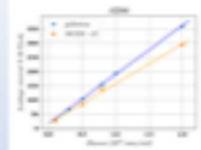
- Very low doping ~  $10^{12}$  atoms/cm<sup>3</sup>
- At 0 V the built-in depletion layer > 1.1 MeV He range
- C-V and DLTS measurements cannot get information about the defects



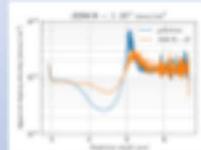
Although the CCE is larger for high flux shots, it is difficult to interpret it quantitatively. Depletion depth dependence on bias varies with damage.



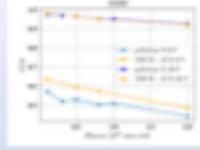
- $\sim 10^{15}$  atoms/cm<sup>3</sup> doping
- C-V and DLTS can get information about the defects for low damage



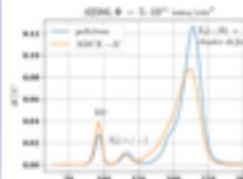
There is small difference in leakage current and the 0 V CCE. At 10 V the CCE is practically the same for the low and high flux irradiation.



The apparent doping shows an acceptor-like defect in the depletion layer (di-vacancies) and a donor-like defect at the end of range of 1.1 MeV He. This is probably a He-defect complex.



Both the apparent doping defect distribution clearly show that the high flux irradiation creates ~40% less defects than the low flux irradiation.



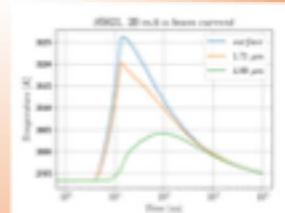
DLTS shows a decrease in the "deep peak" ( $V1(0^-)$  + clustered V2 defects) and an increase in the VO peak. This behavior was observed in the past at high temperatures irradiation by others. We also observed a similar behavior in Si BJTs. Both the increase in leakage current and decrease in CCE are due to the "deep peak" whose energy level is close to midgap.

### COMSOL heat simulation

During the high flux pulse a lot of heat is deposited in a very short time. Can it cause annealing?

Simulation:

- 20 mA current into the device ( 1mm)
- 10 ns pulse
- Back of device is kept at room temperature



### Summary

- We found that the extreme high flux irradiation creates fewer deep energy level defects than low fluence irradiation. All four measurements, leakage current, CCE, C-V, and DLTS proved it.
- This affects the leakage current linearly proportional to the fluence, and much less the CCE.
- The effect strongly depends on the device structure, especially on the doping. At lower doping the effect is stronger.
- The heat transfer simulations do not support the degree of annealing, new model needs to be developed.

### Future plans:

Use 1.1 MeV He irradiation that creates uniform damage profile deep in the device at lower level. It would allow to perform DLTS on the S5821 PIN diodes when the fluence effect is larger.