SAND2015-2412PE

Overview of Emerging Research Memory Devices

2015 ITRS-ERD Meeting

Bridging the Research Gap between Emerging Architectures and Devices

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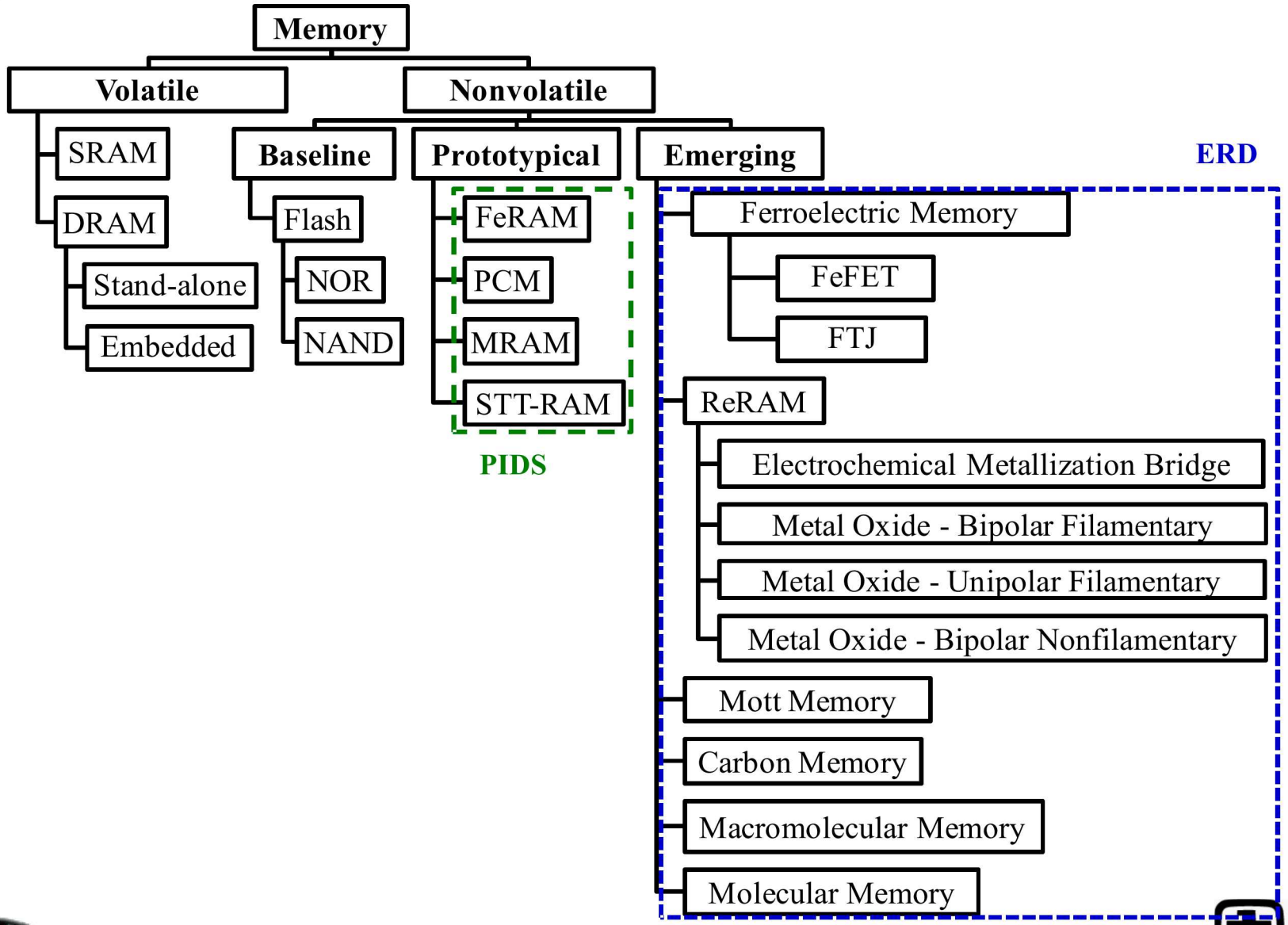
Outline

- 2013 Chapter Overview
- ERD Memory Workshop Summary

Introduction to ERD Memory

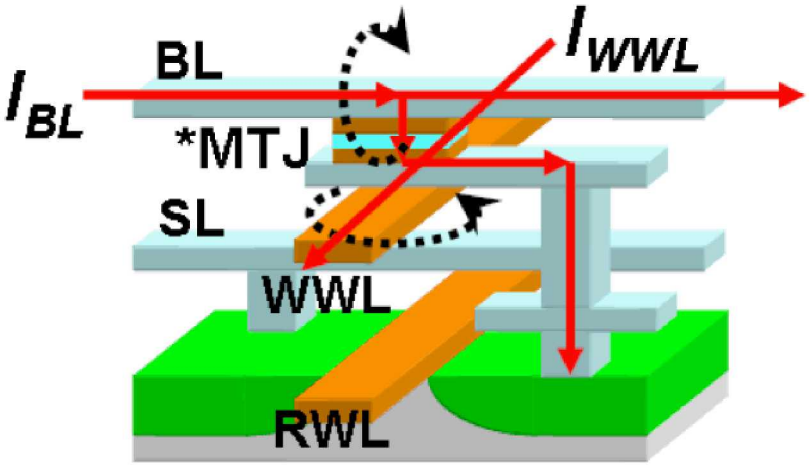
- Purpose:
  - Survey the most relevant emerging memory devices
  - Compile relevant information from the literature on device parameters, strengths, and weaknesses
- Period:
  - Every two years full update (last in 2013)
  - Workshops in off-years to collect data for next version
- Audience:
  - Foundries and Fabless Semiconductor Companies
  - Researchers from Academic Community
  - Government and Corporate Laboratories
- Target Applications:
  - Storage Class Memory: latency gap between DRAM and hard-disk drives (or NAND)
  - ITRS 2.0: Will include additional applications: Such as Internet of Things

2013 ERD Memory Entries

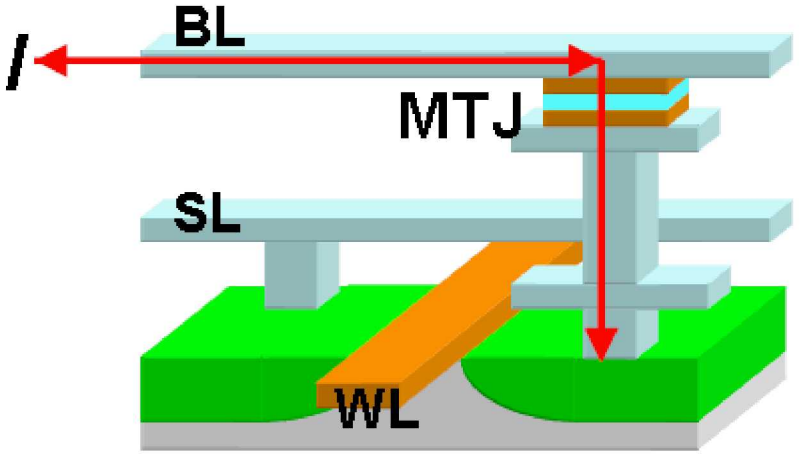


Prototypical Magnetic Memories

Conventional MRAM

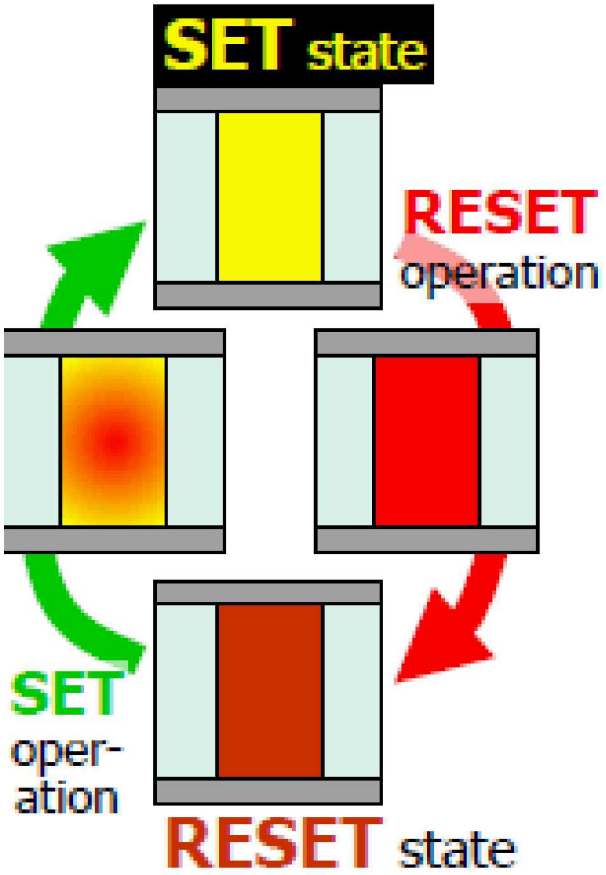


STT-RAM



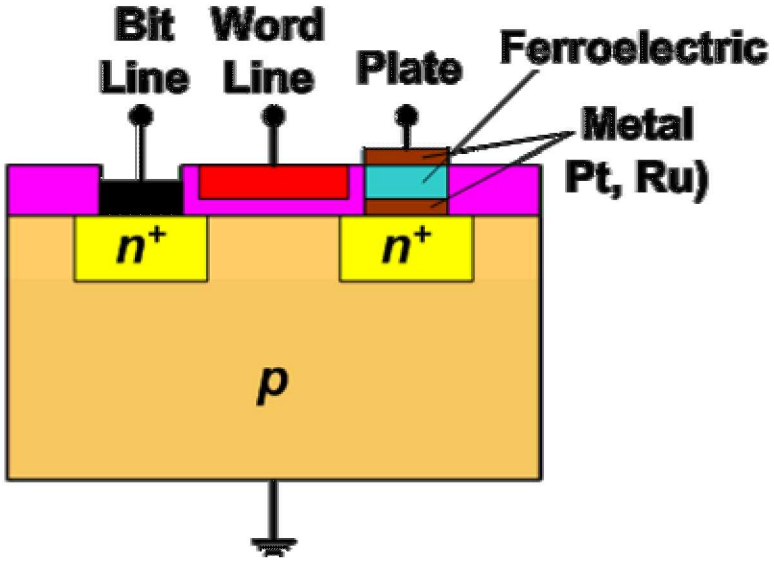
Prototypical Memories

Phase Change Memory



G. Burr, ERD Memory Workshop 2014

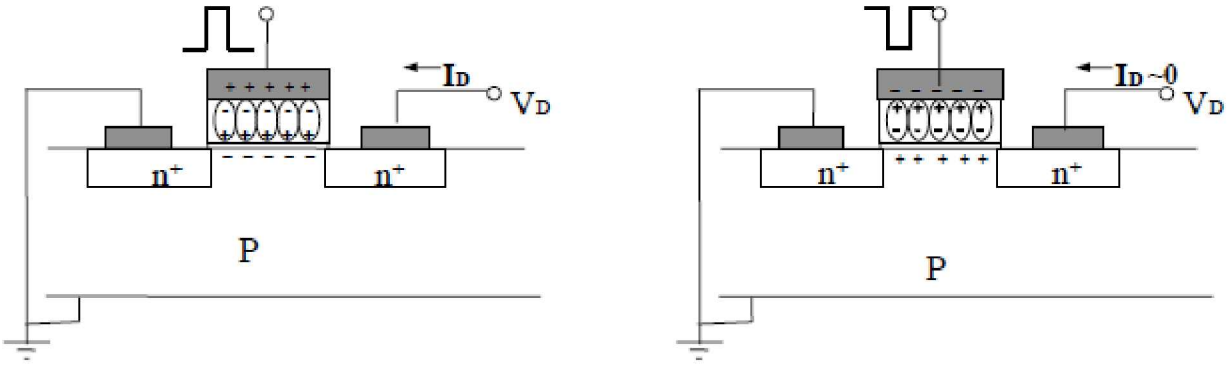
Ferroelectric RAM



Courtesy D.K. Schroder

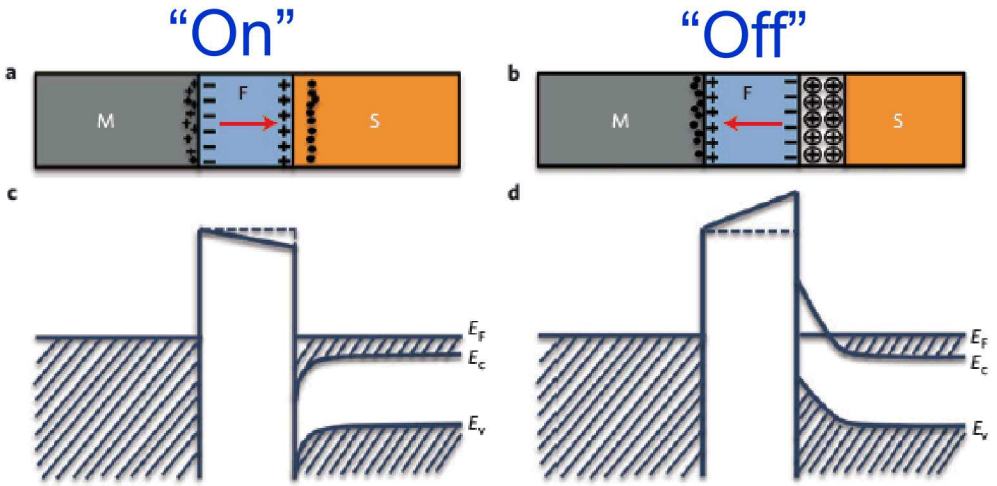
Emerging Ferroelectric Memories

Ferroelectric FET



TP Ma, ERD Memory Workshop 2014

Ferroelectric Tunnel Junction



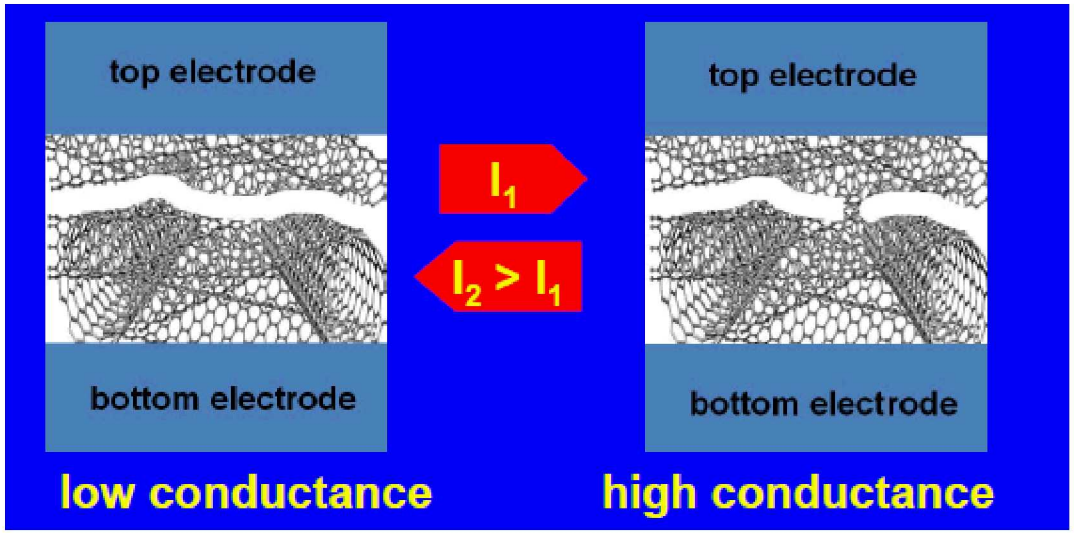
Wen et al, Nature 2013

Carbon Memory

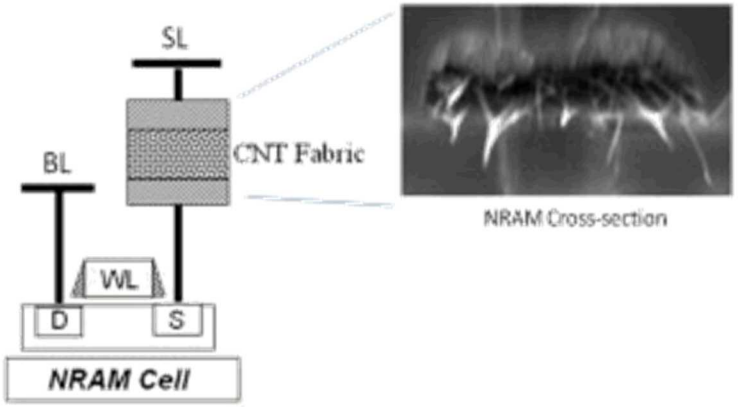
Three material systems

1. **Nanotube (single nanotube and layers)**
2. **Graphene**
3. **Amorphous carbon based resistive memory**

Many possible mechanisms!

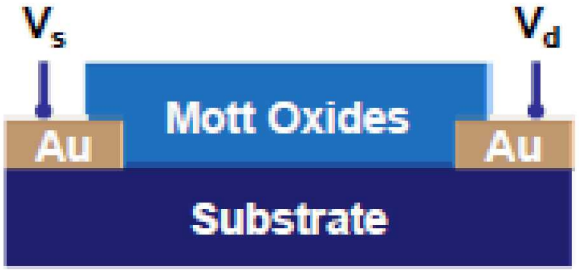


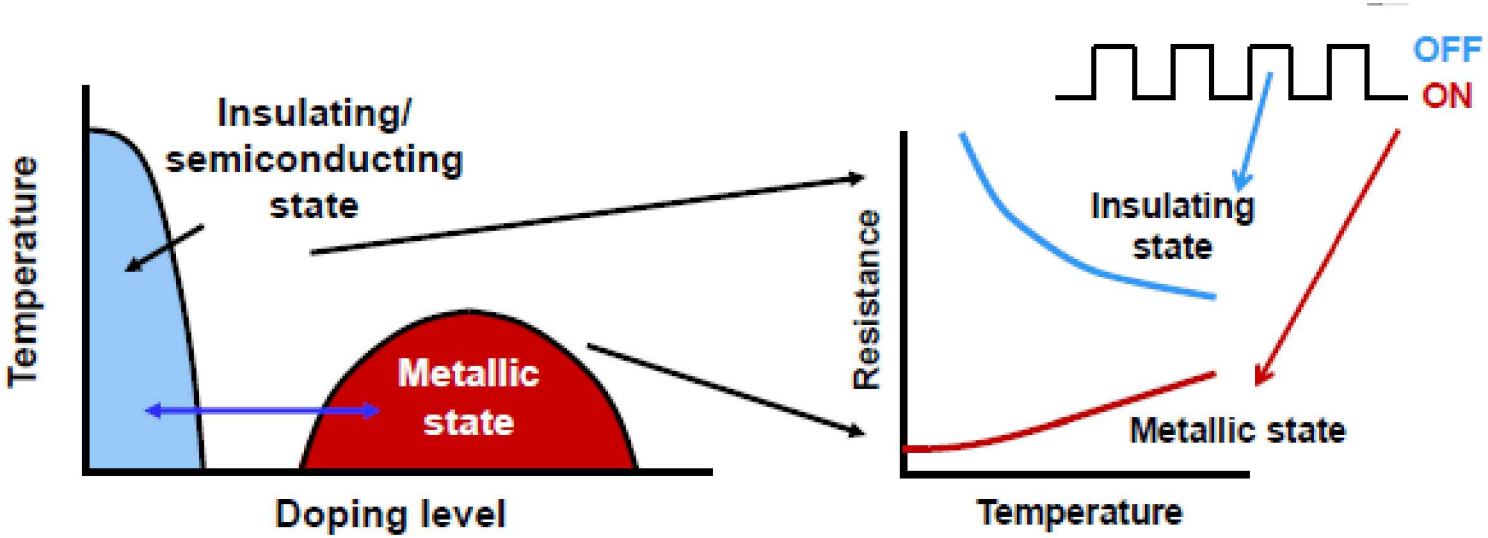
Kreupl, ERD Memory Workshop, 2014



nantero.com

Mott Memory


V_s
V_d
Mott Oxides
Au
Au
Substrate

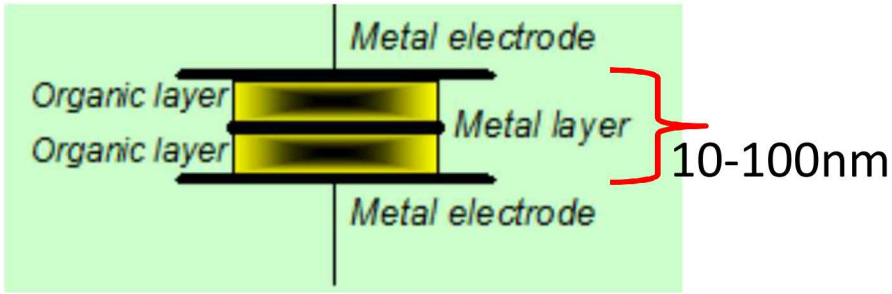

Temperature
Insulating/
semiconducting
state
Metallic
state
Doping level
Resistance
OFF
ON
Insulating
state
Metallic state
Temperature

Macromolecular vs. Molecular Memory

Macromolecular (also polymer or organic)

L. P. Ma, J. Liu, and Y. Yang
"Organic electrical bistable devices and rewritable memory cells"
APPLIED PHYSICS LETTERS VOLUME 80, NUMBER 16 22 APRIL 2002

J. OUYANG, C.-W. CHU, C. R. SZMANDA, L. P. MA and Y. YANG,
Programmable polymer thin film and non-volatile memory device,
NATURE MATERIALS, Nov. 2004



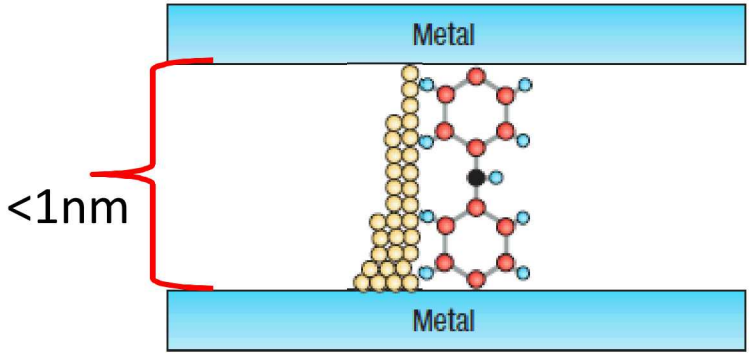
Thicker (many ML organic layer)

Emphasis: low-cost and special applications (flexible etc.)

Molecular

Read et al. "Molecular random access memory cell", APL 2001

Heath et al."A 160-kilobit molecular electronic memory", Nature 2007



Thin (1 ML organic layer)

Emphasis: Ultimate Scaling

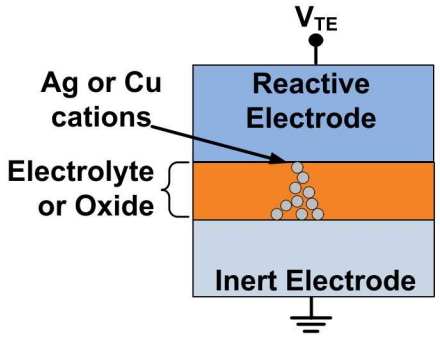
2013 ERD Memory Table (Part A)

		A. Emerging Ferroelectric Memory		B. Carbon Memory	C. Mott Memory	D. Macromolecular Memory	E. Molecular Memory
Subclass		**FeFET**	**FE Tunnel Junction**	NA	NA	NA	NA
Feature size F	Best projected	Same as CMOS transistor	<10 nm	< 5 nm	5-10 nm	5 nm	5 nm
	Demonstrated	28nm	50 nm	22 nm	110nm	100 nm	30 nm
Cell Area	Best projected	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$
	Demonstrated	$4F^2$	not available	not available	not available	$4F^2$	not available
Write/Erase time	Best projected	< 100pS	<1 ns	not available	<1 ns	< 10 ns	<40 ns
	Demonstrated	20ns 10 ns	10 ns	10 ns	2 ns	15 ns	10s , 0.2s
Retention Time	Best projected	10 yr	>10 y	not available	not available	> year	not available
	Demonstrated	$2.5x10^5$s (3 days)	3 days	168 h @ 250°C	not available	10^5 s	2 months
Write Cycles	Best projected	$>10^{12}$	10^{14}	not available	$>10^{16}$	not available	$>10^{16}$
	Demonstrated	10^{12}	$4x10^6$	$5x10^7$	~100	10^5	$2x10^3$
Write operating voltage (V)	Best projected	not available	1 V	not available	not available	~ 1	80 mV
	Demonstrated	+/- 5	2-3 V	5-6V	1.25/0.75	1.4	4V, ~±1.5 V
Read operating voltage (V)	Best projected	not available	0.1 V	not available	not available	< 0.1	0.3V
	Demonstrated	0.5V	0.1 V	1.5V	0.2	0.2	0.5V , 0.5V
Write energy per bit	Best projected	0.1 fJ	1 fJ	not available	not available	0.1 fJ	0.1 aJ
	Demonstrated	1 fJ	10 fJ	not available	~1 fJ	10 fJ	not available
Research activity		30	27	52	31	80	21

Key Updates to 2013

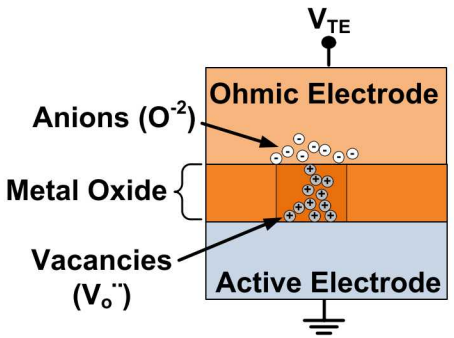
- Updated all tables with current values from the literature
- Split ReRAM into four individual categories
  - Electrochemical Metallization
  - Metal-oxide Bipolar Filamentary
  - Metal-oxide Unipolar Filamentary
  - Metal-oxide Bipolar Nonfilamentary
- Split Ferroelectric Memory into two categories
- Removed nanoelectrical-mechanical systems (NEMS) based memory due to lack of research progress
- Added carbon memory
- Added write-energy

Electrochemical Metallization Bridge



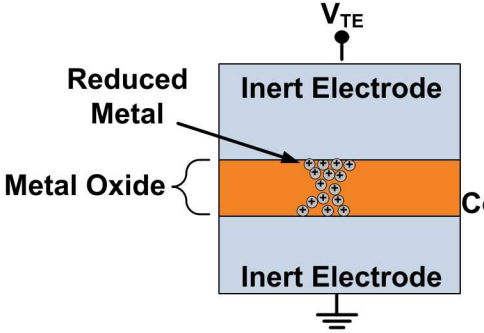
- Switching: Electrochemical formation and dissolution of Ag or Cu filament
- Cation motion (Ag or Cu)
- Chalcogenide or oxide insulating layer
- Switching depends on E-field direction
- R/W current independent of device area

Metal Oxide: Bipolar Filamentary



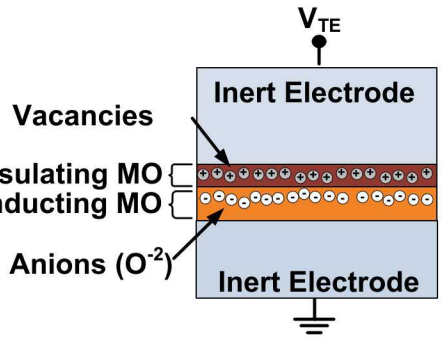
- Switching: Valence change and migration of oxygen vacancies
- Anion motion (O^{2-})
- HfO_x, TaO_x most common insulators
- Switching depends on E-field direction
- R/W current independent of device area

Metal Oxide: Unipolar Filamentary



- Switching: Thermochemical change in oxide valence state
- Anion motion (O^{2-})
- Symmetric structure
- NiO_x most common material
- Switching independent of E-field direction
- R/W current independent of device area

Metal Oxide: Bipolar Non-Filamentary



- Switching: Oxygen exchange causes Schottky barrier height change at interface
- Anion motion (O^{2-})
- Perovskite and insulating metal oxide
- Switching depends on E-field direction
- R/W currents depend on device area

2013 ERD Memory Table (Part B – ReRAM)

		A. Electrochemical Metallization Bridge	B. Metal Oxide: Bipolar Filamentary	C. Metal Oxide: Unipolar Filamentary	D. Metal Oxide: Bipolar Non-filamentary
Storage Mechanism		Electrochemical filament formation	Valence change filament formation	Thermochemical effect filament formation	Change in tunneling characteristics near interface
Feature size F	Best projected	<5nm	<5nm	not available	<10nm
	Demonstrated	20 nm (GeSe) 30 nm (CuS)	5 nm (AlOx)	35 nm	40 nm
Cell Area (2D)	Best projected	$4F^2$	$4F^2$	$4F^2$	$4F^2$
	Demonstrated	$4F^2$	$4F^2$	$4F^2$	$4F^2$
Write/Erase time	Best projected	<1ns	<1 ns	not available	10 ns
	Demonstrated	< 1ns	< 1ns	10 ns (W), 5 ns (E)	<100 ns
Retention Time	Best projected	>10yr	> 10yr	>10yr	>10 yr
	Demonstrated	1000hr 200°C	3000 hr @ 150°C	1000hr @ 150°C	4hr @ 125°C
Write Cycles	Best projected	$> 10^{11}$	$>10^{12}$	not available	$> 10^6$
	Demonstrated	10^{10}	10^{12}	10^6	10^6
Write operating voltage (V)	Best projected	<0.5V	<1V	not available	not available
	Demonstrated	0.6V	1-3V	1-3V	2V
Read operating voltage (V)	Best projected	<0.2V	0.1 V	not available	0.1 V
	Demonstrated	0.2V	0.1-0.2V	0.4 V	0.5V
Write/Erase energy (J/bit)	Best projected	not available	0.1 fJ	not available	not available
	Demonstrated	1 pJ (W), 8 pJ (E)	115fJ (W), < 1 pJ (E)	not available	1 pJ
Research activity	593 (includes all categories)				

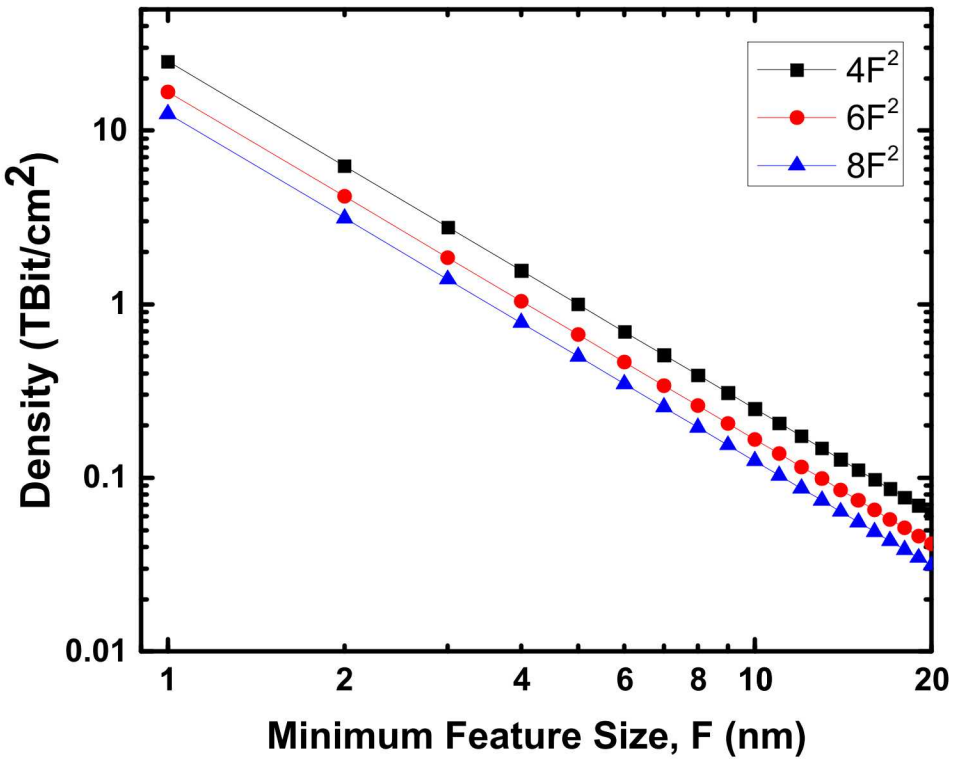
2013 ITRS ERD Memory Survey

	Overall	Scalability	Speed	Energy Efficiency	ON/OFF "1"/"0" Ratio	Operational Reliability	Room Temperature Operation	CMOS Technological Compatibility	CMOS Architectural Compatibility
ReRAM	18.7	2.9	2.5	2.1	2.2	1.6	2.5	2.4	2.4
FeFET	17.4	2.0	2.4	2.3	2.1	1.7	2.4	2.3	2.4
FTJ	17.3	2.3	2.2	2.2	2.1	1.7	2.4	2.1	2.2
Carbon-based	17.0	2.2	2.2	2.0	2.3	1.7	2.4	2.0	2.2
Mott	16.6	2.1	2.4	2.1	2.2	1.7	1.9	2.0	2.2
Macromolecular	13.9	1.8	1.7	1.7	1.6	1.3	2.2	1.7	1.8
Molecular	13.9	2.6	1.7	2.0	1.3	1.1	2.0	1.6	1.8

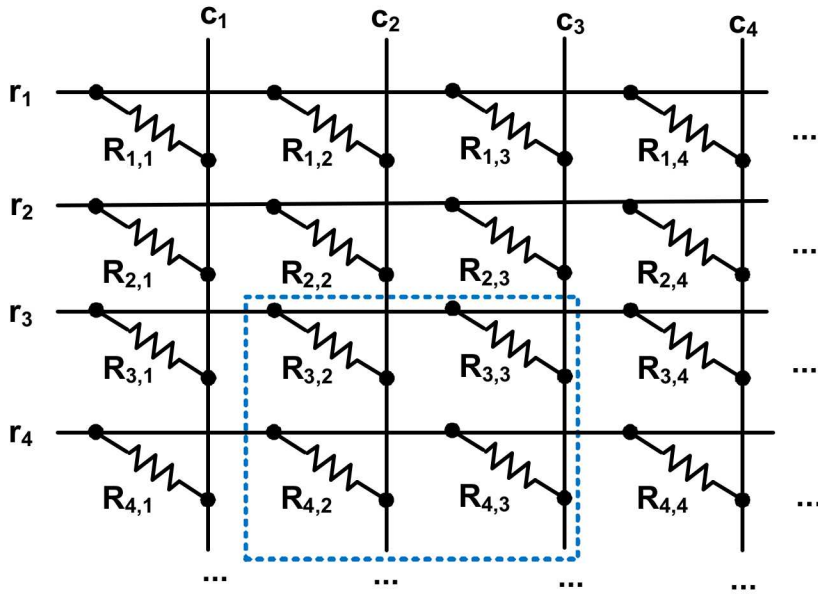
www.itrs.net

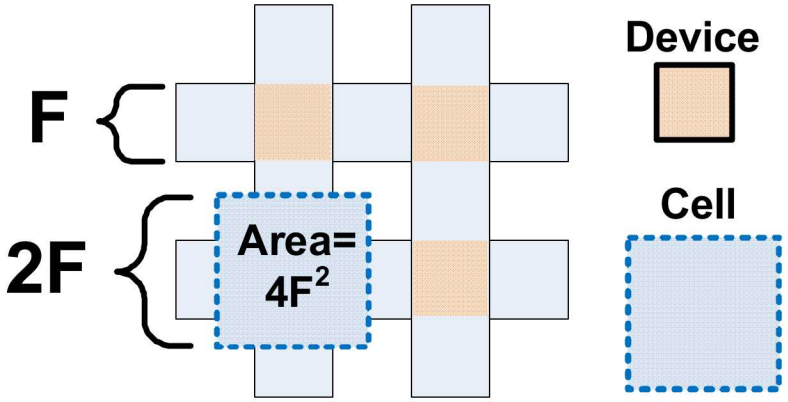
Resistive Crossbar Memories

- F=Feature size
- Max areal density possible → $4F^2$

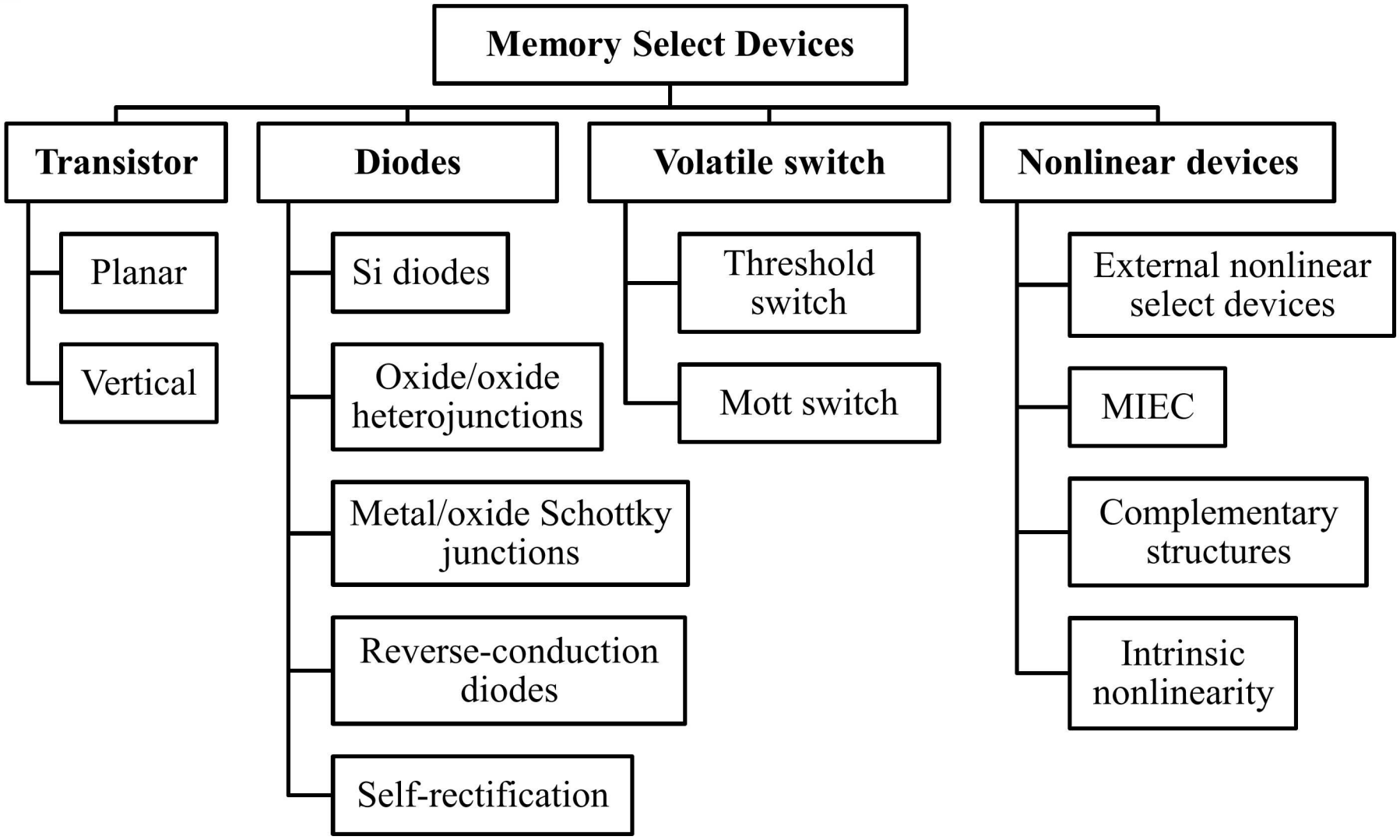


Marinella and Zhrinov, in Emerging Nanoelectronic Technologies, Wiley, 2014.





Select Device



Application Space

	Embedded NVM Replacement[1]	NAND Flash Replacement (e.g. SSD)[2]	S-Type Storage Class Memory[3]	M-Type Storage Class Memory[3]	Stand-Alone DRAM (DIMM) Replacement[4]	CMOS Integrated DRAM/Storage/Main Memory[5]
Time to Implementation	**Now**	**5 years**	**5 years**	**5-10 years**	**5-10 years**	**> 10 years**
Quantitative Requirements						
Min Bit Level Endurance	10^3-10^6	10^3	10^6	10^9	10^{16}	10^{16}
Min Bit Level Retention	10 y	6-12 months	10 y	5 days	64 ms	10 y
Max System Level Read/Write Latency	100 µs	100 µs	5 µs	200 ns	100 ns	10 ns
Max System Level Write Energy	10^4 pJ	100 pJ	25 pJ	100 pJ	100 pJ	1 pJ
Max Feature Size	180 nm	12 nm	20 nm	20 nm	20 nm	10 nm
Min 2D Layer Density	10^9 bit/cm	10^{11} bit/cm	10^{10} bit/cm	10^{10} bit/cm	10^9 bit/cm	10^{11} bit/cm
Max Cost	30 $/GB[6]	2 $/GB	4 $/GB	10 $/GB	10 $/GB	10 $/GB
Qualatative Requirements						
Performance	Low	Low	Moderate	High	High	High
Reliability	High	Low/Moderate	Moderate	Moderate	Moderate	High
CMOS Compatibility	Required	Useful/Not Req	Useful/Not Req	Useful/Not Req	Useful/Not Req	Required
BEOL Process	Required	Not Required	Not Required	Not Required	Not Required	Required
Layering Capability	Not Required	Required	Required	Useful/Not Req	Required	Required

1: Based on common embedded microcontrollers with flash based program/data memory

2: Based on modern NAND flash characteristics, considering a stand-alone module.

3: Based on SCM info from 2013 ITRS ERD Tables

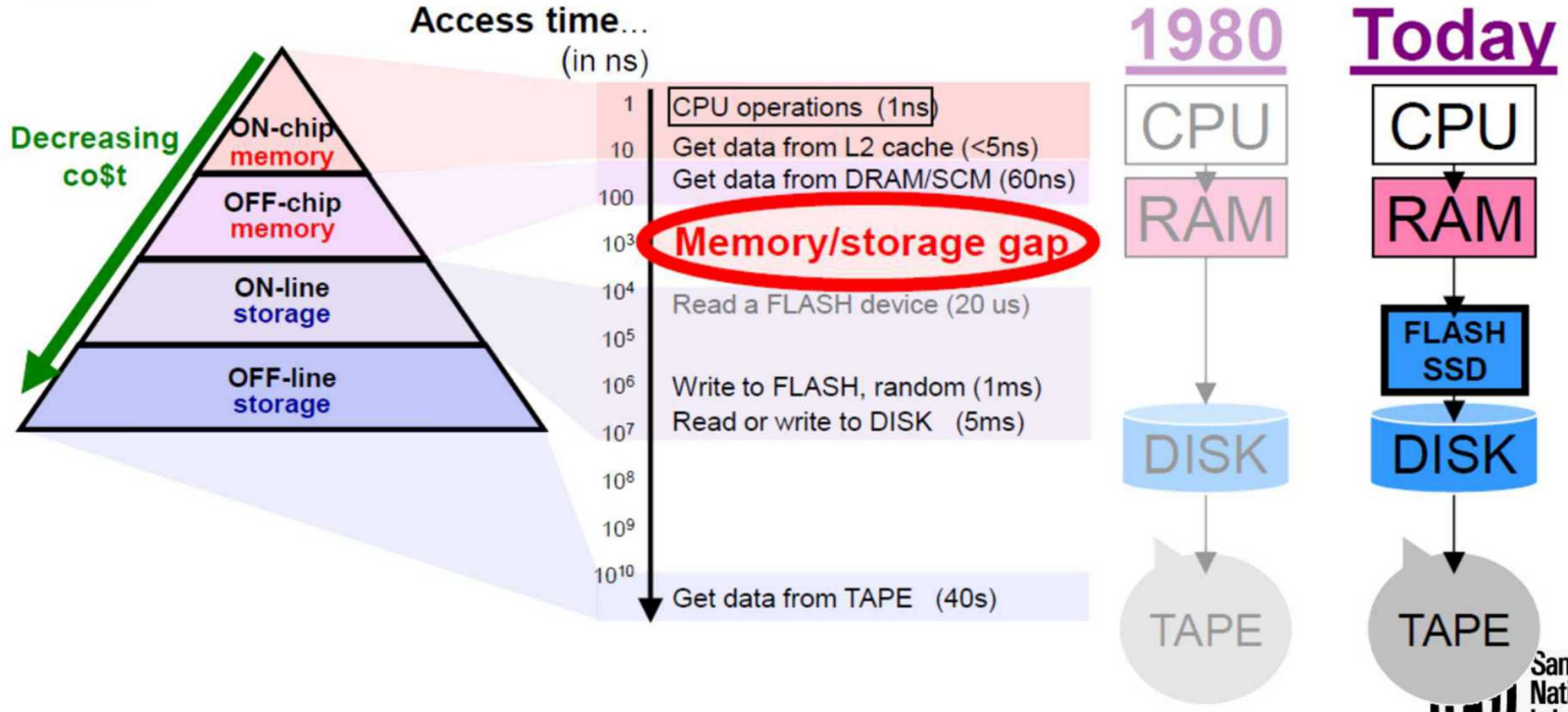
4: Based on modern DRAM characteristics.

5: High performance logic CMOS integration based on estimated requirements for data-center level processor (e.g. a "nanostore" [6]). This could also be thought of as a "univeral memory" which does not require tradeoffs in performance or reliability.

6: Based on the cost of a standalone external microcontroller memory; information on the cost per bit of flash integrated in a microcontroller is not available.

Storage Class Memory

- Major target application for emerging memory technologies
- Addresses major latency discrepancy between memory and storage DRAM to HDD (or flash)
- Workshop in 2012 to address suitability of ERD devices to SCM



Target Device/System Specs for SCM (ERD8)

Parameter	*Benchmark* [A]			*Target*	
	HDD [B]	NAND flash [B]	DRAM	Memory-type SCM	Storage-type SCM
Read/Write latency	3-10 ms	~100µs (block erase ~1 ms)	<100 ns	<200 ns	1-5µs
Endurance (cycles)	unlimited	10^3-10^5	unlimited	$>10^9$	$>10^6$
Retention	>10 years	~10 years	64 ms	>5 days	~10 years
ON power (W/GB)	0.003-0.05	~0.01-0.04	0.4	<0.4	<0.10
Standby power	~52%-69% of ON power[C]	<10% ON power	~25% ON power	<5% ON power	<5% ON power
Areal density	~ 10^{11} bit/cm^2	~ 10^{11} bit/cm^2	~ 10^9 bit/cm^2	$>10^{10}$ bit/cm^2	$>10^{10}$ bit/cm^2
Cost ($/GB)	~0.1-1.0 [D]	2	10	<10	<3-4

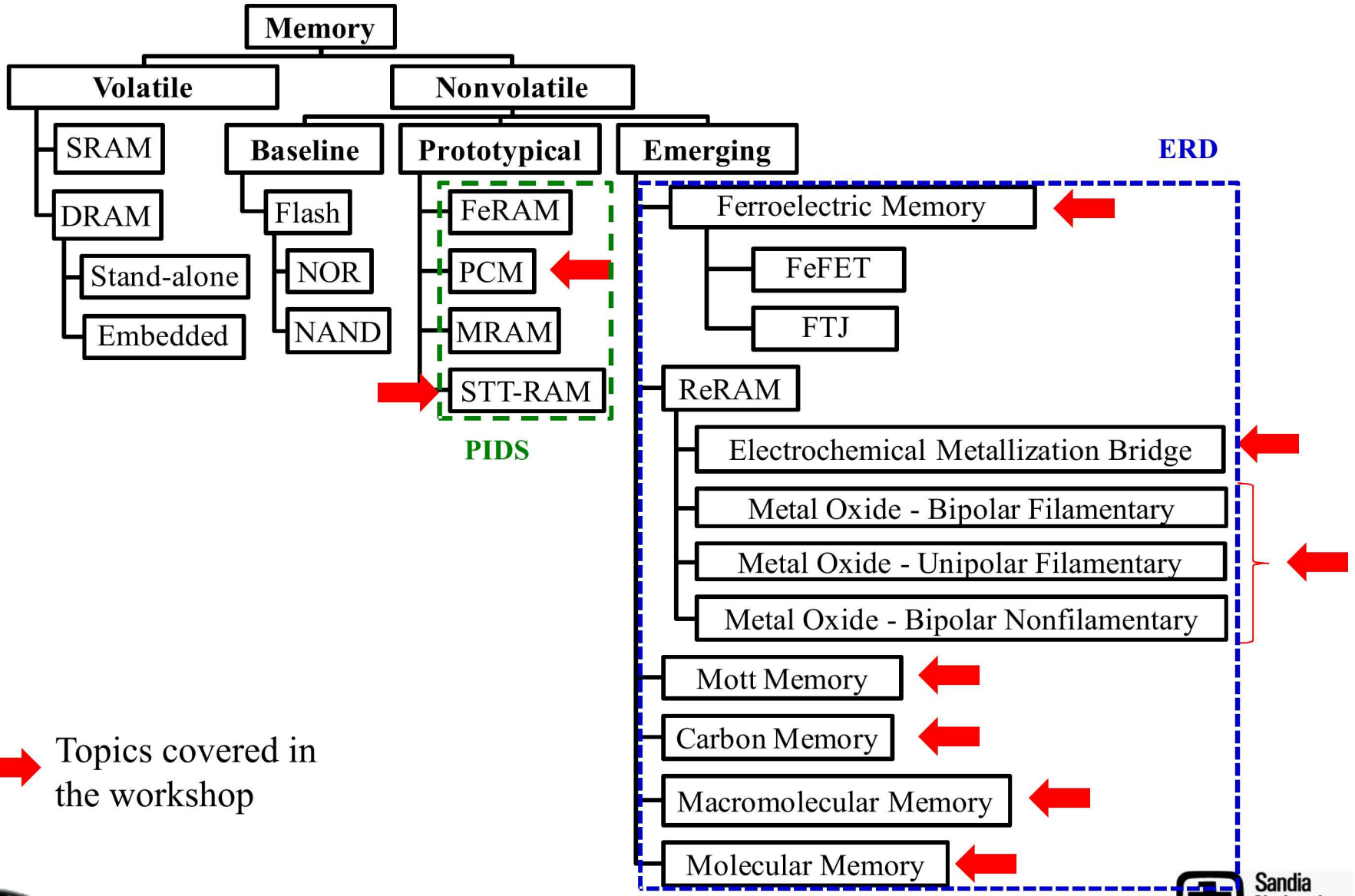
Assessment for Storage Class Memory

	Prototypical (Table ERD3)			*Emerging (Table ERD5)*					
					Redox RRAM				Others
Parameter	FeRAM	STT-MRAM	PCRAM	Emerging ferroelectric memory	Conducting bridge	Metal Oxide: Bipolar Filament	Metal Oxide: Unipolar Filament	Metal Oxide: Bipolar Interface Effects	Carbon-based Memory, Mott Memory, Macro-molecular Memory, Molecular Memory
Scalability	☹	😐	🙂	😐	🙂	🙂	🙂	🙂	?
MLC	☹	☹	🙂	☹	🙂	😐	😐	😐	?
3D integration	☹	😐	🙂	☹	😐	🙂	🙂	🙂	?
Fabrication cost	😐	😐	😐	😐	😐	🙂	😐	😐	?
Retention	😐	😐	😐	😐	😐	🙂	😐	☹	?
Latency	🙂	🙂	😐	🙂	😐	😐	😐	😐	?
Power	🙂	😐	☹	🙂	🙂	😐	☹	😐	?
Endurance	🙂	🙂	😐	😐	😐	😐	☹	😐	?
Variability	🙂	☹	😐	😐	😐	☹	☹	🙂	?

Outline

- 2013 Chapter Overview
- ERD Memory Workshop Summary

2013 ERD Memory Entries



Agenda – Day 1 (Aug. 25, Monday)

Time	Topic	Presenter
11:00am	Registration	
11:30am – 11:50am	Introduction	ERD
11:50am – 1:00pm	***Lunch talk "Potential and Challenges of RRAM"***	***Simon Wong / Stanford U.***
1:00pm – 1:30pm	PCM advocate presentation	Hsiang-Lan Lung / Macronix
1:30pm - 1:50pm	PCM friendly critic presentation	Geoff Burr / IBM
1:50pm – 2:10pm	PCM discussion	Erik DeBenedictis / Sandia
2:10pm – 2:40pm	STTRAM/MeRAM advocate presentation	Min Tai / IMEC
2:40pm – 3:00pm	STTRAM/MeRAM friendly critic presentation	Kelly Baker / Freescale
3:00pm – 3:20pm	STTRAM/MeRAM discussion	An Chen / GF
3:20pm – 3:40pm	***Break***	
3:40pm – 4:20pm	Emerging Ferroelectric Memory advocate presentation	Johannes Muller / Fraunhofer CNT; T.P. Ma / Yale U.
4:20pm – 4:50pm	Emerging Ferroelectric Memory organized discussion	Matt Marinella / Sandia
4:50pm – 5:20pm	Carbon-based Memory advocate presentation	Franz Kreupl / TU Muenchen
5:20pm – 5:40pm	Carbon-based Memory friendly critic presentation	Wabe Koelmans / IBM
5:40pm – 6:00pm	Carbon-based Memory discussion	Mike Garner / Stanford
8:00pm – 9:00pm	Evening discussion	

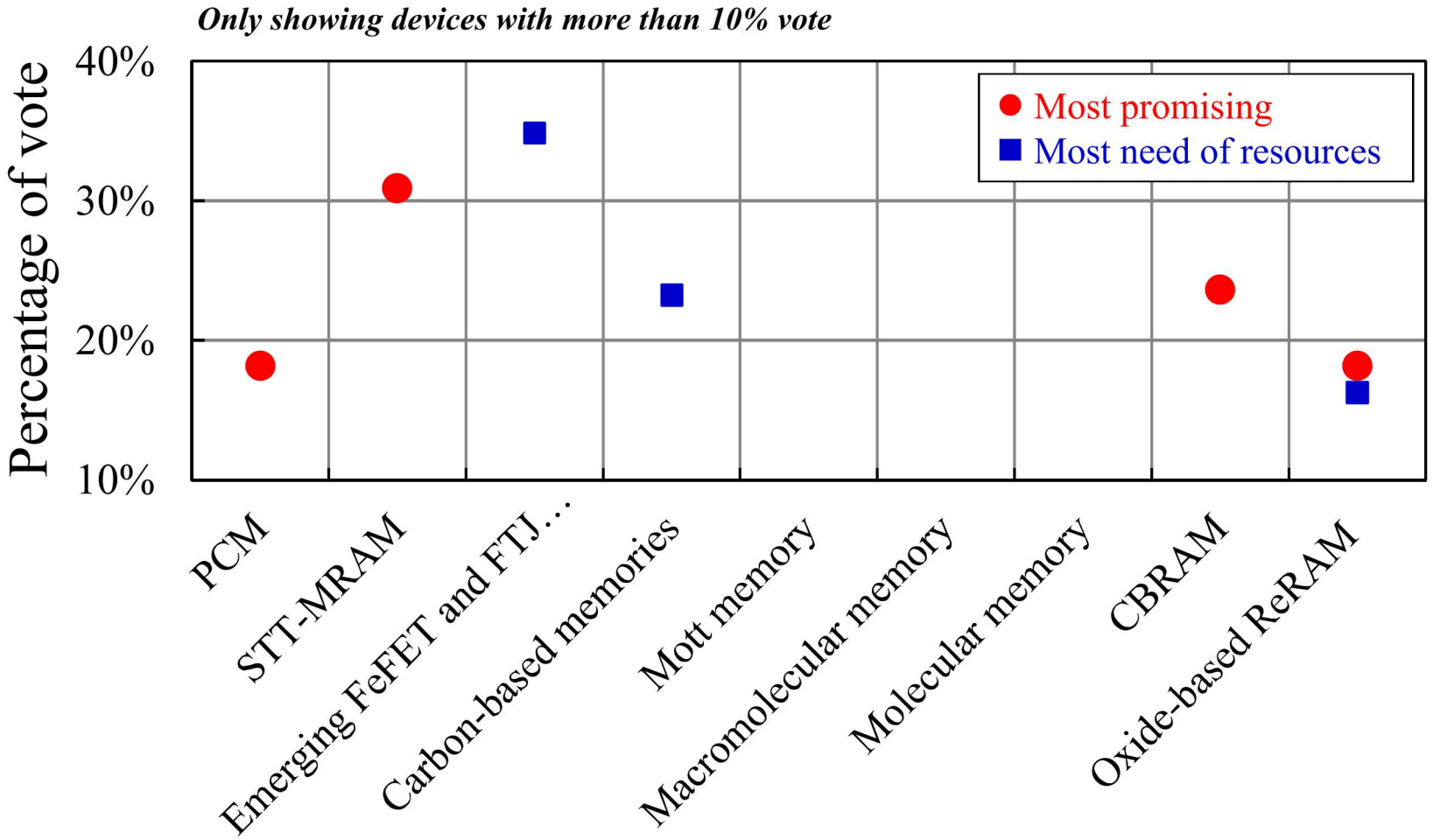
Agenda – Day 2 (Aug. 26, Tuesday)

Time	Topic	Presenter
8:00am	Breakfast	
8:30am – 8:35am	Introduction	ERD
8:35am – 9:20am	**Keynote**	**Gilbert V. Herrera / Sandia**
9:20am – 9:50am	Mott Memory advocate presentation	Xia Hong / U. Nebraska
9:50am – 10:20am	Mott Memory organized discussion	Zoran Krivokapic / GF
10:20am – 10:40am	***Break***	
10:40am – 11:10am	Macromolecular Memory advocate presentation	Stefan Meskers / TU Eindhoven
11:10am – 11:30am	Macromolecular Memory friendly critic presentation	Victor Zhirnov / SRC
11:30am – 11:50am	Macromolecular Memory discussion	Jim Hutchby / SRC
11:50am – 1:00pm	***Lunch talk "Perspective of spintronics – energy scaling and its integration with CMOS"***	***Kang Wang / UCLA***
1:00pm – 1:30pm	Molecular memory: organized discussion	Matt Marinella / Sandia
1:30pm – 2:00pm	CBRAM advocate presentation	Jun Sumino / Sony
2:00pm – 2:20pm	CBRAM friendly critic presentation	Stan Williams / HP
2:20pm – 2:50pm	CBRAM discussion	Mark Kellam / Rambus
2:50pm – 3:10pm	***Break***	
3:10pm – 3:55pm	Oxide-based RRAM advocate presentation	Malgorzata Jurczak / IMEC
3:55pm – 4:20pm	Oxide-based RRAM friendly critic presentation	Seung Kang / Qualcomm
4:20pm – 4:50pm	Oxide-based RRAM discussion	Matt Marinella / Sandia
4:50pm – 6:00pm	Emerging memory priority selection; summary	All
6:00pm	Meeting adjourn	

Workshop Objectives

- Evaluate emerging memory technologies
  - How does it work? What are the key advantages? What are the most suitable applications?
  - What is the state-of-the-art?
  - What are the major challenges and possible solutions?
  - What should industry and academia focus on?
- Identify promising candidates
  - Survey of workshop participants

Survey Result



Most Promising Devices

STT-RAM

Advantages:	Challenges:
• The closet to working memory (SRAM, DRAM) performance, • Well-understood device physics and material engineering • Significant progress in device parameters and processing in the past 5 years	• Repeatability and manufacturability needs to be confirmed • Cost/bit is a major issue; lack of MLC and 3D strategy • Limited demonstration of high temp data, including retention

Key observations:

- R&D focus has shifted from in-plane to perpendicular. Perpendicular MTJ has demonstrated the following characteristics:
- May have near “infinite” endurance for switching voltage below 650mV
- Sub-5ns read and write operation in a 8Mb test chip between -25°C and 125°C
- Thermal stability after 400°C 90min annealing, ready for BEOL CMOS process
- Switching V/I reduced to <450mV/60μA at error rate below 10^{-7} for 37nm MTJs
- Scalability down to 15nm demonstrated
- MeRAM looks exciting for reduced energy writes and endurance, but much work is needed to demonstrate useful operating window

Phase Change Memory

Advantages:	Challenges:
• Very mature (large-scale demos & products) • Industry consensus on material GeSbTe or GST • Large resistance contrast analog states for MLC (& neuromorphic computing) • Offers much better endurance than Flash • Shown to be highly scalable (still works at ultra-small F) and Back-End-Of-the-Line compatible • Can be very fast (depending on material & doping)	• RESET requires high current • Lower current with smaller features, but variability in small features broadens resistance distributions • 10-year retention at elevated temperatures can be an issue recrystallization • Device characteristics change over time due to elemental segregation, leading to device failure • MLC strongly affected by relaxation of amorphous phase, causing resistance drift

Key observations:

- The tradeoffs that bedevil PCM are almost all amenable to engineering – many of its problems could potentially be finessed with new invention.
- Unlike most of the other emerging NVMs, there don't appear to be any fundamental "physics" showstoppers for PCM…

CBRAM

Advantages:	Challenges:
• High scalability, <10nm; high density possible with $4F^2$ crossbar • High endurance • Low voltage; low switching energy • CMOS BEOL compatible process • Wide res range; MLC possible • Recent results show improved high temperature retention	• Historically poor retention • New materials may be required • Retention-switching speed trade-off • Need select device Variability • Device to device (manufacturing improvements?) • Cycle to cycle • Random telegraph noise

Key observations:

- Significant progress in recent years
- Numerous demonstrations of test macros have been demonstrated in the past two years, including Sony/Micron (presenter at workshop)
- Retention is historically problematic, but has been improved with new materials
- Low density commercial product available

Oxide-based ReRAM

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Advantages:	Challenges:
• High scalability, <10nm; high density possible with $4F^2$ crossbar • High endurance, good retention • Fast read and write; low switching energy • CMOS compatible materials & process • Resistive crossbar compatible; can be layered • Numerous test chip demos (up to 32Gbit)	• Product-level limitations • Need lower current, ~1 uA range • Forming process – want forming free • Details of mechanism under debate Variability • Device to device • Cycle to cycle • Random telegraph noise

Key observations:

- Focus of talk (an most work) is on bipolar filamentary, although unipolar and nonfilamentary are included in ERD
- Large increase in interest in the past two years; significant progress has been made
- Variability is a key problem
- Low density commercial product available (Panasonic)

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Most In Need of Resources

Emerging Ferroelectric Memory

Microsystems Science, Technology & Components

Advantages:	Challenges:
FeFET • High endurance possible • Doped HfO is highly CMOS compatible • Fast switching speed and low sw energy • Scalable FTJ • Combines adv. FeFET and ReRAM • Low switching energy • Bit is scalable and crosspoint array compatible (FET not required)	FeFET • Retention historically poor; can only optimize for endurance/retention • Discovery of FE-HfO:x relatively recent; some controversy in mechanism • Not suitable for 3D layering FTJ • Immature technology – memory properties not well understood

Key observations:

FeFET
- Promising new results have turned research focus from traditional materials (eg PZT) to doped HfO. This has created a renewed interest in FeFET
- HfO process demonstrated with slightly modified HKMG CMOS flow
- Possible to optimize for endurance or retention (difficult to get both)

FTJ (less focus in presentation)
- Interesting technology to watch, could combine advantages of RRAM with FeFET, but currently immature. Could make use of FE-HfO.

Carbon-based Memories

Advantages: (depend on memory type)	Challenges:
• High endurance (Nantero) • Good retention; high temperature operation possible (Nantero) • Scalable "to single atomic bond dimensions" • Resistive crossbar compatible – high density	• Contact resistance • Variability (similar or worse than ReRAM) • High switching voltage for certain types

Key observations:

- This category is not well understood. Many mechanisms and materials could be incl
- Two different mechanism suggested in workshop
    1. low mass density: break-junction by local evaporation of carbon and plumbing by field emission
    2. high mass density: conversion of a-C ↔ sp2-bonds
- Alternatively can be broken up by materials: nanotube, graphene, amorphous

Summary

- Successful ERD Memory Workshop in August 2014
- Report in progress, will be first distributed to ERD and workshop attendees
- Those promising has not changed
  - PCRAM
  - STT-MRAM
  - Oxide ReRAM
- "In need of resources" gave new results:
  - Oxide ReRAM (also most promising)
  - Emerging Ferrorelectric Memories
  - Carbon Memories
- Splitting CBRAM and MO-ReRAM was worthwhile – they ranked differently
- Should we create a bone-yard?
- Always interested in other feedback from ERD readers!

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Questions?

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“Other” Emerging Memories

Mott Memory

Advantages:	Challenges:
• Scalability (in theory) below 1nm • Sub-ns switching time • Tunable carrier density and band gap • Significant memory effect at moderate electric field, i.e., low-power operation • Variety of control factors for metal-insulator transition: carrier density, T, E, strain, and optical excitation	• Require growth techniques for large-scale high-quality thin film oxides; solutions exist but are not industry compatible • Precise control of material property at nanoscale with high-level of uniformity is challenging • Stoichiometry and defect control is critical

Key observations:

- It is possible to build FET-like devices with gate-modulated MIT
- Still need to find materials with sufficiently high transition temperature suitable for industry processing and applications
- Field switching MIT mechanism itself is not well understood; need other mechanisms (e.g., ferroelectrics) to maintain the transition condition for retention

Macromolecular Memory

Advantages:	Challenges:
• Option for flexible electronics • Compliance not needed • Solution processing; inexpensive materials (this claim was controversial)	• High programming voltage • Sensitive to oxygen • Switching dead time • Mechanisms not well understood • Endurance • Retention • Materials not CMOS compatible – difficulty surviving BEOL temperatures

Key observations:

- Category not well understood – mixed with molecular to some degree
- Mechanisms reported ften similar to ReRAM

Need better definition in 2014 roadmap

- Option 1: Combine with Macromolecular
- Option 2: Drop
- Option 3: Boneyard (Geoff)

Molecular Memory

Advantages:	Challenges:
• Ultimate scalability, information stored in single molecule	• Lack of device demonstration • Experiments very difficult – contact tends to obscure molecule results • Poor demonstrated endurance and retention • Progress on true single molecule switching very limited

Key observations:

- Category not well understood – mixed with macromolecular to some degree
- Many historic demonstrations of interest turned out to be parasitic/contact effects, possibly ionic switching
- Single molecule conduction should be in pA range (Victor)