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Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy-Ion Irradiation

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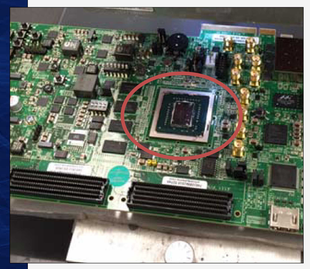
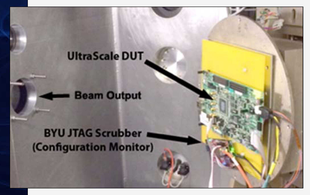
Abstract

This study examines the single-event response of the Xilinx 20 nm Kintex UltraScale Field-Programmable Gate Array irradiated with heavy ions. Results for single-event latch-up and single-event upset on configuration SRAM cells and Block RAM memories are provided.

Introduction



Kintex UltraScale DUT (circled) mounted on a commercially available KCU105 evaluation card.



Test setup inside the LBL vacuum chamber

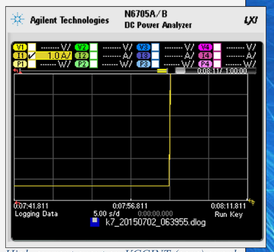
This study examines the single-event effects susceptibility of the Xilinx Kintex UltraScale Field-Programmable Gate Array. The Kintex UltraScale is the latest FPGA offering from Xilinx, built on TSMC's 20 nm, 20SoC process [1]. The purpose of this work is to determine the flight-worthiness and feasibility of utilizing these parts in space environments.

XCKU040-2FFVA1156 Characteristics [2]

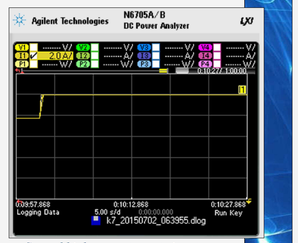
Logic Cells	424,200
CLB Flip-Flops	484,800
CLB LUTs	242,400
Maximum Distributed RAM (Mb)	7.0
Block RAM/FIFO w/ECC (36Kb each)	600
Total Block RAM (Mb)	21.1
CMTs (1 MMCM, 2 PLLs)	10
I/O DLLs	40
Maximum HP I/Os (up to 1.8V)	416
Maximum HR I/Os (up to 3.3V)	104
DSP Slices	1,920
System Monitor	1
PCIe Gen3 x8	3
GTH 16.3Gb/s Transceivers	20

Device SEL Results

- The device passes SEL testing at LET = 79.2 MeV-cm^2/mg at 95° C and maximum biases, but only when the hardware reset (PROG) pin is asserted for the duration of the irradiation (this is not a typical mode of operation).
- A high-current event on the core supply (VCCINT, 0.95V) was observed which caused the power supply to draw its maximum current (10A).
- Current events would not clear through configuration scrubbing nor through assertion of the device's reset (PROG) pin.
- No damage or loss of functionality was observed, but have not yet fully exercised all circuits; latent damage is also a possibility.
- Event exceeded the capacity of the power supply to deliver current, which made event characterization and investigation difficult.
- A second high-current error signature was observed where the core VCCINT supply drew 8A of current but appeared to remain functional. Upon trying to re-configure the device, VCCINT rose sharply to the supply maximum (10A).
- All other voltage rails appear to be latchup-free.



High-current event on VCCINT (core) supply

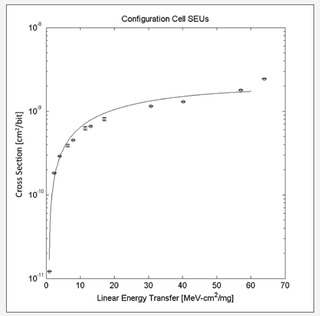


Second high-current event signature

SEU Results

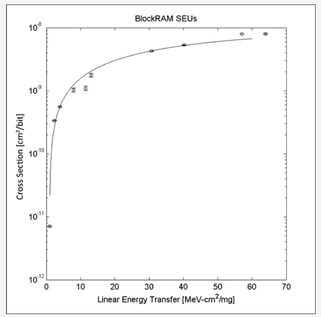
I. Configuration Memory Bits

- Static configuration memory test performed by configuring, irradiating, and then reading back the device.
- 95,343,200 configuration bits assumed; this number is about 10% lower than the actual number of bits in the configuration bitstream to account for overhead bits that have no function in the device.
- Readback of the configuration memory state occurred frequently (on average, every 15 seconds) while irradiation was occurring in order to minimize the possibility of masked upsets through coincident SEUs occurring on one memory cell.



II. Block RAM

- Block RAM test was performed by configuring, irradiating, and then reading back the device.
- BlockRAM was not exercised in the design or clocked during irradiation.
- 25,221,888 Block RAM bits were analyzed.
- A Block RAM reset-like phenomenon would occasionally occur that would affect and clear (to zero) clusters of 1024 bits. These events were removed from the analysis.



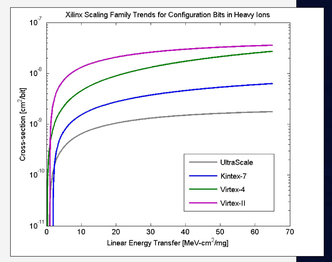
Proton Sensitivity Extrapolated from Heavy Ion Data

- The Edmonds model [4] estimates the upper bound proton sensitivity cross-section from heavy ion data using a generic charge collection efficiency function.
- Using Method 3 described in [5], the heavy-ion cross-section curve is integrated over LET values to perform this calculation.
- SEU data from the heavy-ion Weibull curves for configuration memory and Block RAM were used in the calculation of the proton cross-section estimate.
- The estimate correlates well to the proton results published in [6].

	Configuration Memory	Block Ram
Upper Bound Proton Estimate Cross Section (cm^2 bit)	1.87E-15	4.74E-15

Scaling Trends

- The device performed consistently with expectations from previous scaling trends in Xilinx FPGA families.
- Device shows ~2x lower cross section for configuration bits than previous 28 nm generation family.
- Rates assume a GEO orbit, solar minimum conditions, and 100 mils of aluminum shielding.



	Configuration Memory Rates			Weibull Parameters			
	per bit, per day	Improvement*	Node	Onset (MeV-cm^2/mg)	Limit (cm^2/bit)	Width (MeV-cm^2/mg)	Power
Virtex-II	3.99E-07	1	130 nm	1	4.37E-08	33	0.8
Virtex-4	2.63E-07	1.517	90 nm	0.2	1.76E-07	400	0.98
Kintex-7	1.41E-08	28.298	28 nm	1.9	1.43E-08	125	0.8
UltraScale	7.56E-09	52.778	20 nm	0.8	2.00E-09	27	0.88

** compared to Virtex-II*

Beam Parameters

Ion Species	Energy (MeV/u)	Incident LET (MeV-cm^2/mg)
B	10	0.98
O	10	2.38
Ne	10	3.96
Si	10	7.88
Ar	10	13.04
Cu	10	30.71
Kr	10	40.15
Xe	10	63.91
Ho	15	79.20

The part was irradiated with heavy ions for SEU at Lawrence Berkeley Laboratory's 88-inch cyclotron with effective LETs from 0.98 to 63.91 MeV-cm^2/mg in May 2015 and for SEL at Texas A&M's K500 cyclotron with a LET of 79.2 MeV-cm^2/mg in July 2015.

For SEU testing with neon, tilt angles of up to 65 degrees were utilized to obtain higher effective LETs.

On-Orbit Rates

CREME96 [3] estimates for configuration memory and Block RAM SEUs is shown below for a GEO orbit, solar minimum conditions, and 100 mils of Al shielding:

	Configuration Memory	Block RAM
per bit, per day	7.54E-09	2.48E-08
per device, per day	7.19E-01	6.26E-01

References

[1] M. Santarini, "Xilinx Ships Industry's First 20-nm All Programmable Devices," *Xcell Journal*, no. 86, pp. 9-15, 2014.
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