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Device-Level Thermal Management of Gallium Oxide Field-Effect Transistors

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***Abstract*— The ultra-wide bandgap (~4.8 eV) and melt-grown substrate availability of β-Ga_2O_3 gives promise to the development of next generation power electronic devices with dramatically improved size, weight, power, and efficiency over current state-of-the-art wide bandgap devices based on 4H- SiC and GaN. Also, with recent advancements made in GHz frequency RF applications, the potential for monolithic or heterogenous integration of RF and power switches has attracted researchers' attention. However, it is expected that Ga_2O_3 devices will suffer from self-heating due to the poor thermal conductivity of the material. Thermoreflectance thermal imaging and infrared thermography were used to understand the thermal characteristics of a MOSFET fabricated via homo-epitaxy. A 3D coupled electro-thermal model was constructed based on the electrical and thermal characterization results. The device model shows that a homo-epitaxial device suffers from an unacceptable junction temperature rise of ~1500°C under a targeted power density of 10 W/mm indicating the importance of employing device level thermal managements to individual Ga_2O_3 transistors. The effectiveness of various active and passive cooling solutions was tested to achieve a goal of reducing the device operating temperature below 200°C at a power density of 10 W/mm. Results show that flip-chip hetero-integration is a viable option to enhance both the steady-state and transient thermal characteristics of Ga_2O_3 devices without sacrificing the intrinsic advantage of high-quality native substrates. Also, it is not an active thermal management solution that entails peripherals requiring additional size and cost implications.**

***Index Terms*—Electronics cooling, Gallium oxide, β-Ga_2O_3, Infrared imaging, Thermal management, Thermoreflectance, Flip-chip devices.**

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I. Introduction

β-gallium oxide (Ga_2O_3) has a bandgap of 4.6-4.9 eV which is larger than that for wide bandgap (WBG) materials such as 4H-silicon carbide (SiC) and gallium nitride (GaN) [1]–[4]. Devices based on this ultra-wide bandgap (UWBG) material can withstand a far larger critical electric field (6-8 MV/cm) [5] before avalanche breakdown when compared to WBG devices. This should enable device scaling to design next generation power switching application under high voltage operation. The advantage of Ga_2O_3 in power switching application can be understood from comparing Baliga's figure of merit for Ga_2O_3 with that of Si (3000×), SiC (10×) and GaN (4×) [6]. Moreover, one of the major advantages for Ga_2O_3 is the feasibility of synthesizing high quality single crystalline substrates using melt growth techniques such as Czochralski [7], [8], floating-zone [2], [9], [10], and edge defined film-fed growth (EFG) methods [11]. Due to these advantages, Ga_2O_3 has generated significant interest in high voltage switching applications. Wong et al. [12] have already demonstrated Ga_2O_3 metal oxide semiconductor field effect transistors (MOSFETs) with breakdown voltages exceeding 750V. In addition, the large critical electric field (E_{cr}) allows aggressive scaling of the Ga_2O_3 FETs which opens up possibility for radio frequency (RF) applications [5], [13] . The potential benefit of using Ga_2O_3 in RF applications can be seen from Johnson's figure of merit (JFOM/Power-frequency product) of Ga_2O_3 (3× of GaN) [14], as shown in table I. Green et al. had demonstrated an output power density of 0.23 W/mm with a power added efficiency (PAE) of 6.3% at 800 MHz utilizing passive source and load tuning. More recently, using a thin and highly doped channel, Chabak et al. reported a drain to source current of 275 mA/mm at a drain to source bias (V_{DS}) of 10 V for Ga_2O_3 MOSFETs that exhibited record-high f_t/f_{max} = 5.1/17.1 GHz [5]. It should be noted that with potential improvements in contact fabrication and channel mobility [15], the feasibility of Ga_2O_3 applications in the RF sector will be enhanced. This may lead to potential circuit level implications by realizing a monolithic integration of RF and power devices [5], [13], [16].

Table I. Material properties and the Johnson's figure of merit (JFOM) for Si, 4H-SiC, GaN and Ga_2O_3 [14].

	Si	4H-SiC	GaN	Ga_2O_3
E_g (eV)	1.1	3.3	3.4	4.6-4.9
μ_n (cm^2/V-s)	1400	1000	2000	100-200
E_{cr} (MV/cm)	0.3	2.5	3.3	8
ε	11.8	9.7	9.0	10.0
Normalized JFOM $E_{cr}^2.v_{sat}^2/4\pi^2$	1	278	1089	2844
κ at 300 K (W/m-K)	150	370	210	27 [010] 11 [110]

However, as shown in table I, the extremely low thermal conductivity (κ) of Ga_2O_3 (11-27 W/m-K at room temperature [17], [18]) may limit the commercial viability of this materials system for ultra-high power density applications. Singh et al. demonstrated the effect of self-heating and elevated operating temperature on the RF performance of field-plated Ga_2O_3 MOSFETs [19]. Due to the lower thermal conductivity, the self-heating effect in Ga_2O_3 devices will be significantly intensified as compared to WBG counterparts. Therefore, device-level thermal management solutions suitable for Ga_2O_3 devices must be developed to enable device operation at acceptable junction temperatures under nominal service conditions [20]. Various techniques used by the GaN community such as diamond integration and microchannel cooling can be leveraged in the Ga_2O_3 technology [20].

This work focuses on both the electro-thermal characterization and the thermal management of a Ga_2O_3 metal-oxide-semiconductor field-effect transistor (MOSFET). The goal is to achieve an operating junction temperature (T_j) less than 200°C (adapted from GaN RF applications [21]–[23] for commercial and military applications) under a targeted power density of ~10 W/mm (2× of the nominal power density for GaN-on-SiC based power amplifiers [21]–[23]). It is to be noted that present Ga_2O_3 RF devices have not yet demonstrated power densities close to those of GaN devices. However, Ga_2O_3 devices are likely to target a many-fold increase in power over SiC applications (Mastro et al. [24]). Recently, Cheng et al. used 10 W/mm power density to demonstrate the effect of thermal boundary resistance on the thermal performance of a Ga_2O_3 device [25]. Considering these facts, 10 W/mm was chosen as the target power density for this study. Similarly, the junction temperature target range of 200°C - 250°C comes from GaN legacy. Recently Tadjer [26] used 175°C as a target junction temperature, while the silicon industry uses 125°C as the maximum junction temperature. Accounting these, and in absence of an agreed upon industry standard, 200°C was used as maximum allowable junction temperature in this work. To accomplish this goal, the effectiveness and practicality of a range of top-side and bottom side active and passive cooling solutions were studied.

Previous efforts on the thermal management of GaN-based high electron mobility transistors (AlGaN/GaN HEMTs) have focused on bottom-side cooling via replacement of the non-native Si or SiC substrate material with high thermal conductivity diamond. Recently, Cheng et al. [25] demonstrated successful integration of Ga_2O_3 thin membrane with diamond to mitigate the self-heating effects. Using thermal simulation, Pomeroy et al. [27] showed that a temperature reduction of 75% is possible by thinning down the Ga_2O_3 substrate. Tadjer et al. showed a 20× improvement in power to reach 175°C by replacing the 200 µm thick Ga_2O_3 substrate with a 50 µm thick Cu substrate [26]. Apart from performing bottom side cooling studies similar to these, microchannel cooling near the device channel was pursued for efficient heat removal in GaN device technology [22], [28]–[31]. Bottom-side cooling methods were proven to work well for AlGaN/GaN HEMTs since selective etching allows locating the cooling medium in close proximity (1-4 µm) to the heat source. GaN material possesses a reasonable thermal conductivity to begin with. For these reasons, in recent years, top-side cooling techniques such as flip-chip integration have not been very attractive for GaN devices. However, as the availability of low cost and high-quality single crystal substrate is one of the most important advantages of Ga_2O_3, top side cooling techniques that preserve the native substrate were also investigated in this work. Pomeroy et al. showed an 18% reduction in thermal resistance using nanocrystalline diamond and a 44% reduction in thermal resistance using the diamond carrier to flip chip bond [27]. However, due to the anisotropic thermal conductivity of Ga_2O_3, these relative improvements are expected to be different for the present study (with a $(\bar{2}01)$ substrate orientation) as compared to devices studied by Pomeroy et al. (with a (010) substrate orientation). Nanocrystalline diamond passivation, air jet impingement cooling, and flip-chip hetero-integration [32]–[35] were evaluated to determine the feasibility of achieving the targeted junction temperature rise under 10 W/mm power dissipation.

II. ELECTRO-THERMAL ANALYSIS OF THE GALLIUM OXIDE MOSFET

A. Device description

The tested Ga_2O_3 MOSFET and its current-voltage (I-V) characteristics are shown in Fig. 1. The substrate is an EFG-grown, $(\bar{2}01)$ oriented, Ga_2O_3 substrate unintentionally doped with Si with a carrier concentration of 2.8×10^{17} cm^{-3}. The active channel layer is a 200 nm epitaxial layer grown by ozone molecular beam epitaxy (MBE) with an effective doping of 2.0×10^{17} cm^{-3} on a semi-insulating substrate. Details of the device fabrication steps and electrical characteristics have been reported elsewhere [36].

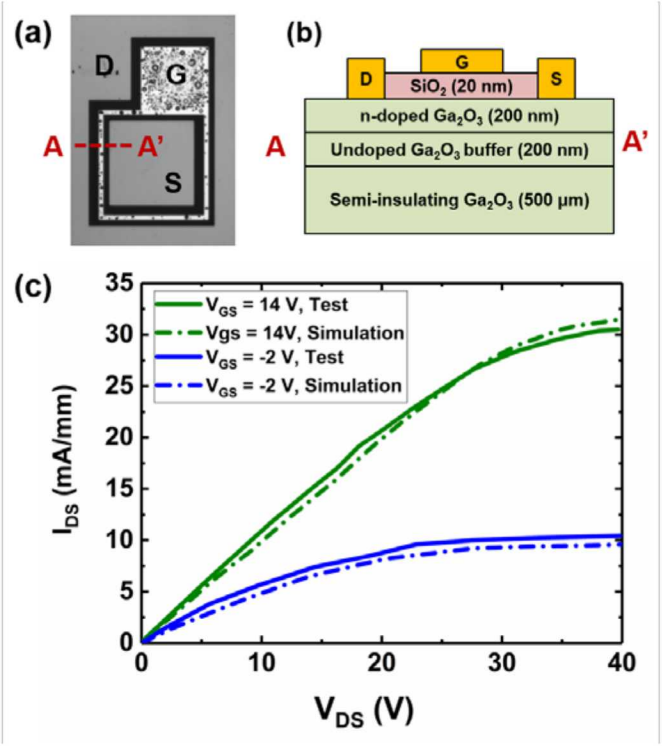

Fig. 1 (a) Top-side optical image of the device. (b) Cross-sectional schematic of the Ga_2O_3 MOSFET. For the measured device, gate to drain distance (L_{GD}) = 10 μm, gate length (L_G) = 12 μm, and gate width (W_G) = 540 μm. (c) I-V characteristics of the Ga_2O_3 MOSFET obtained using experiment and simulation.

B. *Thermoreflectance Thermal Imaging*

Temperature imaging of the source and drain electrodes was performed via visible-wavelength thermoreflectance thermal imaging [37], [38] using a Microsanj NT-210A Thermal Imaging System. This technique takes advantage of the linear change of reflectivity with temperature rise (which is represented by the thermoreflectance coefficient, C_{TR} [37]) to deduce the surface temperature of the specimen. Therefore, it provides effective means of measuring the surface temperature of metal electrodes of microelectronic devices [39]. The experimental procedure involves a lock-in modulation scheme where the device is illuminated with a pulsed light source and the reflected light intensity is measured using a charge coupled device (CCD) camera. The system is equipped with a 1626×1236 pixel charge CCD detector. A green LED with a wavelength of λ=530 nm was used as the illumination source. Using a super long working distance 50X objective with a numerical aperture of 0.45, the set up offers a diffraction limited lateral spatial resolution of ~0.59 μm.

The devices were operated with a 5 second square voltage pulse applied to the drain (V_{DS}) with a period of 200 s (i.e., 10% duty cycle) while the gate voltage (V_{GS}) was fixed at 10 V. This time period was selected to ensure that the device temperature would reach a steady-state value, while the gate bias (V_{GS}) was kept at a constant value of 10 V to ensure that the current channel was open. Measurements were taken at multiple power dissipation levels ranging from 25 mW to 200 mW (0.046 W/mm-0.373 W/mm) with a constant base plate temperature of 25°C.

C. *Infrared Thermography*

To corroborate the temperature information obtained from the thermoreflectance technique, surface temperature maps of the Ga_2O_3 MOSFETs were acquired using a QFI Infrascope mid-wavelength infrared (MWIR, λ = 2-4 μm) thermal microscope [40]–[42]. Temperature maps were recorded with a 15X objective where the resulting spatial resolution was ~2.8 μm. A pixelated emissivity correction approach was employed to increase the accuracy of the measured temperature field. Measurements were taken at multiple power dissipation levels ranging from 25 mW to 200 mW with a constant base temperature of 45°C. The gate bias (V_{GS}) was again kept constant at 10 V.

D. *Electro-thermal simulation*

A 3D electro-thermal model was built by coupling a 2D technology computer aided design (TCAD) model (using Synopsis Sentaurus, the internal heat generation profile is derived in this 2D electrical model) and a 3D finite element thermal model (using COMSOL Multiphysics, the subsequent thermal energy transport is handled in this 3D thermal model). Details of this modeling scheme can be found in [43] and [44]. Temperature dependent electronic and thermal properties including bandgap energy, electron mobility, dielectric constant, and thermal conductivity were adopted from values reported in literature [18], [45], [46]. This modeling scheme [47], [48] allows accurate deduction of the bias dependent channel temperature distribution as a result of self-heating which simplistic models fail to capture [30]. Fig. 1(c) shows the agreement between measured output characteristics and that obtained using this electro-thermal simulation scheme.

In order to reduce the computational load, the heat generation profile across the channel, obtained from the 2D TCAD model, was discretized into multiple sections as shown in Fig. 2 and then applied to the 3D thermal model.

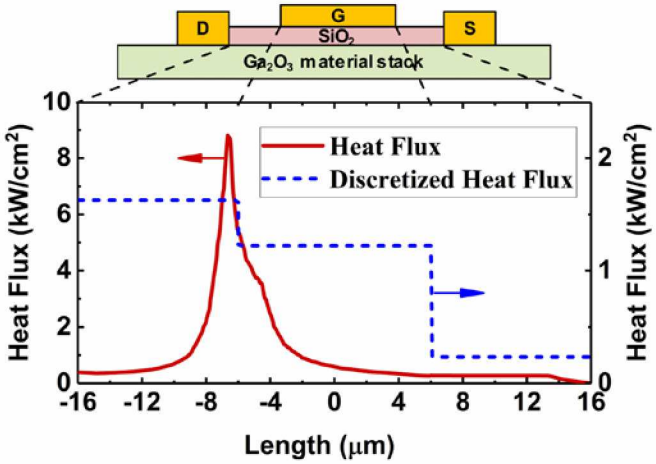

Fig. 2 Discretized heat generation profile used in the 3D thermal model. The actual heat generation profile at V_{GS} = 10 V and V_{DS} = 43.2 V is also shown.

E. *Validation of the Device Model*

The electro-thermal device model was validated using temperature maps acquired from the thermoreflectance thermal imaging and the IR thermography techniques. Reliable temperatures were measurable only for the metal electrodes since the Ga_2O_3 channel region is transparent to both visible and

infrared photon wavelengths. For available illumination sources spanning a wide range of visible wavelengths (λ = 365-780 nm), the gate metal exhibited insufficiently low C_{TR} values (C_{TR} < $5x10^{-5}$/°C) making it difficult to measure accurate temperatures. Hence, the drain and source electrode temperatures were used to validate the modeling results. Fig. 3 shows thermoreflectance imaging results using a green (λ = 530 nm) LED illumination (along with those obtained from IR thermography). The drain and source C_{TR} values were $2.0x10^{-4}$ ± 2.75 $x10^{-6}$ /°C and $1.93x10^{-4}$ ± 3.15 $x10^{-6}$/°C, respectively. Measured temperatures showed excellent agreement with those acquired using a violet (λ=405 nm) LED source.

In contrast to the thermoreflectance technique, IR thermography relies on the emissivity of the materials to be measured. While the emissivity of the metallization structures were reasonably high (> 0.2) [43], the relatively low diffraction limited spatial resolution (~3 μm) resulted in considerable lateral avergaing across the 12 μm-long gate region. This yielded underestimation of the gate surface temperature. In contrast, the drain and source region temperatures were less impacted by lateral averaging and showed excellent agreement with the thermoreflectance imaging as well as simulation results as shown in Fig. 3(a). In addition, as expected, the simulation shows that the channel peak temperature occurs at the gate region of the device. These room temperature results show a device thermal resistance of 94 K.mm/W. This is very comparable with the observation by Pomeroy et al. who found a value of 88 K.mm/W [27] even though the substrate orientations are different. It needs to be noted that the temperature rise in these two cases were very different. Due to the degradation of thermal conductivity at higher temperature, the thermal resistance will increase. However, both of these values are significantly higher than previous report of 48 mm.K/W [49] partly due to different thermal conductivity along in-plane and out of plane directions and partly due to the fact that electrical measurements measure an average temperature over the whole device area [27]

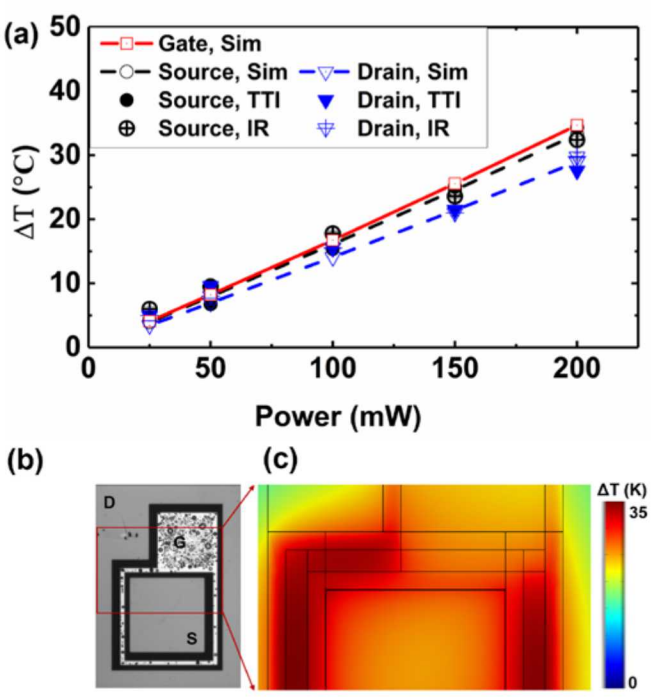

Fig. 3. (a) Electrode peak temperatures vs. dissipated power. The drain and source temperatures were measured using TTI and IR thermography. Simulation results include the source, drain and gate temperatures. All results were obtained at V_{GS} = 10 V, while V_{DS} was varied to get the required power conditions. (b) Optical image of the Ga_2O_3 MOSFET. Source and drain region temperature maps within the red boxed region were acquired via TTI and IR. (c) Electro-thermal simulation map at a power dissipating condition of P = 200 mW.

The validated model was then used to extrapolate the channel temperature rise under the targeted 10 W/mm power dissipation level. For the tested device, it was difficult to increase V_{DS} to achieve this power level due to premature breakdown. The simulated peak temperature at 10 W/mm was found to be ~1504°C. This level of extreme temperaturers are clearly not realistic as this is considerably higher than gold melting point. However, this emphasizes the fact that device-level thermal management is essential to enable high power operation of Ga_2O_3 MOSFETs. Temperature dependent properties were used from literature to ensure that the temperatures obtained were indicative of the real scenario. The reduction in thermal conductivity with increase in temperature causes non-linear increase in temperature between the power density values of 0.37 W/mm and 10 W/mm. This also results in the significantly higher thermal resistance at the power density of 10 W/mm (150.4 K.mm/W).

III. Analyzed Thermal Management Schemes

Using the validated electro-thermal device model, the effectiveness of various bottom-side and top-side passive and active cooling schemes for the Ga_2O_3 MOSFET were evaluated and compared via 3D finite element simulation. For all these cooling studies, the die/microchannel cooling module/high-κ carrier is attached to a 100 μm thick copper molybdenum (CuMo) spreader with a 50 μm thick Au-Sn solder layer, as represented by the configuration schematic for respective cases.

The spreader is mounted on a 5 mm thick copper cold plate with a commercial thermal epoxy layer. The thicknesses of various layers constituting this mounting arrangement (called package henceforth in this paper), the boundary conditions and the related thermal conductivities are adapted from references [21] and [50]. For all the comparative studies, the environment temperature (T_{Env}) is assumed to be 25°C [21]. However, an additional study was performed to evaluate the final proposed solution at T_{Env} of 85°C [51]. The schematic layout of the package, as modeled in the 3-D COMSOL FEA simulation software, is shown in Fig. 4 (a). Even though the package was modeled in detail in the 3-D simulation, for the sake of conciseness, the package is replaced with a thermal resistor ($R_{th,\ package}$) in rest of the schematic diagrams in this work (e.g. Fig. 4(b)).

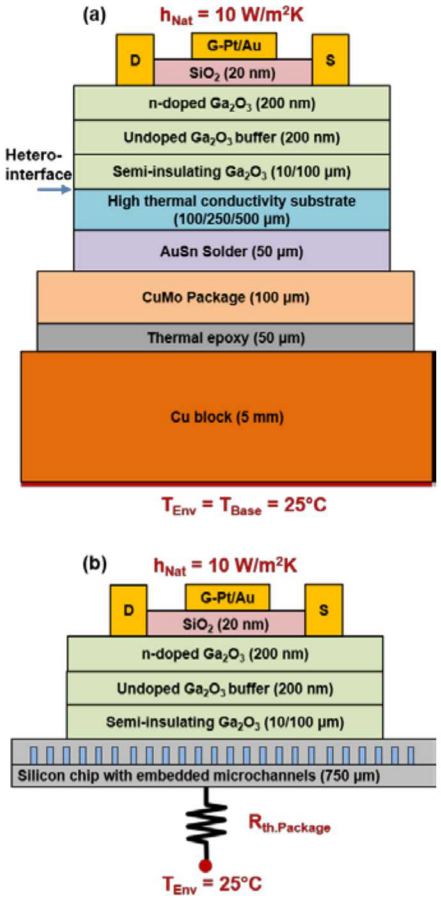

Fig. 4. (a) Schematic of the Ga_2O_3 MOSFET integrated with a high thermal conductivity substrate. The package stack-up is shown here. (b) Layout of a silicon embedded cooling module (with microchannels) attached to the Ga_2O_3 substrate. For both cases, the Ga_2O_3 substrate was thinned down to 10 or 100 µm to reduce the junction-to-cooling medium thermal resistance. The Si chip is mounted on the package which is represented by a thermal resistor in this schematic.

A. Bottom-Side Cooling Methods

First, substrate engineering (Fig. 4 (a)) as a bottom-side passive cooling solution was investigated. This approach involves thinning of the Ga_2O_3 substrate followed by integration (using an approach such as direct bonding [52]–[56]) with high thermal conductivity substrates including poly-crystalline chemical vapor deposition (CVD) grown diamond, silicon carbide (4H-SiC), and aluminum nitride (AlN). Because very few studies have reported actual Ga_2O_3/substrate integration [25], [57], a range of interfacial thermal boundary resistance (TBR) values reported in Ga_2O_3-on-diamond, GaN-on-diamond and GaN-on-SiC integration practices [21], [29], [31], [58], [59] were adopted in this study. The thermal barrier conductance (TBC) value reported by Cheng et. al. [25] was taken as the upper bound of TBR since this represents very early stage efforts. Moreover, the contribution of the post-integration Ga_2O_3 thickness to the overall thermal resistance of the material stack was studied. Two resultant Ga_2O_3 thickness values of 10 µm and 100 µm were compared. For this study and all the rest of the thermal management schemes, the bottom surface of the package was assumed to be kept at 25°C while a natural convection heat transfer coefficient of 10 W/m^{2}K was applied at the device surface exposed to the ambient, as shown in Fig. 4 (a).

Second, a bottom-side active cooling approach known as microchannel liquid cooling was investigated. In this study, microchannels were placed underneath the Ga_2O_3 substrate with varying thicknesses (10 and 100 µm). The microchannels were embedded into a silicon-based cooling module, as shown in Fig. 4(b). Physical dimensions of the embedded cooling module were adapted from those in [60]. The individual channels were 35 µm wide and 250 µm tall, with a pitch of 25 µm, which are in accordance with [21]. For the simulation, a pressure difference of 100 kPa [21], [61] across the channels was employed. Deionized (DI) water was used as the coolant. Recent literature on micro-channel heat sinks have delved into two-phase flow using water and other coolants such as HFE-7100 [61], [62]. Compared to single phase flow, two phase cooling solutions provide higher heat flux removal rate, with better axial uniformity of temperature. However, this study only focused on a single-phase cooling scheme using water.

B. Top-Side Cooling Methods

In addition to testing the effectiveness of heat extraction from the bottom-side of the material stack, it is also important to assess methods that extract heat from the top-side of the device. This is because the active region where heat generation occurs is located near the device surface. Furthermore, top-side cooling methods do not require manipulation of the cost-effective substrate material. It should be recalled that one key motivation for transitioning from GaN and SiC-based devices to the Ga_2O_3 system is the availability of low-cost melt-grown single crystalline substrates.

The third cooling approach that was tested is the use of thin diamond heat spreader as shown in Fig. 5 (a). Previously, both nanocrystalline diamond (NCD) and diamond thin films have been utilized as heat spreaders for AlGaN/GaN HEMTs. However, depending on the diamond layer thickness and grain size, the resulting thermal conductivity was shown to range between 12 W/m-K and 1370 W/m-K [32], [63]–[66]. Julian et al. [67] showed that thermal conductivity of the nanocrystalline diamond (κ_{NCD}) increases with thicker deposition. Recently, Pomeroy et al. used κ_{NCD} = 200 W/m-K for 400 nm thick diamond film [27]. In this case study, the cooling effectiveness of diamond passivation with various thermal conductivity values [63]–[65] was evaluated for the complete range obtained from literature, with a nominal value of 400 W/m-K [32].

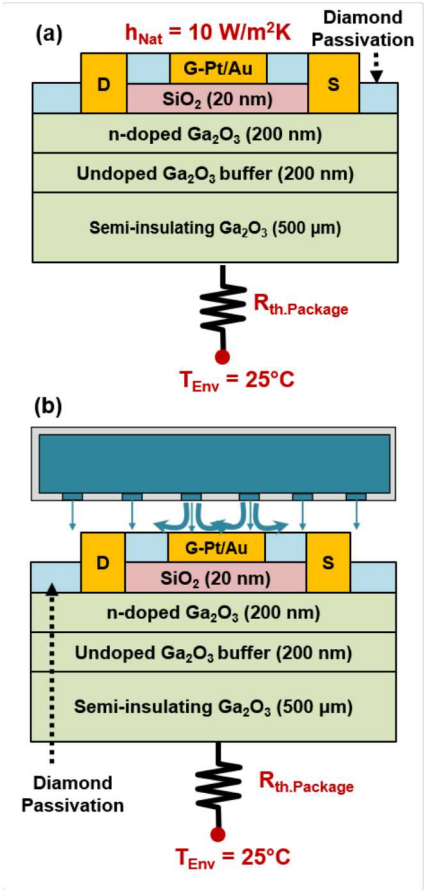

Fig. 5 (a) Schematic of Ga_2O_3 MOSFET employing NCD diamond passivation. (b) Layout of top-side air-jet impingement cooling with NCD diamond passivation.

As the fourth method, air jet impingement cooling was combined with the use of nanocrystalline diamond in order to further enhance the cooling effectiveness. The schematic is shown in Fig. 5 (b). A large pressure vessel acted as a plenum chamber with absolute pressure of 200 kPa. Six slots of 250 µm width and 100 µm height (hydraulic diameter ~67 µm) with 100 µm spacing (pitch) were used as air-jet impingement nozzles to cool the device which was at a distance of 500 µm from the nozzle exits (impingement height/ slot width = 2) [68], [69].

As a final option, flip-chip hetero-integration of the Ga_2O_3 MOSFET onto a high thermal conductivity carrier wafer made of AlN and poly-crystalline diamond was studied. Earlier studies on AlGaN/GaN HEMTs grown on sapphire substrates showed flip-chip designs would enable device operation at 2-3 times higher power conditions than standard devices for identical channel temperature conditions [42]. This is because the low thermal conductivity of the sapphire substrate hinders heat dissipation through the bottom side of the device. Compared to wire-bonded structures, the flip-chip design is also beneficial in terms of reducing the parasitic inductance [42], [70]. Because the thermal conductivity of Ga_2O_3 is less than half of that of sapphire, flip-chip design manifests itself as a viable thermal management solution for lateral Ga_2O_3 MOSFETs. Design parameters employed in the present study are similar to those in [34] that were used for thermal management of a GaAs-based heterojunction bipolar transistor (HBT). Gold pads that were mirror-images of gate, source, and drain bond pads of the Ga_2O_3 MOSFET and interconnects leading to carrier bond pads were fabricated on the carrier wafer. Indium (In) bumps were used to electrically connect the respective gold pads on the device and carrier wafer. An epoxy under-fill material was used to attach the carrier and the Ga_2O_3 MOSFET. Fig. 6 shows the schematic of a Ga_2O_3 MOSFET flip-chip integrated with a high thermal conductivity carrier wafer. The gold bond pads and interconnects on the carrier were 5 µm thick, whereas the thickness of the Indium bumps was 10 µm. The carrier was mounted on the package described earlier in Fig. 4(a).

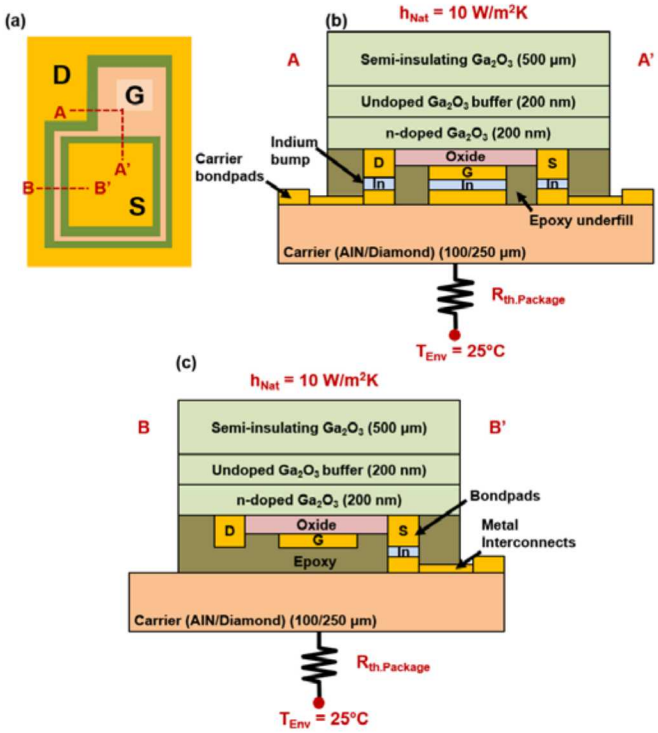

Fig. 6. Flip-chip hetero-integration of a Ga_2O_3 MOSFET onto a high thermal conductivity carrier wafer. (a) Device schematic. (b) Cross-sectional view showing electrical connection between the device and carrier wafer. (c) BB' cross-section. 3-D simulation was performed to evaluate the improvement offered by this design.

Heat dissipation from the device active region to the carrier can be further improved by reducing the thermal resistance associated with the epoxy (κ = 1.1 W/m-K [34]) under-fill material. This can be obtained by using high-κ composite epoxy and also by introducing the previously discussed NCD passivation on the device surface. Both of these cases were studied in the present work. A schematic of the device stack that utilizes the NCD passivation to augment heat dissipation from the Ga_2O_3 channel is shown in Fig. 7.

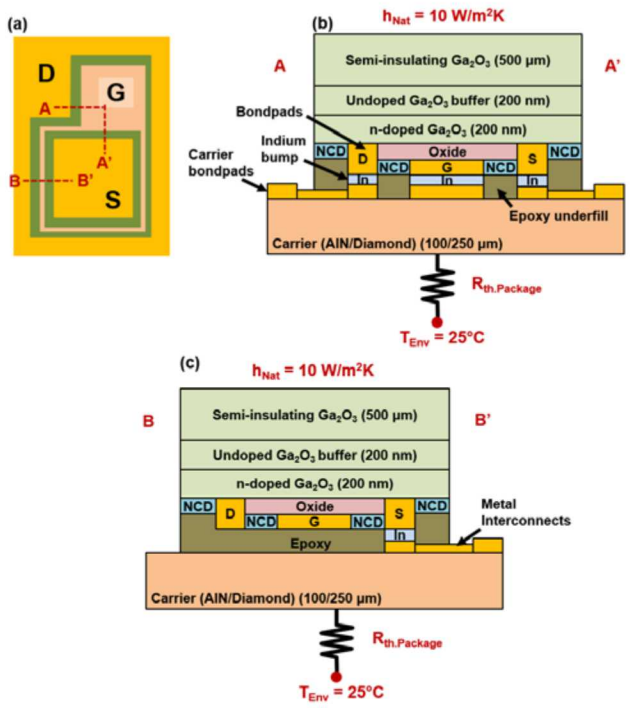

Fig. 7. Flip-chip hetero-integration of a Ga_2O_3 MOSFET employing nanocrystalline diamond (NCD) passivation. (a) Device schematic. (b) Cross-sectional view showing electrical connection between device and the carrier wafer. (c) The BB' cross-section.

Additional reduction in the device thermal resistance can be achieved by inserting thermal heat sinks (i.e., thermal bumps) between the device surface and the carrier wafer. A thin silicon nitride layer can be used for electrical insulation across the heat transfer path as shown in Fig. 8 (c).

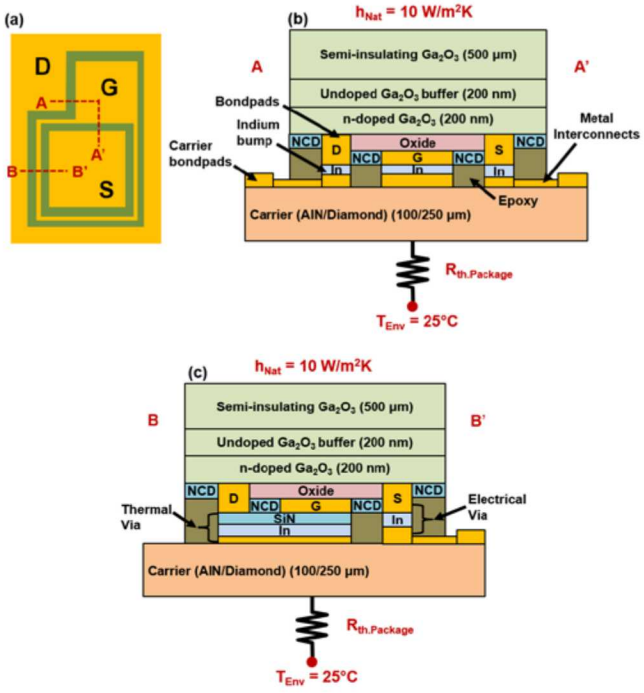

Fig. 8. Flip-chip hetero-integration of a Ga_2O_3 MOSFET combined with the use of NCD passivation and thermal bumps. (a) Device schematic. (b) AA' cross-sectional view. (c) The BB' cross-section showing heat sinks (i.e., thermal bumps) between the device channel region and the carrier wafer.

IV. Results and Discussion

A. Substrate Integration

High thermal conductivity substrates (with a thickness of 100 µm) including AlN, SiC, and CVD diamond were integrated with Ga_2O_3 MOSFETs that underwent native substrate thinning down to 100 µm and 10 µm to study the configurations shown in Fig. 4. The thinnest case was chosen to be 10 µm as opposed to ~1 µm for previous efforts on GaN-on-diamond integration. The base material stack for AlGaN/GaN HEMTs includes a ~1 µm thick GaN layer which is hetero-epitaxially grown on a non-native substrate. Selective etching/removal of the non-native substrate (typically SiC) leaves behind a ~1 µm thick GaN buffer that is integrated with the diamond substrate via either bonding [52]–[56] or direct growth [71]–[73]. Since Ga_2O_3 devices are homoepitaxially grown, the option of selective etching (leaving behind the n-doped epilayer) is irrelevant. Instead, a substrate thinning process is required that typically involves mechanical lapping followed by chemical mechanical polishing (CMP). This renders thinning beyond 10 µm very challenging.

For the case of thinning down the Ga_2O_3 substrate to 100 µm, even integrating with a diamond substrate results in a device channel temperature rise exceeding 1000°C at 10 W/mm. This is because of the low thermal conductivity of Ga_2O_3 combined with the large distance between the diamond substrate and the near-surface device active region (current channel) where heat generation occurs. In contrast, when the Ga_2O_3 substrate was thinned down to 10 µm, integration with a diamond substrate reduces the junction to package thermal resistance by a factor of six. Simulation results are shown in Fig. 9 (a).

Fig. 9 (b) shows the impact of the interfacial thermal boundary resistance (TBR) between the Ga_2O_3 layer and the high thermal conductivity substrates. Three TBR values from the Ga_2O_3-on-diamond [24] and GaN-on-diamond literature were tested. These TBR values are representative of early-stage integration efforts (60 m^2K/GW, [25], [74]–[79]), common values resulting from established bonding and growth methods (12 m^2K/GW [16], [31], [75]), and latest state-of-the-art results (6.5 m^2K/GW [58]). It was found that it is not necessary to improve the TBR beyond 12 m^2K/GW, which is in contrast to the case of AlGaN/GaN HEMTs [31]. This is mainly because the thermal resistance associated with the Ga_2O_3 layer (from the lower thermal conductivity and larger layer thickness) is considerably larger than that for a 1 µm GaN layer in AlGaN/GaN HEMTs. The largest TBR value of 60 m^2K/GW was found to impair the cooling performance of the integrated devices. This effect is most pronounced when employing a diamond substrate since the fractional contribution of the TBR to the overall thermal resistance of the material stack is increased compared to other cases.

For a constant TBR of 12 m^2K/GW, the effect of the foreign substrate thickness was studied in Fig. 9 (c). The thicker substrate with order of magnitude higher thermal conductivity as compared to the native Ga_2O_3 substrate acts as a heat spreader in these scenarios. It is observed that for higher

thermal conductivity substrates, the substrate thickness has a lower impact on the device peak temperature as compared to relatively lower thermal conductivity substrates. For example, for the relatively less thermally conductive AlN, the 100 µm substrate showed ~10% higher junction temperature as compared to that for a 500 µm thick substrate. For higher thermal conductivity diamond, the impact is ~5%.

Fig. 9 (d) is a thermal resistance waterfall chart that shows the relative impact of various design parameters on the device thermal resistance. The "baseline" case (i.e. a Ga_2O_3 MOSFET based on homoepitaxy) results in a junction-to-package thermal resistance ($R_{Th\,j\text{-}p}$, as shown in Fig. 9(d)) of 150.4 mm.K/W. For an unoptimized Ga_2O_3-on-AlN device (with a Ga_2O_3 substrate thickness of 100 µm, a carrier wafer thickness of 500 µm, and a Ga_2O_3/AlN TBR of 60 m^2K/GW), a reduction in the junction-to-package thermal resistance ($R_{Th,j\text{-}p}$) of 22% was achieved, indicating the benefit of improving the substrate thermal conductivity. On the other hand, reducing the foreign substrate thickness from 500 µm to 100 µm yielded a mere 0.5% improvement in the $R_{Th,j\text{-}p}$. Fig. 9 (d) shows that reducing the Ga_2O_3 thickness from 100 µm to 10 µm dramatically improves $R_{Th,j\text{-}p}$ (73% reduction). This manifests that pre-integration Ga_2O_3 substrate thinning is the key design parameter for the substrate integration method. Employing a higher thermal conductivity diamond substrate instead of AlN further reduces $R_{Th,j\text{-}p}$ by 21%. Improving the TBR from 60 m^2K/GW to 12 m^2K/GW reduces the $R_{Th,j\text{-}p}$ by 7%. However, consistent with results shown in Fig. 9 (c), reducing the TBR from 12 m^2K/GW to 6.5 m^2K/GW marginally improves $R_{Th,j\text{-}p}$ (< 1%).

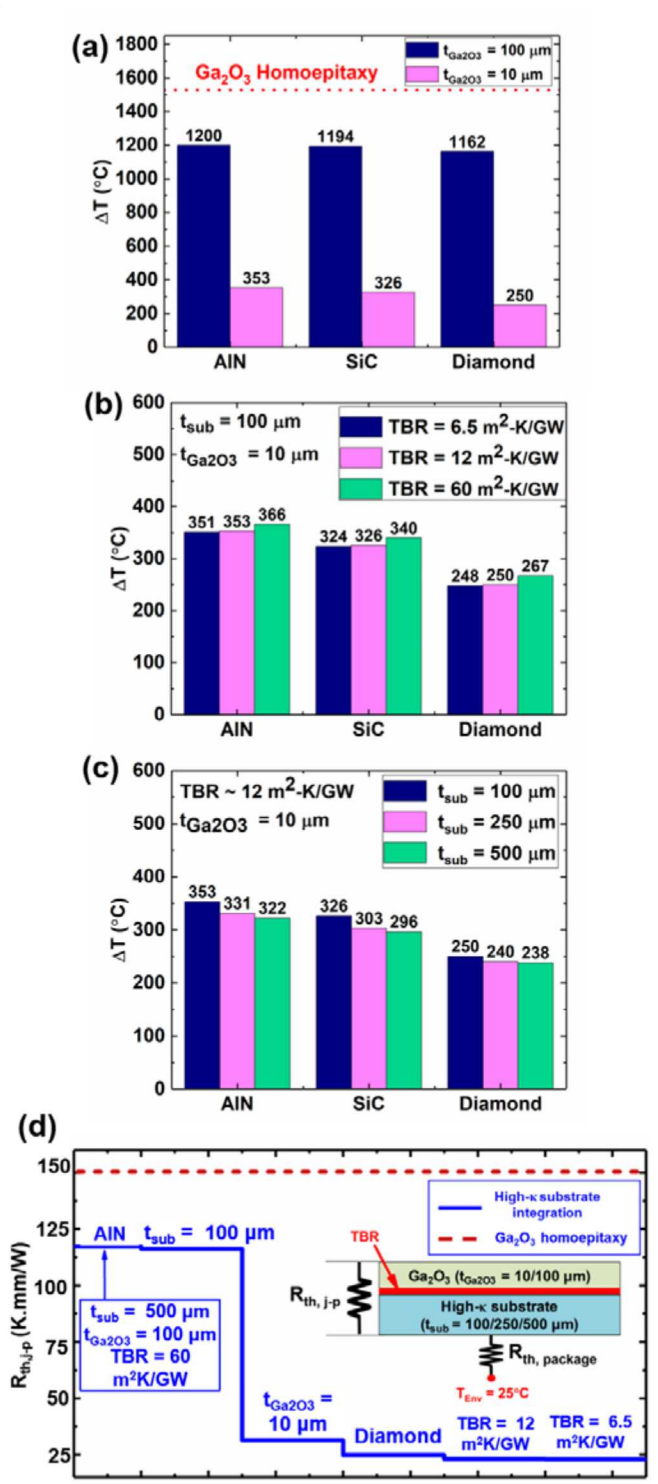

Fig. 9. (a) Reduction in the device channel temperature by engineering the substrate. Thinning down the native Ga_2O_3 substrate is the key to realizing superior thermal performance. (b) The effect of thermal boundary resistance (TBR) on the junction temperature rise (at 10 W/mm) for a Ga_2O_3 MOSFET (with a Ga_2O_3 thickness of 10 µm) integrated with 100 µm thick high thermal conductivity substrates including AlN, 4H-SiC, and diamond. (c) The effect of reducing the foreign substrate thickness at a fixed TBR of 12 m^2K/GW. (d) The thermal resistance waterfall diagram for high-κ substrate hetero-integration indicates that reducing the Ga_2O_3 thickness from 100 µm to 10 µm results in remarkable improvement in the device thermal performance.

B. Microchannel Cooling

Simulation results for bottom-side active thermal management using a Si-based microchannel cooling module also revealed the importance of locating the heat sinking medium as close as possible to the device active region. The cooling effectiveness of this method for Ga_2O_3 MOSFETs with the native substrate thicknesses of 10 and 100 µm is shown in Fig. 10. For both cases, the device peak temperature exceeds the stipulated limit (T_j < 200°C). It should be noted that the microchannel configuration, choice of coolant, and flow rates were not optimized. Therefore, further improvement in the cooling performance is possible. However, similar to the case of employing substrate integration, this method invalidates the key advantage of the Ga_2O_3 materials system—the availability of low-cost bulk substrates. For a comparative purpose, results in Fig. 10 also show the junction temperature rise when microchannels are directly grooved through the Ga_2O_3 substrate, 10 and 100 µm below the device active region. This impractical approach (in terms of difficulty in fabrication) does not necessarily perform better than the case using a Si embedded cooling module for the assumed flow geometry/conditions. The relatively high thermal conductivity of Si material helps the spreading of the heat away from the active region.

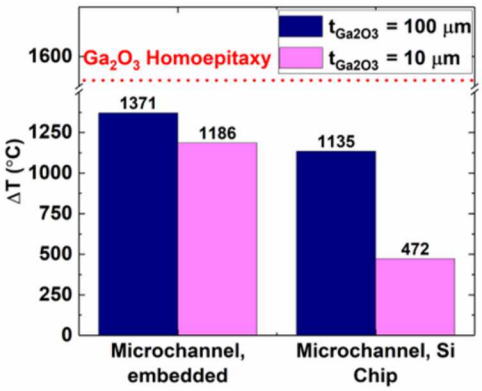

Fig. 10. Temperature rise for microchannel cooled devices. Two cases where microchannels were directly formed in the Ga_2O_3 substrate and enclosed in a Si-based embedded cooling module were studied. Thinning down the low thermal conductivity Ga_2O_3 substrate was found to be critical in order to reduce the device temperature.

C. Nanocrystalline diamond (NCD) passivation

Nanocrystalline diamond (NCD) passivation was found to offer insufficient cooling performance required to meet the targeted junction temperature (T_j < 200°C) under 10 W/mm power dissipation. The benefit obtained using the NCD with κ = 400 W/m-K is found to be only ~8%. This is significantly lower than the 18% reduction obtained by Pomeroy et. Al. [27]. The difference can be attributed to different crystal orientation, as well as the difference in the FET geometry. For the present geometry, even for a NCD passivation with thermal conductivity of 1370 W/m-K (highest value reported for NCD films [63], [64]), the device peak temperature would exceed 1000°C at 10 W/mm as shown in Fig. 11. Despite the fact that NCD layer serves as an effective top-side heat spreader, the natural convection boundary condition acts as a bottleneck for subsequent heat dissipation to the surrounding air. It should be noted that the simulated diamond passivation thickness was set at ~500 nm in accordance with the "gate after diamond" approach described in [63]. This approach enables the use of higher diamond growth temperature without affecting the thermally sensitive Schottky gate. For AlGaN/GaN HEMTs, growing the diamond passivation beyond this thickness was shown to be challenging due to the large mismatch between key crystalline properties of the AlGaN barrier and diamond, including lattice constants and coefficients of thermal expansion. Also, a thicker diamond film may result in undesired wafer bowing, cracking, delamination, and degrading material quality [80]–[82]. Although they have not been pursued in this work, approaches using NCD to shunt to a thermal via may be a viable option for top-side thermal management.

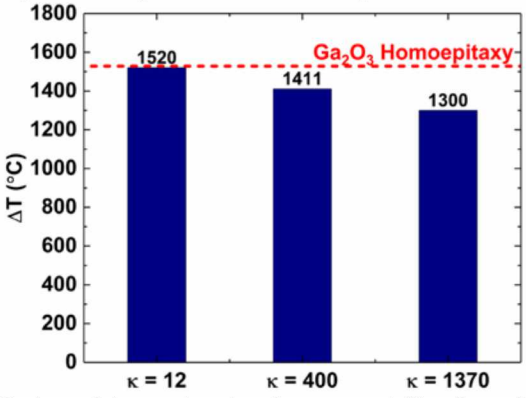

Fig. 11. Device peak temperature rise when nanocrystalline diamond (NCD) was employed as a top-side heat spreading passivation layer. This study was performed on a homoepitaxial Ga_2O_3 MOSFET with a substrate thickness of 500 µm.

D. Air-Jet Impingement Cooling, Combined with Diamond Passivation

As shown in Fig. 12, air-jet impingement cooling alone is not a viable solution. The junction temperature exceeds 1000°C at 10 W/mm, despite applying air-jet impingement cooling on the Ga_2O_3 MOSFET, as described in Section III and as shown in Fig. 5(b). The peak air jet velocity as it ejects from the slots was found to be 250 m/s, while the velocity prior to impingement was found to be 75 m/s. The design parameters were closely referenced from successful designs of air-cooled multi-chip modules, as well as studies done on uniform heat flux over hot plates [68], [69].

However, once combined with the diamond passivation scheme (κ_{NCD}=1370 W/m-K), the junction temperature was lowered to 318°C. Since this is an active cooling technique, by optimizing the air flow rate, jet velocity, and impingement height, it is possible to achieve higher heat transfer coefficients and lower peak temperatures. However, active cooling solutions involve the incorporation of ancillary equipment into the system. This impairs the size, weight, and power (SWaP) benefits, along with cost. This gives a motivation to explore the potential of top-side passive cooling methods that may offer thermal performance of Ga_2O_3 MOSFETs comparable to that for commercial GaN-on-Si and/or GaN-on-SiC technologies.

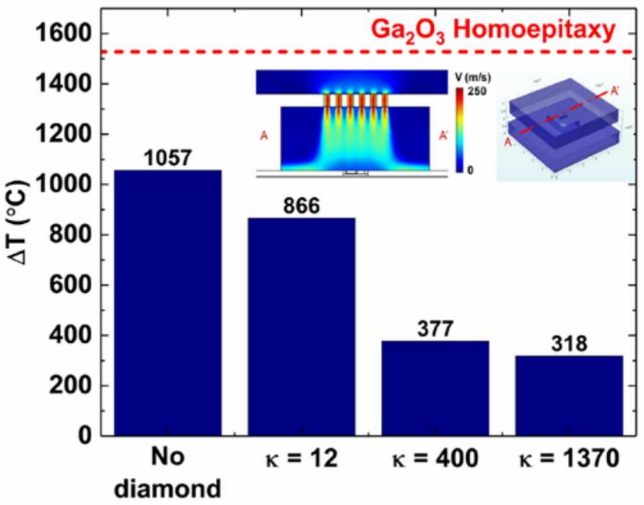

Fig. 12. Reduction of the device junction temperature rise by the combined use of air-jet impingement cooling and diamond passivation. This study was performed on a homoepitaxial device with a 500 µm thick substrate.

E. Flip-Chip Hetero-Integration

Employing the flip-chip configuration enables locating the heat spreader, i.e., a high thermal conductivity carrier wafer, in close proximity to the device active region without altering the Ga_2O_3 substrate. In the flip-chip configuration, according to Fig. 6, most of the heat generated from the device channel is routed through the device-side bond pads, then the indium bumps, interconnects, and finally extracted throughout the volume of the carrier wafer. Fig. 13 (a) shows that by replacing the indium bumps (which electrically and physically connect the device chip and carrier bond pads) with gold (Au) bumps, one can reduce the junction temperature by ~7%. Also, using a thinner carrier (100 µm thick as compared to 250 µm) marginally improves the cooling performance. Despite gold bumps being used together with a diamond carrier, the device junction temperature was found to exceed 400°C, well-beyond the stipulated temperature limit of 200°C. The equivalent thermal circuit of this design shows that the extremely low thermal conductivity of the epoxy (κ = 1.1 W/m-K) [34] used to bond the device and carrier chip acts as the thermal bottleneck. Hexagonal boron nitride (h-BN) infused composite epoxy that provides a thermal conductivity as high as 14 W/m-K [83]–[85] can be used to minimize this thermal resistance and thereby reduce the device junction temperature. Fig. 13 (b) shows that employing a h-BN/epoxy composite with a thermal conductivity of 9 W/m-K and a lower cost AlN carrier is capable of lowering the junction temperature rise below 200°C at 10 W/mm power dissipation. However, this still does not meet the criterion of $T_j < 200$°C (T_j is the sum of the channel temperature rise and the ambient temperature). Using an h-BN/epoxy composite offering a thermal conductivity of 14 W/m-K together with an AlN carrier wafer (this design is henceforth referred to as FC1) or a diamond carrier wafer (henceforth referred to as FC2) reduces the junction temperature rise to 191°C and 151°C respectively, at the same power level, thus meeting the aforementioned temperature requirement.

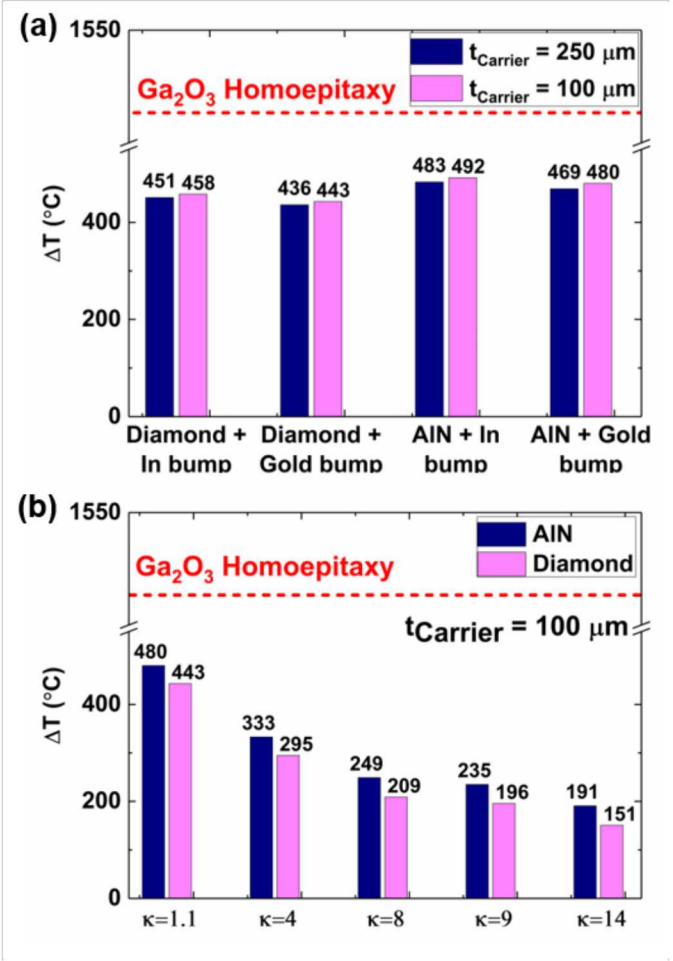

Fig. 13. (a). Device junction temperature rise at 10 W/mm as a function of the carrier wafer material (AlN vs. diamond), carrier thickness (100 µm vs. 250 µm), and electrical bump material (In vs. Au). (b) The effect of the thermal conductivity of the epoxy under-fill material to device temperature rise.

The metal bumps help in driving the heat generated in the device active region out through the contacts, but the dominant thermal resistance is still the contribution from the Ga_2O_3 as the heat flows laterally through the semiconductor to the location of the device-side bond pads. Incorporating high thermal conductivity NCD passivation opens another heat removal pathway from the device active region to the contacts which bypasses the Ga_2O_3 and epoxy regions. The schematic of this design is shown in Fig. 7. This configuration can be beneficial for RF devices because of the small gate dimensions and the minimized addition of electrical parasitics caused by adding metal structures such as thermal bumps (which will be discussed henceforth in the thermal point of view). In addition to employing NCD passivation, introducing heat sinks (i.e., thermal bumps) between the device active region and the carrier wafer as shown in Fig. 8 should result in further enhancement of the heat removal effectiveness of the flip-chip hetero-integration design. The metal thermal bumps will add undesired capacitance, but not to an extent to degrade the performance of power devices because of the electrically insulating nature of the carrier wafer. Simulation results are shown in Fig. 14 which provides a summary of the incremental improvements in $R_{th,j\text{-}p}$ accrued by incorporating the various design modifications discussed in Figs. 6-8. The chart demonstrates that upon hetero-

integration with an AlN carrier of thickness 250 µm, $R_{Th,\ j\text{-}p}$ reduces from 150.4 mm·K/W to 46 mm·K/W (70% reduction as compared to a baseline homoepitaxial Ga_2O_3 device). However, reducing the carrier thickness from 250 µm to 100 µm and replacing the AlN carrier to diamond results in merely a 2% improvement in $R_{Th,j\text{-}p}$. On the other hand, when the thermal conductivity of the epoxy underfill increased by using a h-BN/epoxy composite (κ=14 W/m-K), an additional 68% reduction in $R_{Th,j\text{-}p}$ was obtained, which brings the $R_{Th,j\text{-}p}$ of the Ga_2O_3 MOSFET down to the level of a commercial GaN-on-Si HEMT. It was observed that when the indium bump was replaced with gold, ~3% improvement in $R_{Th,j\text{-}p}$ could be obtained. Next step in the design optimization was to incorporate the use of NCD passivation as discussed above. For κ_{NCD}=400 W/m-K, a further 37% reduction in the MOSFET thermal resistance was obtained, bringing it down to ~8.9 mm.K/W, which is significantly below that for a GaN-on-Si HEMT ($R_{th,j\text{-}p}$~13 mm.K/W). This also means that the junction temperature rise is only ~89°C under 10 W/mm power dissipation. When thermal bumps as described in Fig. 8 are used in conjunction with the NCD passivation (henceforth referred to as FC3), the thermal resistance further reduces to a value of 6.5 mm.K/W. Using the maximum thermal conductivity reported for NCD films (κ_{NCD}=1370 W/m-K), an $R_{Th,j\text{-}p}$ of 4.4 mm.K/W can be accomplished. This is lower than that for a GaN-on-SiC HEMT device with a similar device layout.

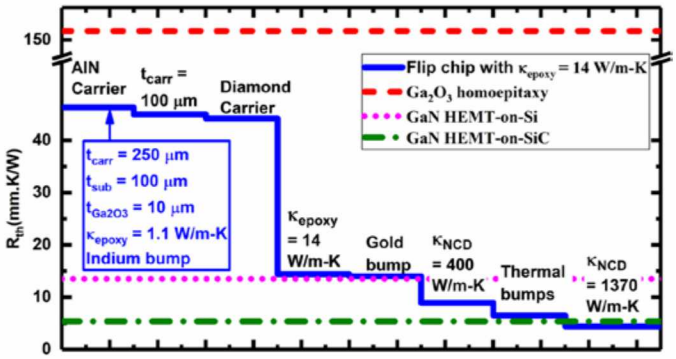

Fig. 14. Thermal resistance waterfall chart for flip-chip hetero-integration design schemes shown in Fig. 6-8. Each step corresponds to a single design modification. The chart shows the incremental improvement accrued by the carrier thickness (t_{carr})/material, along with the remarkable improvement in the thermal performance offered by a high thermal conductivity composite epoxy used to bond the device die and carrier wafer. By using thermal bumps in accordance with Fig. 8 in conjunction with NCD passivation (κ_{NCD}=1370 W/m-K), theoretically, a device thermal resistance lower than that for a GaN-on-SiC HEMT can be achieved.

F. Summary

As Ga_2O_3 devices target to overcome the power handling capability limits of GaN-based devices (i.e., AlGaN/GaN HEMTs), the thermal performance of the two device technologies were compared. A commercial GaN-on-Si HEMT material stack was used as a benchmark. Previous research efforts on device-level thermal management of AlGaN/GaN HEMTs focused on the use of high thermal conductivity diamond substrates, replacing lower conductivity Si and SiC substrates [86], and the introduction of liquid cooling in the near-junction region by removal of the low conductivity epitaxial and transition layers at the interface of the GaN buffer and the substrate [21].

The key to maximizing the device-level thermal performance of Ga_2O_3 devices is to minimize the thermal resistance between the device active region (where the heat is generated) and the heat sinking medium or the region where the low temperature thermal boundary condition applies (for most cases, the device package temperature). The thermal resistance of Ga_2O_3 MOSFETs flip-chip integrated with a commercial polycrystalline AlN carrier using a high thermal conductivity epoxy underfill material (~14 mm.K/W) was found to be comparable with that for a GaN-on-Si HEMT employing an identical device layout (13 mm.K/W), as shown in Fig. 15. By introducing thermal bumps (between the device surface and the carrier wafer) and employing NCD passivation (κ = 400 W/m-K), a device thermal resistance comparable with that for a GaN-on-SiC HEMTs was achieved. Although the thermal performance accompanied by active cooling solutions were shown to be inferior to the proposed top-side passive cooling method (i.e., flip-chip hetero-integration), it should be noted that the effectiveness of active cooling can be improved by optimizing various design parameters. However, active cooling solutions entail peripherals that negatively impact the system SWaP.

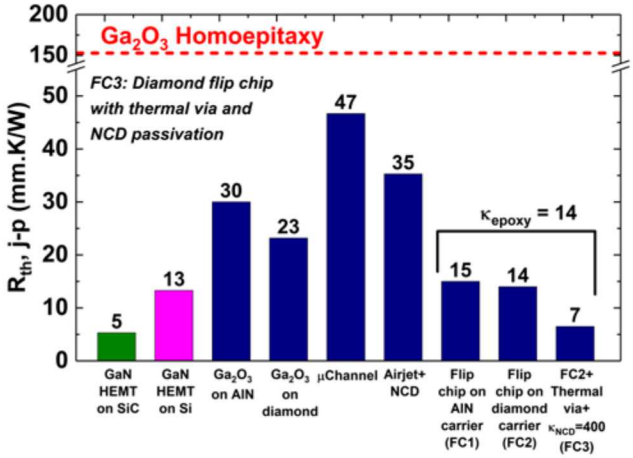

Fig. 15. Overall comparison of the device thermal resistance associated with the thermal management schemes studied in this work as well as the benchmark GaN-on-Si HEMT technology. Ga_2O_3 MOSFETs employing flip-chip hetero-integration using commercially available base materials makes it possible to achieve a junction-to-package device thermal resistance value comparable with that for a GaN-on-Si HEMT. When the flip-chip design is augmented with NCD passivation and thermal heat sinks, the device thermal resistance can reach that of a GaN-on-SiC HEMT.

Findings of this work together with economic and manufacturing considerations suggest that a configuration that employs flip-chip hetero-integration at the device-level in conjunction with package/module-level active cooling methods such as double sided cooling and utilization of AlSiC metal matrix composite (MMC) materials [87]–[91] could be the most practical and viable approach to resolve thermal challenges associated with the emerging ultra-high power Ga_2O_3 lateral device technology.

In the end, the transient thermal response of the candidate thermal solutions and the benchmark GaN-on-Si technology was compared (excluding the package). Results are compared

in Fig. 16. For a Ga_2O_3 MOSFET based on homoepitaxy (i.e., no thermal solution employed), not only the steady-state temperature rise but also the transient thermal dynamics (reflected by a thermal time constant [43] which turns out to be on the order of ~1 ms) are unacceptable for high voltage/current switching applications. Diamond substrate integration improves the thermal time constant by two orders of magnitude (14 μs) which is the lowest among all of the bottom-side thermal management solutions discussed in this work. Flip-chip hetero-integration leads to a time constant of 32 μs, which is larger than that for the case of diamond substrate integration. However, this value is lower than that for a GaN-on-Si HEMT employing an identical device layout (56 μs). This suggests that flip-chip hetero-integration of Ga_2O_3 MOSFETs with commercial polycrystalline AlN carrier wafers using a high thermal conductivity under-fill material can serve as a cost-effective thermal solution for Ga_2O_3 MOSFETs while still offering acceptable steady-state and transient device thermal characteristics. Furthermore, when a diamond carrier, NCD passivation ($\kappa = 400$ W/m-K), and thermal bumps are employed in the flip-chip hetero-integration scheme, a thermal time constant of ~8 μs is achieved, which is the best value among all of the thermal management schemes discussed in this work. This design is referred as FC3 in Fig. 16 which also shows that the FC3 configuration results in a shorter thermal time constant than that of a GaN-on-SiC HEMT (22 μs).

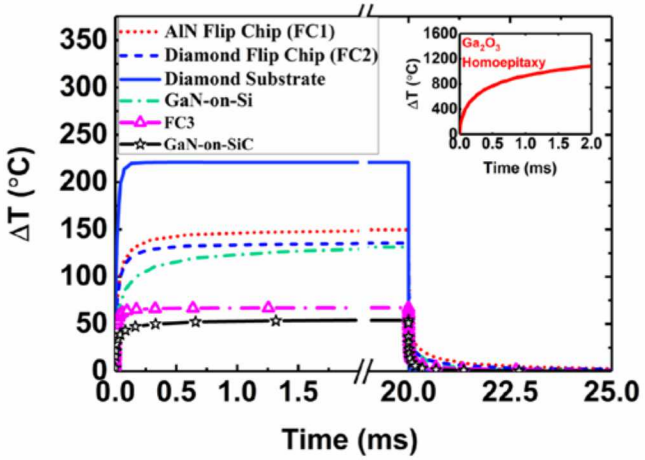

Fig. 16. Comparison of the thermal dynamics of a Ga_2O_3/diamond substrate-integrated MOSFET, a Ga_2O_3 MOSFET flip-chip integrated onto an AlN carrier wafer, a Ga_2O_3 MOSFET flip-chip integrated onto a diamond carrier wafer (FC2), a configuration where FC2 is augmented with thermal bumps and NCD passivation (FC3), a GaN-on-Si HEMT, and a GaN-on-SiC HEMT.

V. Conclusion

Various device-level cooling schemes to manage the self-heating in Ga_2O_3 MOSFETs were compared with the objective of achieving a device junction temperature below 200°C under a targeted power dissipation level of 10 W/mm. Some of the proposed solutions are more expensive or more difficult to implement. For example, the air-jet cooling requires ancillary equipment that increase size and expenses associated with the thermal management scheme. Also, etching embedded microchannels in Ga_2O_3 substrate might prove to be challenging. However, substrate integration and flip chip integration are techniques that have been already demonstrated in GaN and Ga_2O_3 technologies. Additional components are not required while the running cost is minimal. Considering thermal performance improvement as well as these economic and manufacturing considerations, the combined use of flip-chip hetero-integration at the device-level and existing package/module-level active cooling will serve as a viable and practical solution to the resolution of thermal challenges associated with high power Ga_2O_3 lateral device technologies. Flip-chip hetero-integration onto a thermally conductive carrier using a high thermal conductivity composite epoxy resin was found to yield a junction-to-package thermal resistance value comparable to that for GaN-on-Si HEMTs. Furthermore, this flip-chip design was shown to provide a superior thermal transient response to GaN-on-Si devices by roughly 40%. By introducing thermal bumps and NCD passivation, the flip chip design can reduce the junction temperature below the stipulated target junction temperature of 200°C while operating at a power density of ~13.3 W/mm and a copper cold plate temperature condition of 85°C (that represents the system environment temperature into which the Ga_2O_3 device is integrated [51]). This exceeds the targeted power density of 10 W/mm for Ga_2O_3 devices by a 33%, indicating the feasibility and potential of the materials system in spite of the existing thermal challenges.

Acknowledgment

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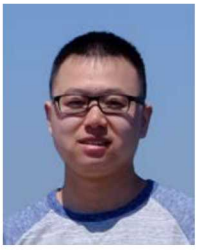

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List of Figures

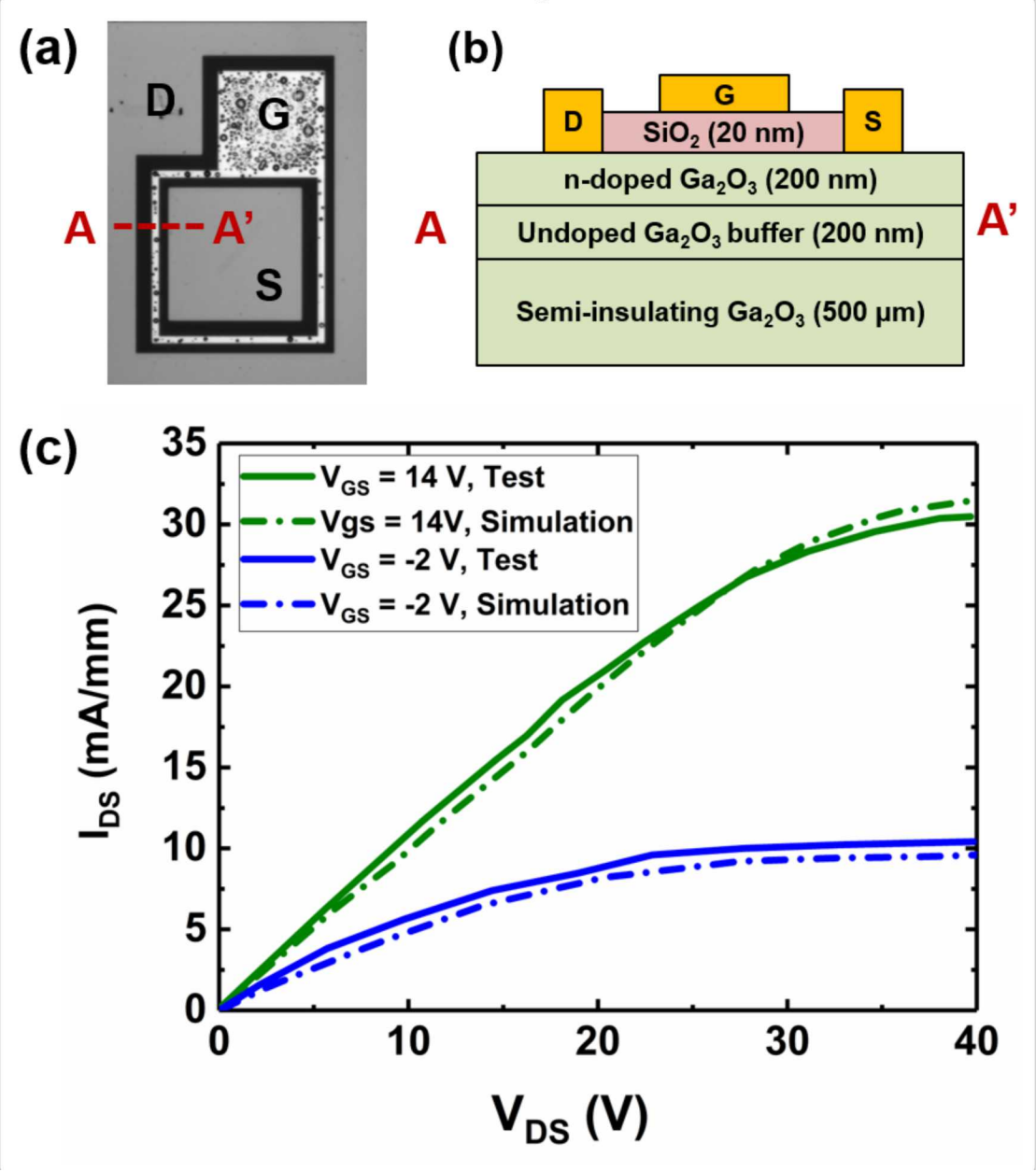

Fig. 1 (a) Top-side optical image of the device. (b) Cross-sectional schematic of the Ga_2O_3 MOSFET. For the measured device, gate to drain distance (L_{GD}) = 10 μm, gate length (L_G) = 12 μm, gate width (W_G) = 540 μm. (c) I-V characteristics of the Ga_2O_3 MOSFET obtained using experiment and simulation.

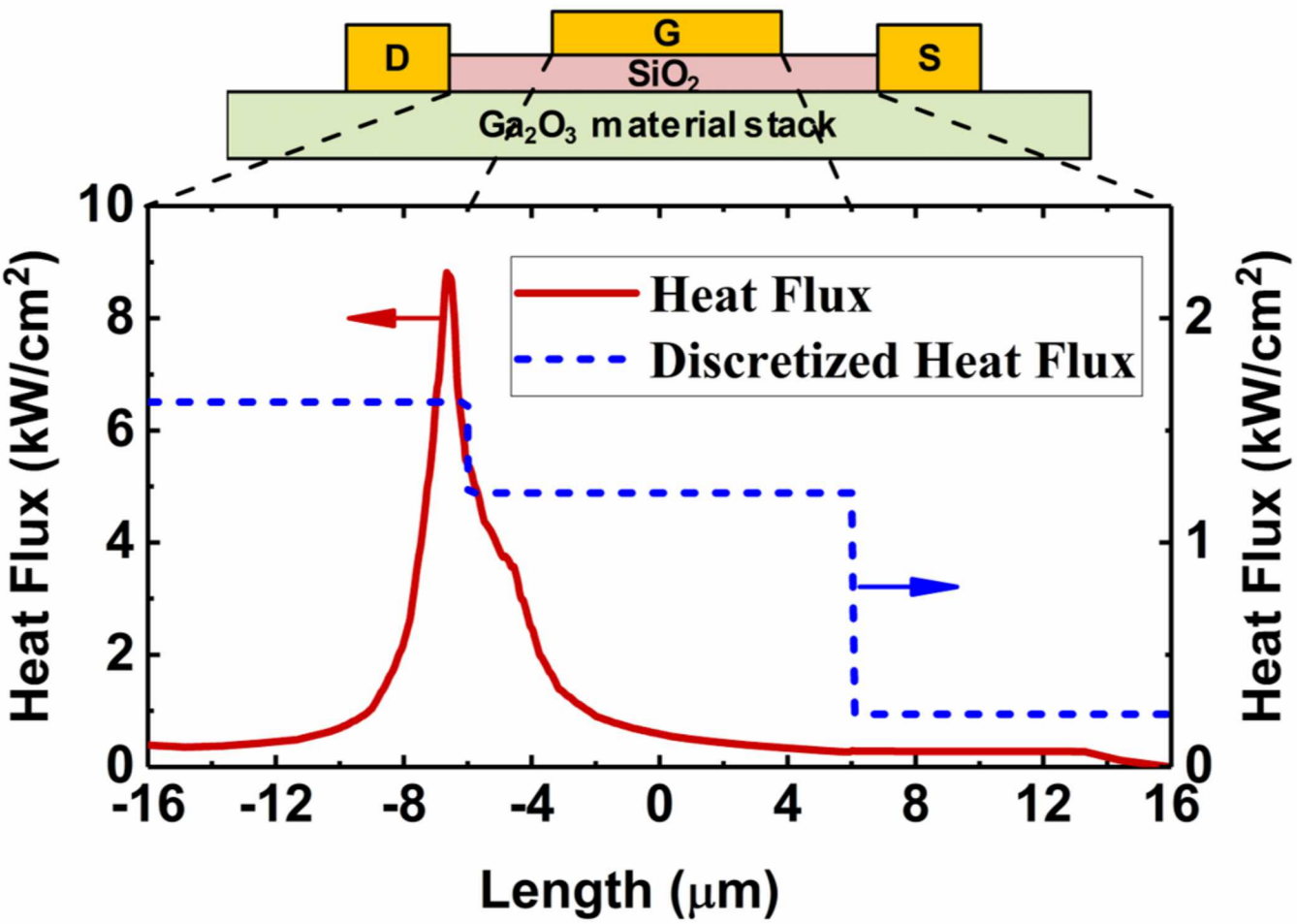

Fig. 2 Discretized heat generation profile used in the 3D thermal model. The actual heat generation profile at V_{GS} = 10 V and V_{DS} = 43.2 V is also shown.

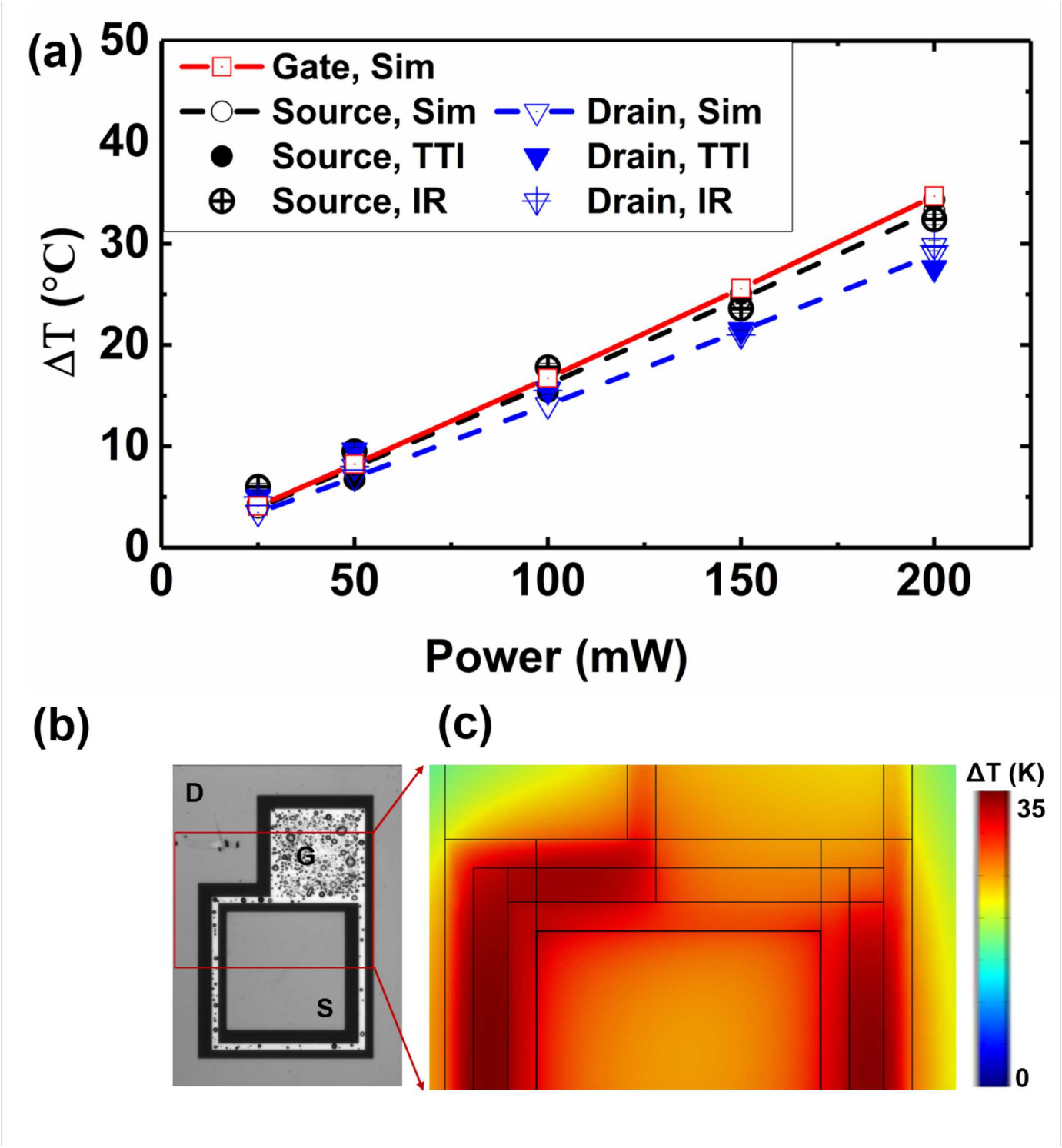

Fig. 3. (a) Electrode peak temperatures vs. dissipated power. The drain and source temperatures were measured using thermoreflectance thermal imaging (TTI) and IR thermography. Simulation results include the source, drain as well as gate temperatures. All results were obtained at V_{GS} = 10 V, while V_{DS} was varied to get the required power conditions. (b) Optical image of the Ga_2O_3 MOSFET. Source and drain region temperature maps within the red boxed region were acquired via TTI and IR. (c) Electro-thermal simulation map at a power dissipating condition of P = 200 mW.

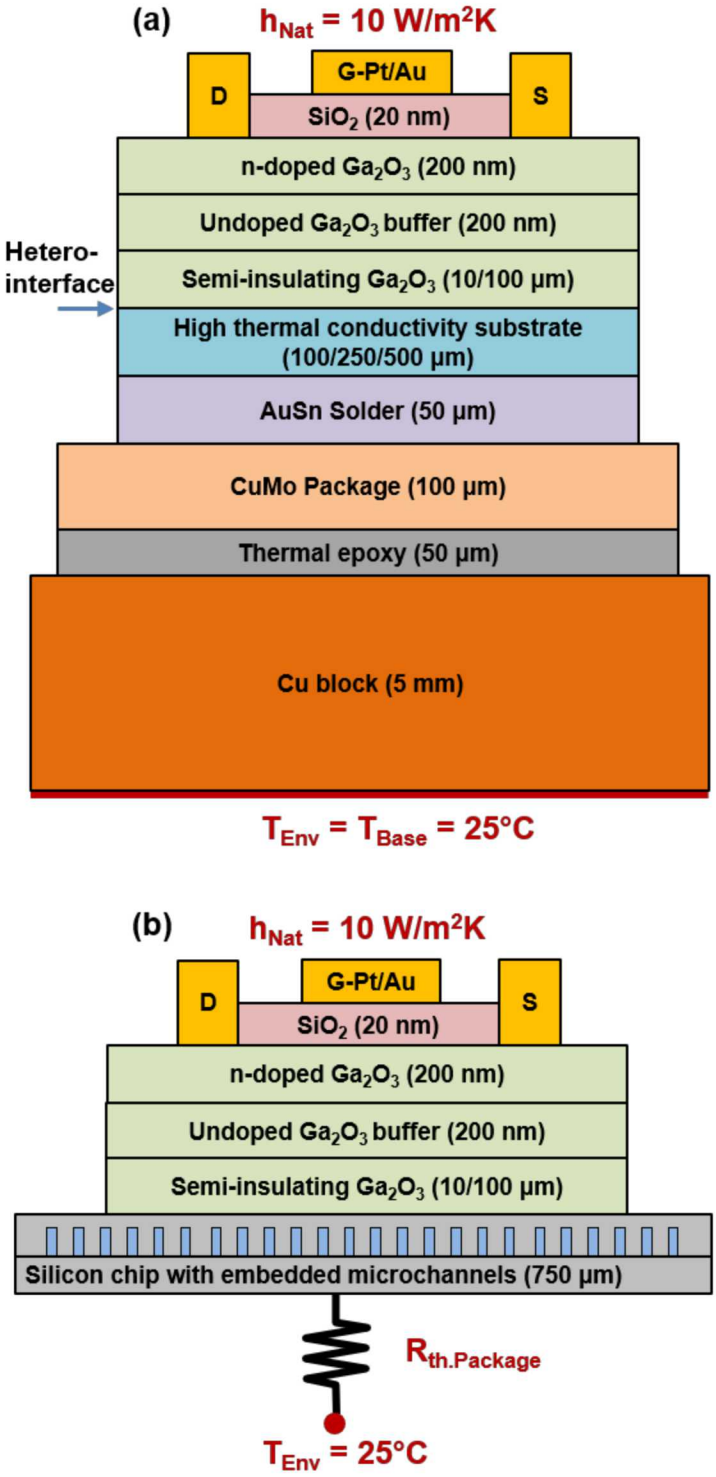

Fig. 4. (a) Schematic of the Ga_2O_3 MOSFET integrated with a high thermal conductivity substrate. (b) Layout of a silicon embedded cooling module (with microchannels) attached to the Ga_2O_3 substrate. For both cases, the Ga_2O_3 substrate was thinned down to 10 or 100 µm to reduce the junction-to-cooling medium thermal resistance.

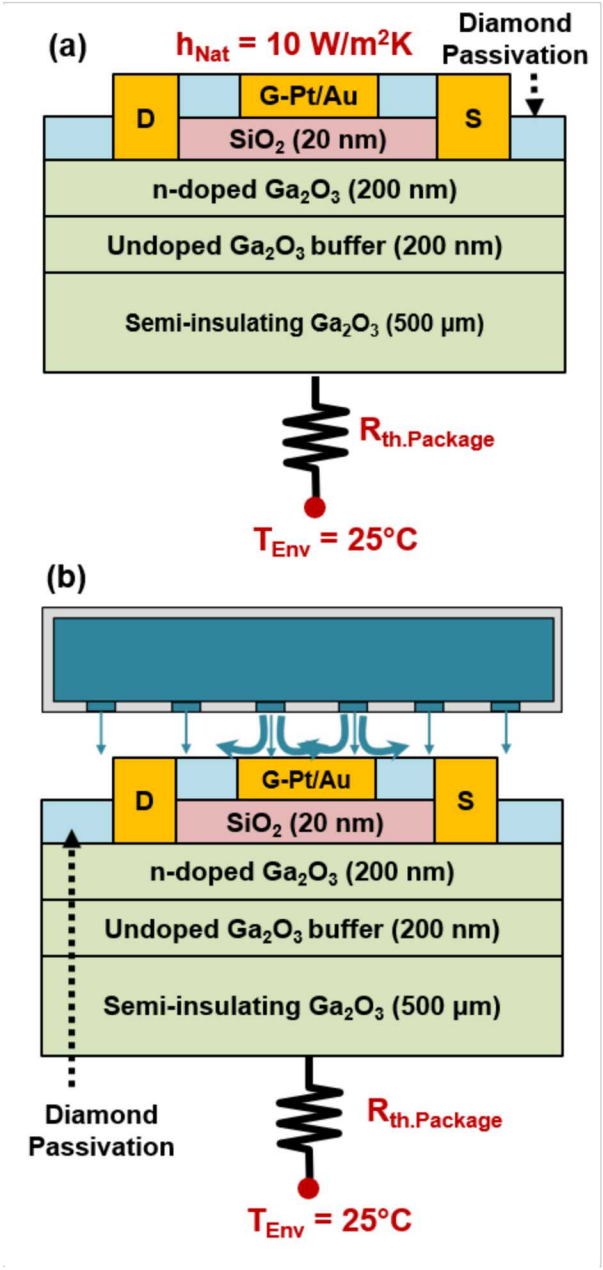

Fig. 5 (a) Schematic of Ga_2O_3 MOSFET employing NCD diamond passivation. (b) Layout of top-side air-jet impingement cooling with NCD diamond passivation.

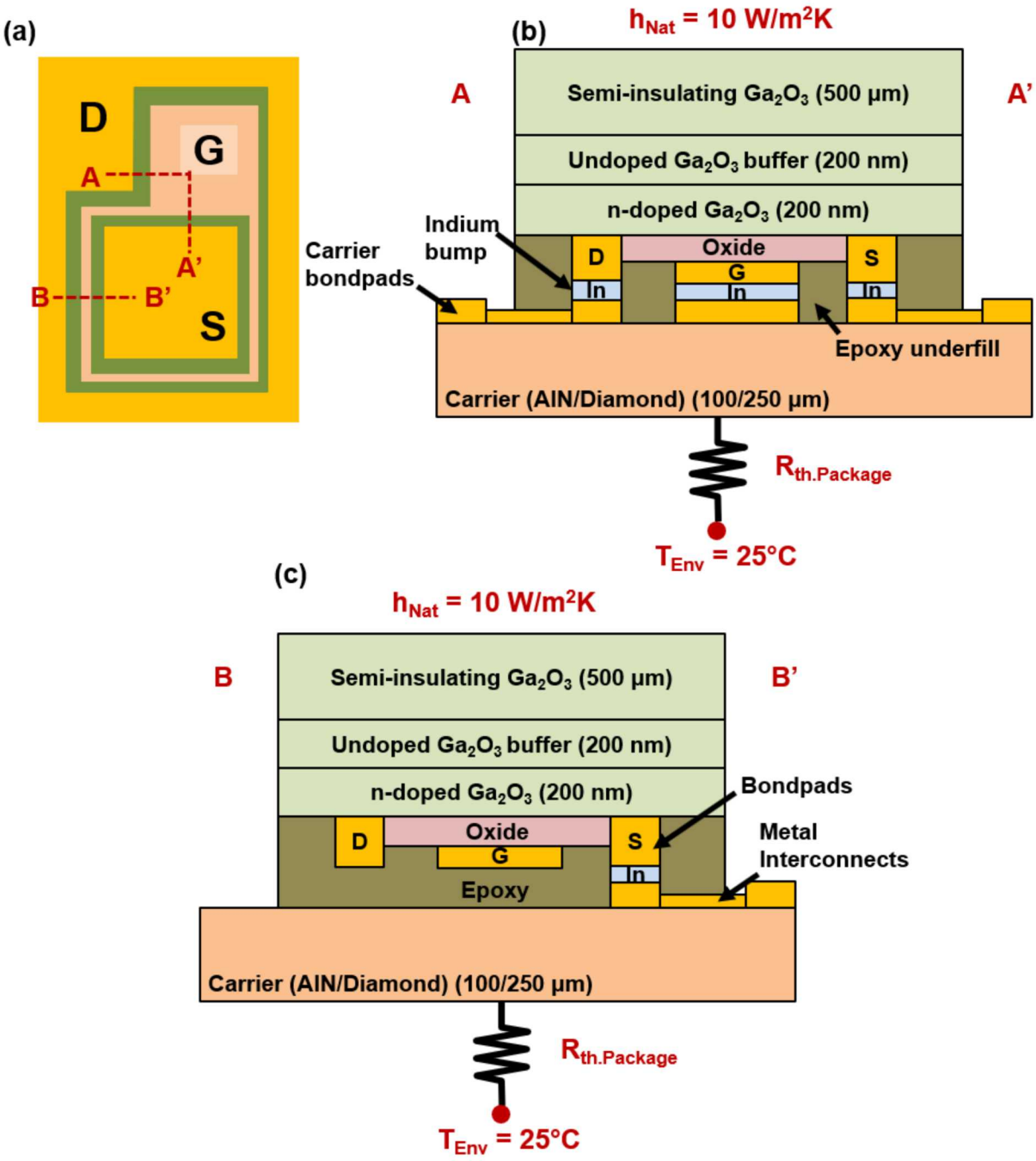

Fig. 6. Flip-chip hetero-integration of a Ga_2O_3 MOSFET onto a high thermal conductivity carrier wafer. (a) Device schematic. (b) Cross-sectional view showing electrical connection between the device and carrier wafer. (c) BB' cross-section. 3-D simulation was performed to evaluate the improvement offered by this design.

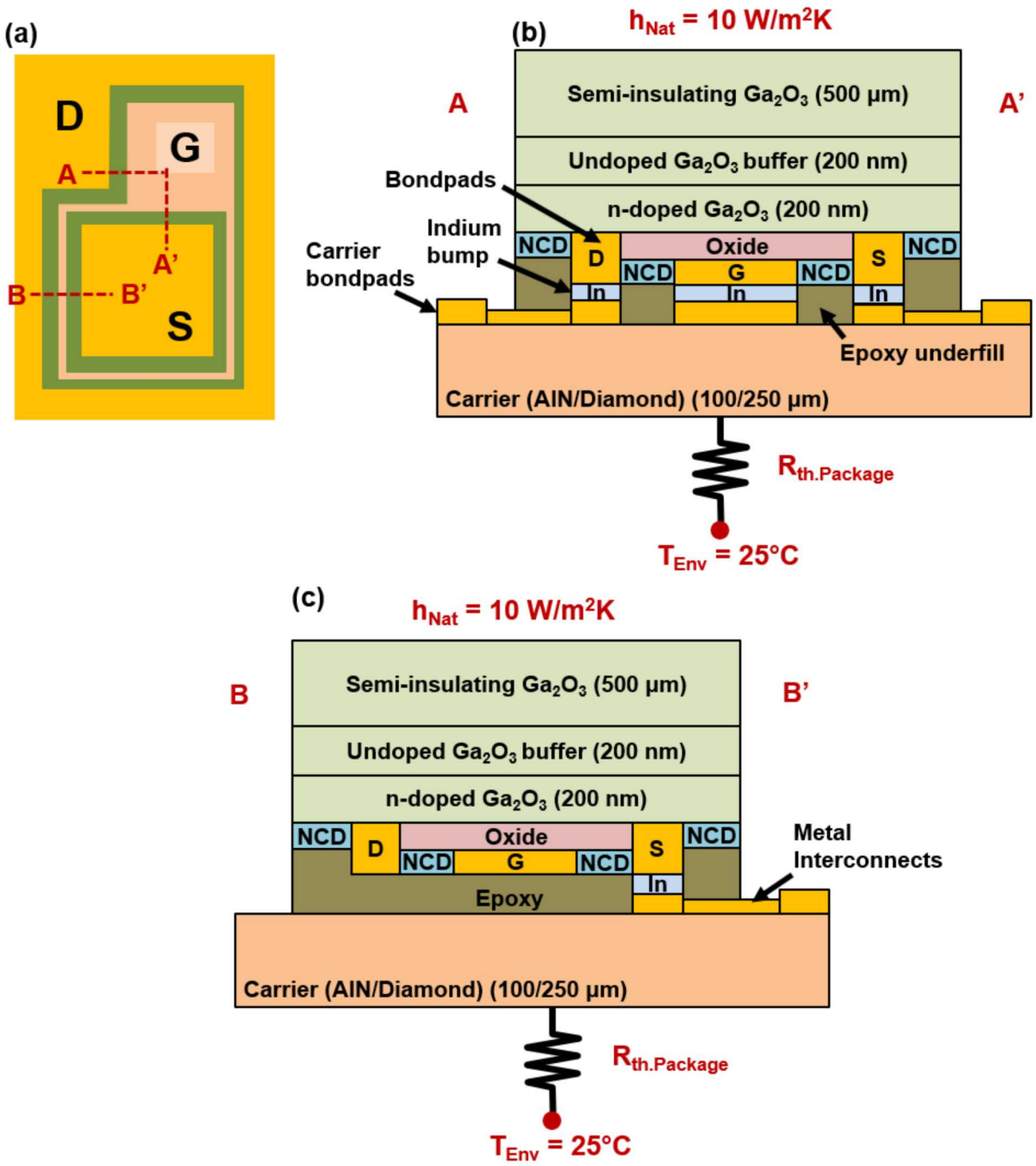

Fig. 7. Flip-chip hetero-integration of a Ga_2O_3 MOSFET employing nanocrystalline diamond (NCD) passivation. (a) Device schematic. (b) Cross-sectional view showing electrical connection between device and the carrier wafer. (c) The BB' cross-section. 3-D simulation was performed to evaluate the improvement offered by this design.

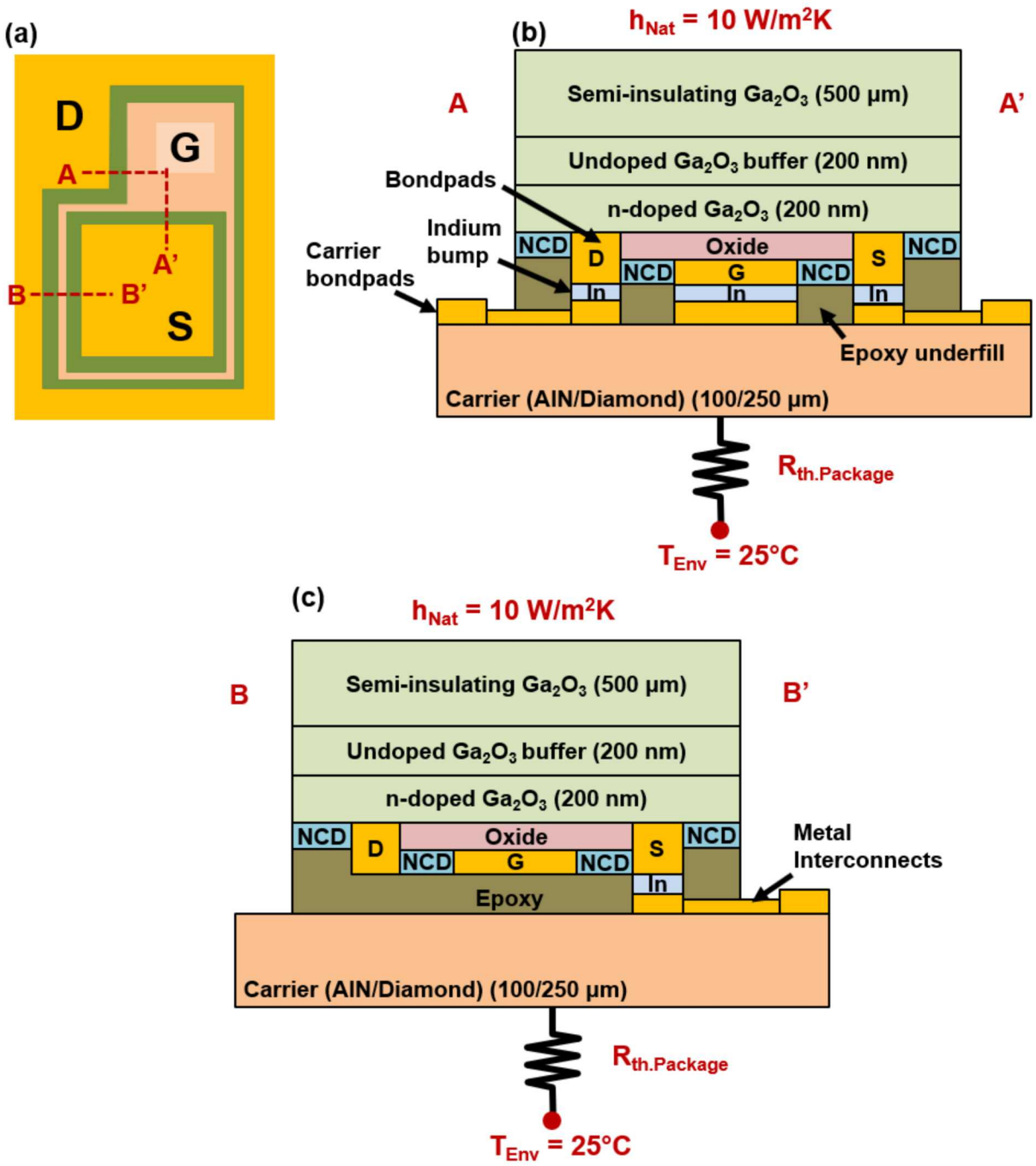

Fig. 8. Flip-chip hetero-integration of a Ga_2O_3 MOSFET combined with the use of NCD passivation and thermal bumps. (a) Device schematic. (b) AA' cross-sectional view. (c) The BB' cross-section showing heat sinks (i.e., thermal bumps) between the device channel region and the carrier wafer. 3-D simulation was performed to evaluate the improvement offered by this design.

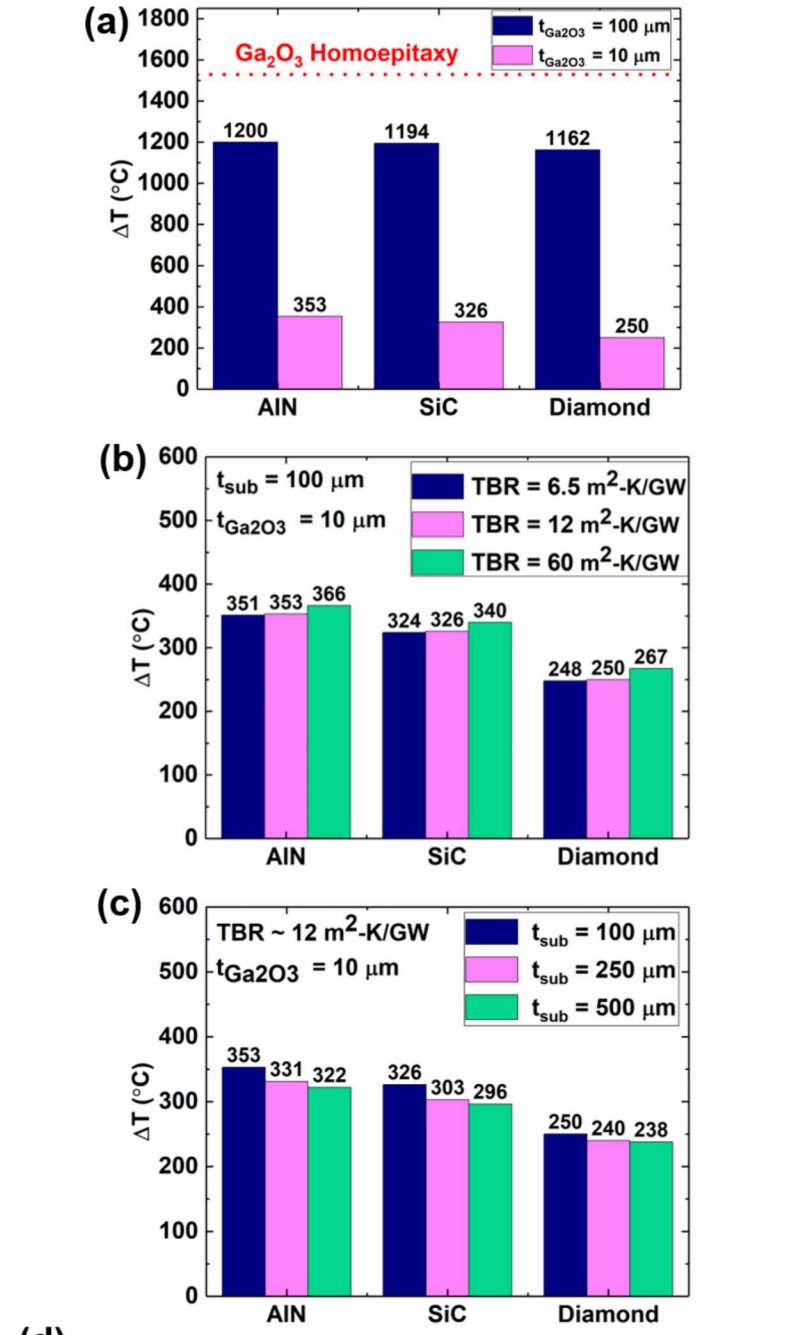
(a)
Ga2O3 Homoepitaxy
tGa2O3 = 100 µm
tGa2O3 = 10 µm
ΔT (°C)
1200
353
1194
326
1162
250
AlN
SiC
Diamond
(b)
tsub = 100 µm
tGa2O3 = 10 µm
TBR = 6.5 m2-K/GW
TBR = 12 m2-K/GW
TBR = 60 m2-K/GW
351 353 366
324 326 340
248 250 267
(c)
TBR ~ 12 m2-K/GW
tGa2O3 = 10 µm
tsub = 100 µm
tsub = 250 µm
tsub = 500 µm
353 331 322
326 303 296
250 240 238
(d)
Rth,j-p (K.mm/W)
AlN tsub = 100 µm
tsub = 500 µm
tGa2O3 = 100 µm
TBR = 60 m2K/GW
tGa2O3 = 10 µm
Diamond
TBR = 12 m2K/GW
TBR = 6.5 m2K/GW
High-κ substrate integration
Ga2O3 homoepitaxy
TBR
Ga2O3 (tGa2O3 = 10/100 µm)
High-κ substrate (tsub = 100/250/500 µm)
Rth, j-p
Rth, package
TEnv = 25°C

Fig. 9. (a) Reduction in the device channel temperature by engineering the substrate. Thinning down the native Ga_2O_3 substrate is the key to realizing superior thermal performance. (b) The effect of thermal boundary resistance (TBR) on the junction temperature rise (at 10 W/mm) for a Ga_2O_3 MOSFET (with a Ga2O3 thickness of 10 μm) integrated with 100 μm thick high thermal conductivity substrates including AlN, 4H-SiC, and diamond. (c) The effect of reducing the foreign substrate thickness at a fixed TBR of 12 m^2K/GW. (d) The thermal resistance waterfall diagram for high-κ substrate hetero-integration indicates that reducing the Ga_2O_3 thickness from 100 μm to 10 μm results in remarkable improvement in the device thermal performance.

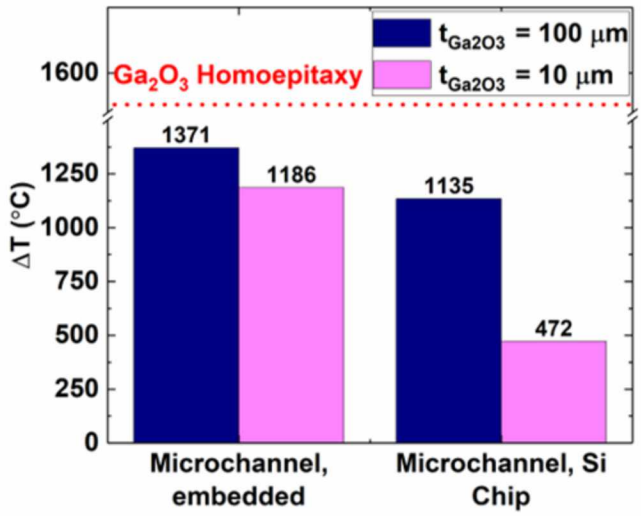

Fig. 10. Temperature rise for microchannel cooled devices. Two cases where microchannels were directly formed in the Ga_2O_3 substrate and enclosed in a Si-based embedded cooling module were studied. Thinning down the low thermal conductivity Ga_2O_3 substrate was found to be critical in order to reduce the device temperature.

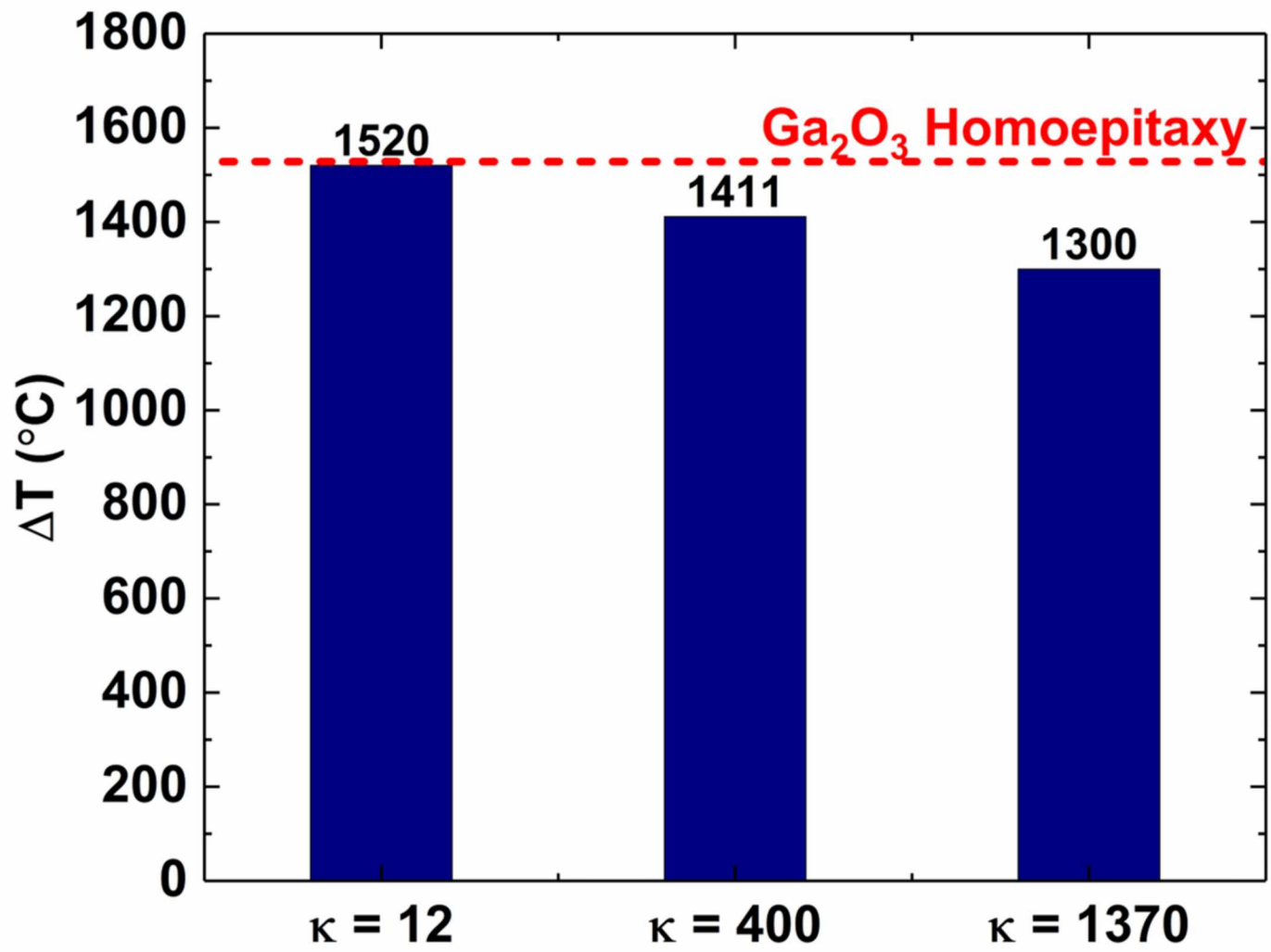

Fig. 11. Device peak temperature rise when nanocrystalline diamond (NCD) was employed as a top-side heat spreading passivation layer. This study was performed on a homoepitaxial Ga_2O_3 MOSFET with a substrate thickness of 500 μm.

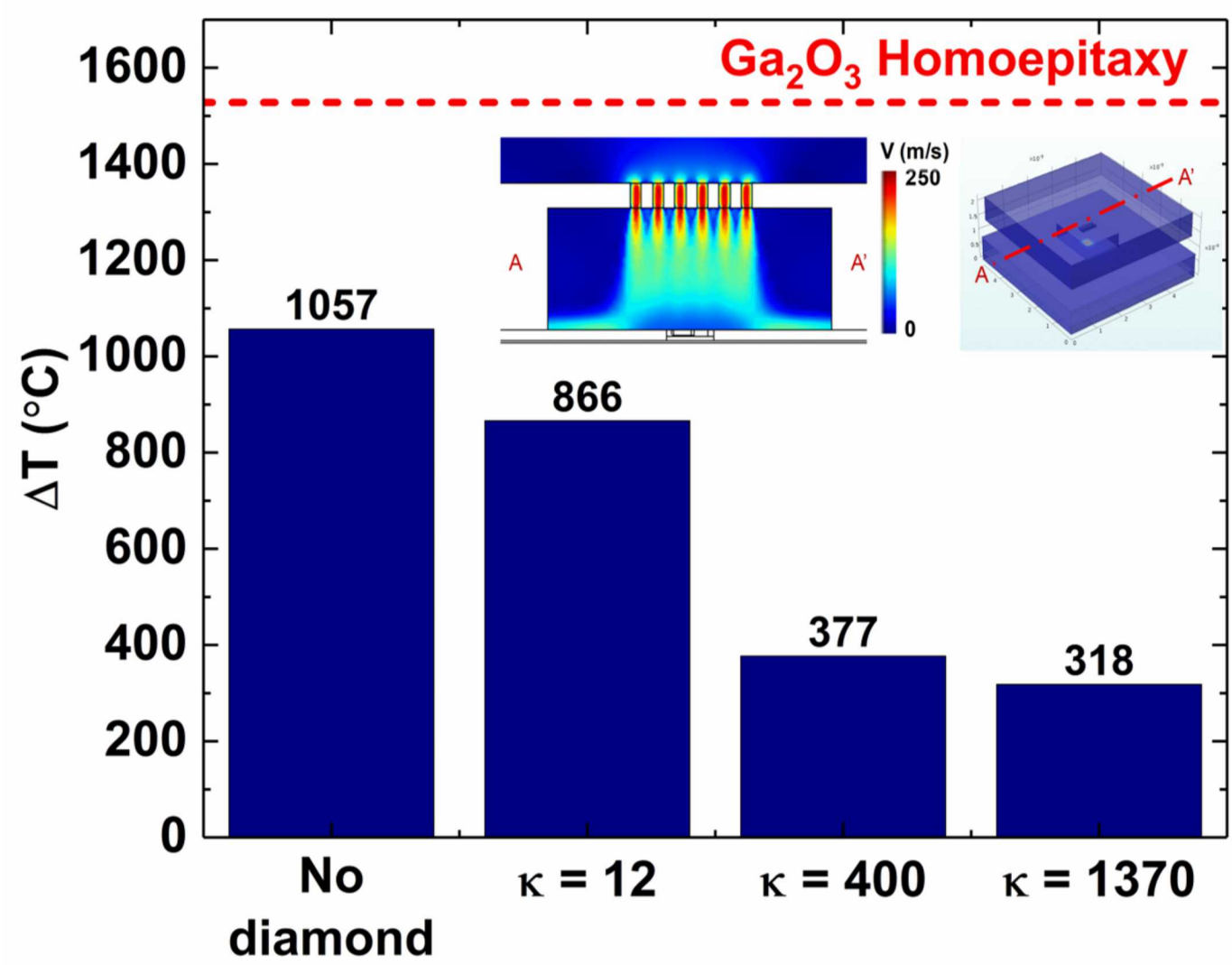

Fig. 12. Reduction of the device junction temperature rise by the combined use of air-jet impingement cooling and diamond passivation. This study was performed on a homoepitaxial device with a 500 μm thick substrate.

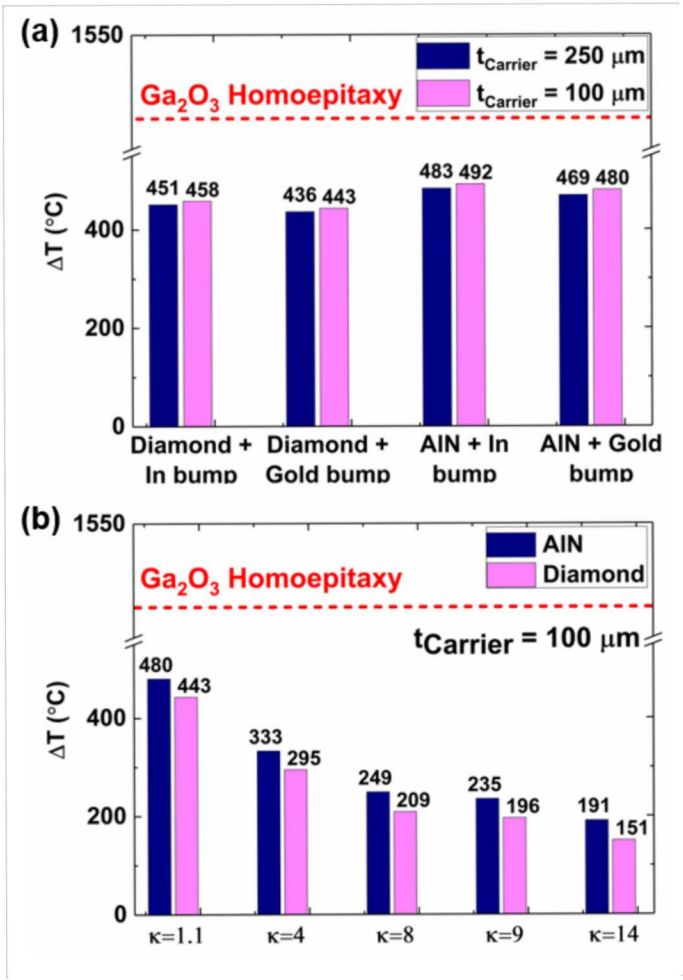

Fig. 13. (a). Device junction temperature rise at 10 W/mm as a function of the carrier wafer material (AlN vs. diamond), carrier thickness (100 μm vs. 250 μm), and electrical bump material (In vs. Au). (b) The effect of the thermal conductivity of the epoxy under-fill material to device temperature rise.

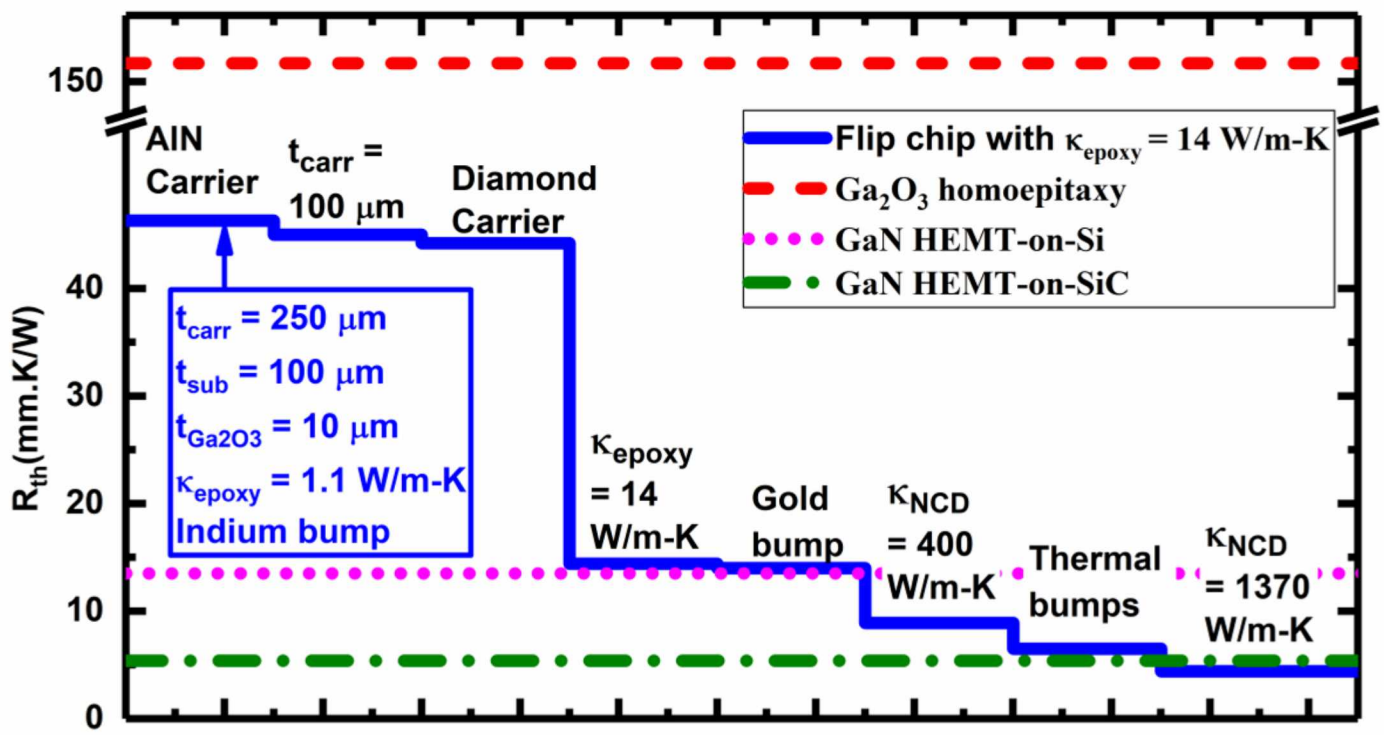

Fig. 14. Thermal resistance waterfall chart for flip-chip hetero-integration design schemes shown in Fig. 6-8. Each step corresponds to a single design modification. The chart shows the incremental improvement accrued by the carrier thickness (t_{carr})/material, along with the remarkable improvement in the thermal performance offered by a high thermal conductivity composite epoxy used to bond the device die and carrier wafer. By using thermal bumps in accordance with Fig. 8 in conjunction with NCD passivation (κ_{NCD}=1370 W/m-K), theoretically, a device thermal resistance lower than that for a GaN-on-SiC HEMT can be achieved.

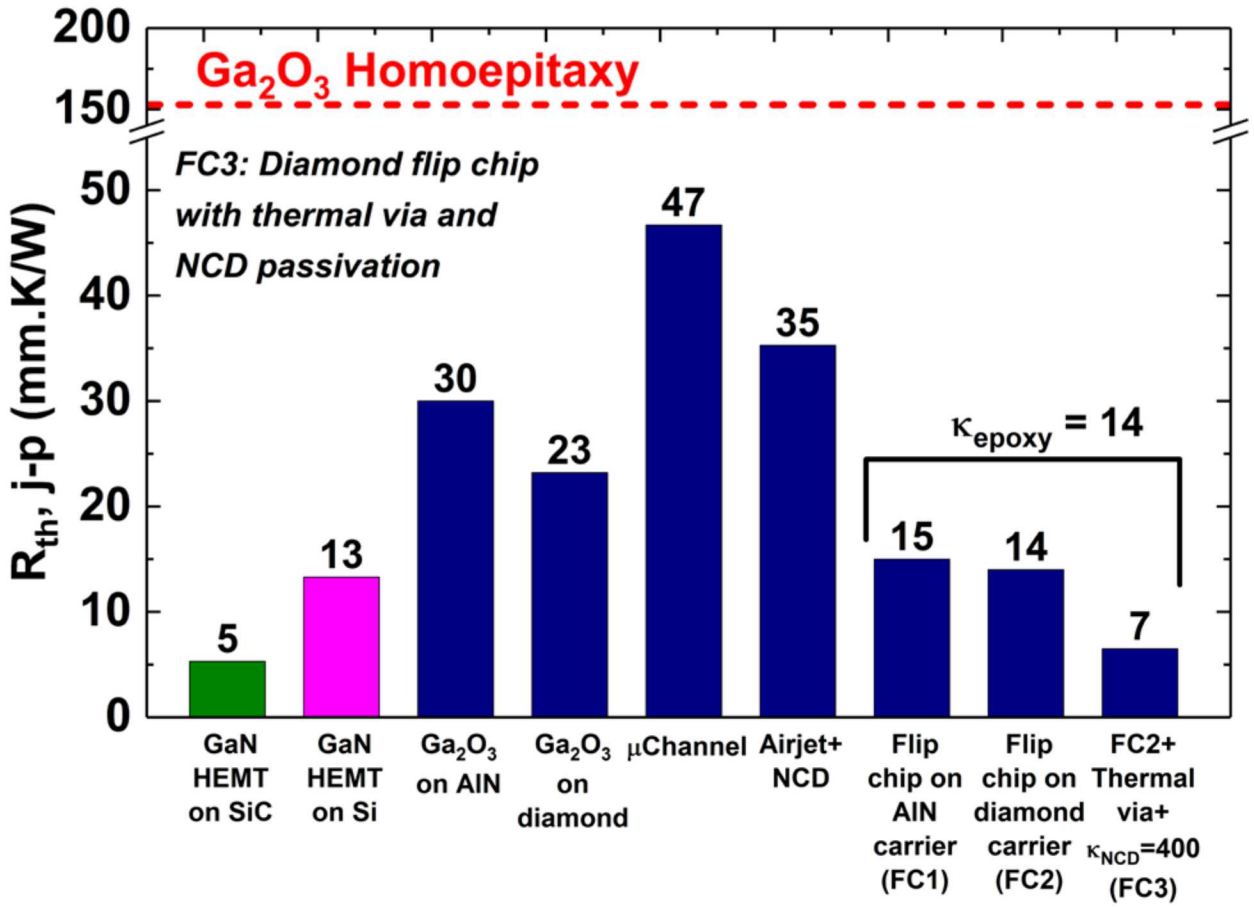

Fig. 15. Overall comparison of the device thermal resistance associated with the thermal management schemes studied in this work as well as the benchmark GaN-on-Si HEMT technology. Ga_2O_3 MOSFETs employing flip-chip hetero-integration using commercially available base materials enables to achieve a junction-to-package device thermal resistance value comparable with that for a GaN-on-Si HEMT. When the flip-chip design is augmented with NCD passivation and thermal heat sinks, the device thermal resistance can reach that of a GaN-on-SiC HEMT.

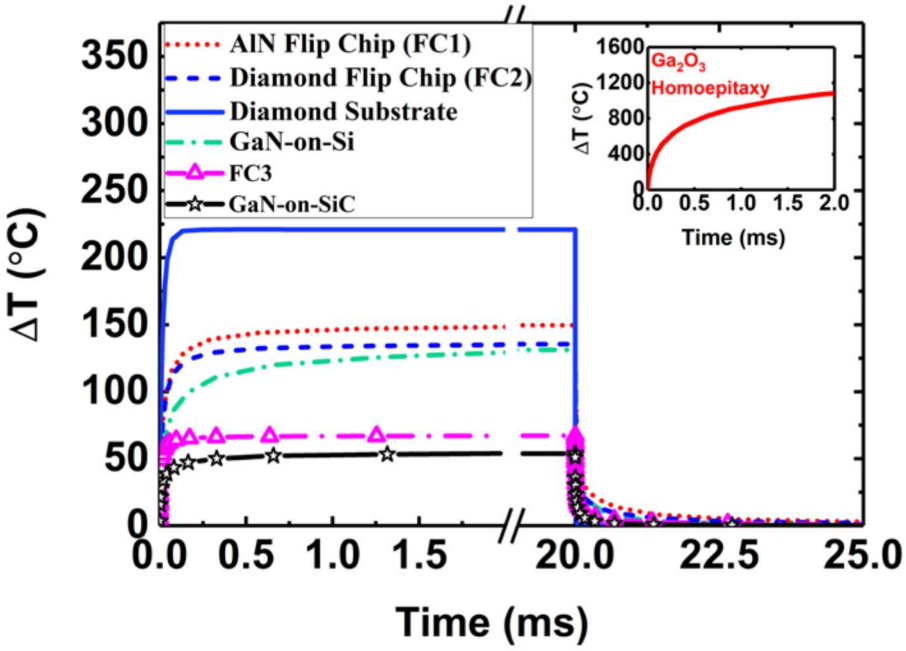

Fig. 16. Comparison of the thermal dynamics of a Ga_2O_3/diamond substrate-integrated MOSFET, a Ga_2O_3 MOSFET flip-chip integrated onto an AlN carrier wafer, a Ga_2O_3 MOSFET flip-chip integrated onto a diamond carrier wafer (FC2), a configuration where FC2 is augmented with thermal bumps and NCD passivation (FC3), a GaN-on-Si HEMT, and a GaN-on-SiC HEMT.

List of tables

Table I. Material properties and the Johnson's figure of merit (JFOM) for Si, 4H-SiC, GaN and Ga_2O_3 [14].

	Si	4H-SiC	GaN	Ga_2O_3
E_g (eV)	1.1	3.3	3.4	4.6-4.9
μ_n (cm^2/V-s)	1400	1000	2000	100-200
E_{cr} (MV/cm)	0.3	2.5	3.3	8
ε	11.8	9.7	9.0	10.0
Normalized JFOM $E_{cr}^2.v_{sat}^2/4\pi^2$	1	278	1089	2844
κ at 300 K (W/m-K)	150	370	210	27 [010] 11 [110]