Single-Event Characterization of the 16 nm FinFET Xilinx Kintex UltraScale+ Field-Programmable Gate Array in Heavy Ion Irradiation

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Abstract

This study examines the single-event response of the Xilinx 16 nm FinFET-based Kintex UltraScale Field-Programmable Gate Array (FPGA) irradiated with heavy ions. Results for single-event upset on configuration SRAM cells are provided, which show excellent SEU performance compared to previous Xilinx FPGA families. This study also describes a destructive single-event latch-up signature observed during testing.

Introduction

This study examines the single-event effects susceptibility of the latest UltraScale+ FPGA device family from Xilinx. These FPGAs are built with a TSMC 16 nm FinFET process and are categorized into Kintex, Virtex, and Zynq MPSoC families. The DUT selected for this experiment has the following characteristics:

Device	Xilinx Kintex UltraScale+ XCKU9P (ES2)
Package	FFVE900E (flip-chip, extended temperature grade)
Configuration	212,086,240 bits
Flip-Flops	548,160
BlockRAM™	32.1 Mbits (912 @ 36kb each)
Look-up Tables	274,080 LUTs, 6-input
Other device features	4 clock management tiles (total 4 MMCMs and 8 PLLs), 28 Transceiver blocks (16.3 Gbps), 10-bit ADC, 2,520 DSP slices

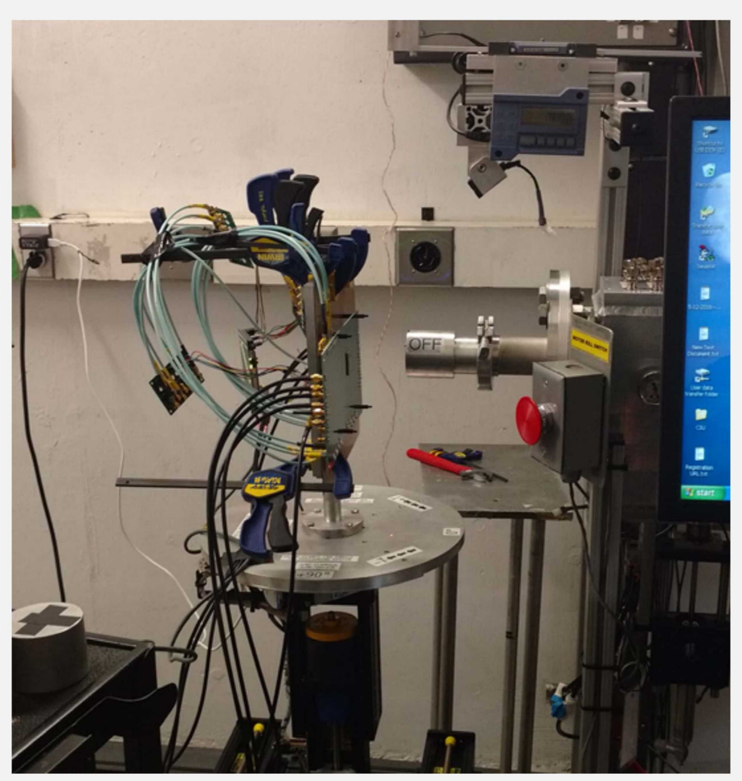
Test and Beam Parameters

This device was tested at the Texas A&M K500 Cyclotron in May of 2017. Irradiation was performed using Argon and Neon, which provided LETs ranging from 3.2 to 20.1 MeV-cm2/mg.

All irradiations were performed at normal incidence and at room temperature.

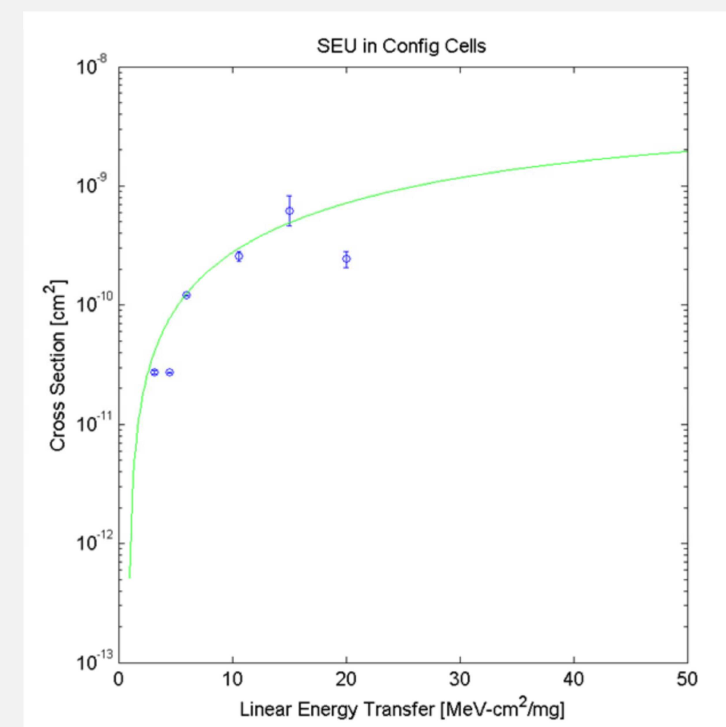
Prior to each run, the device was power cycled and programmed static design, comprised of pre-initialized flip-flop shift registers and BlockRAM. There was no running clock during the irradiation.

Scrubbing and readback operations were performed with the BYU JTAG Configuration Monitor using the FPGA's JTAG interface.



Single-Event Upset Results

- Static configuration memory test was performed by configuring, irradiating, and then reading back the device.
- Comparisons were masked to only include bits pertinent to device operation and to exclude dynamic content (such as user flip-flop data). The mask file provided by the Xilinx Vivado tools was used for this purpose. This led to an approximate total of 119 million bits being observed for upset.
- After normalizing the results for the number of 0s and 1s in the bitstream, the configuration cells storing "0" values appeared to upset more often than bits storing "1" by a ratio of ~4:1



Comparison to Previous Families

The SEU susceptibility of the Kintex UltraScale+ was compared to previous Xilinx families. There is significant improvement in SEU response, likely due to device scaling and the new FinFET-based transistor structures.

Configuration Memory Rates

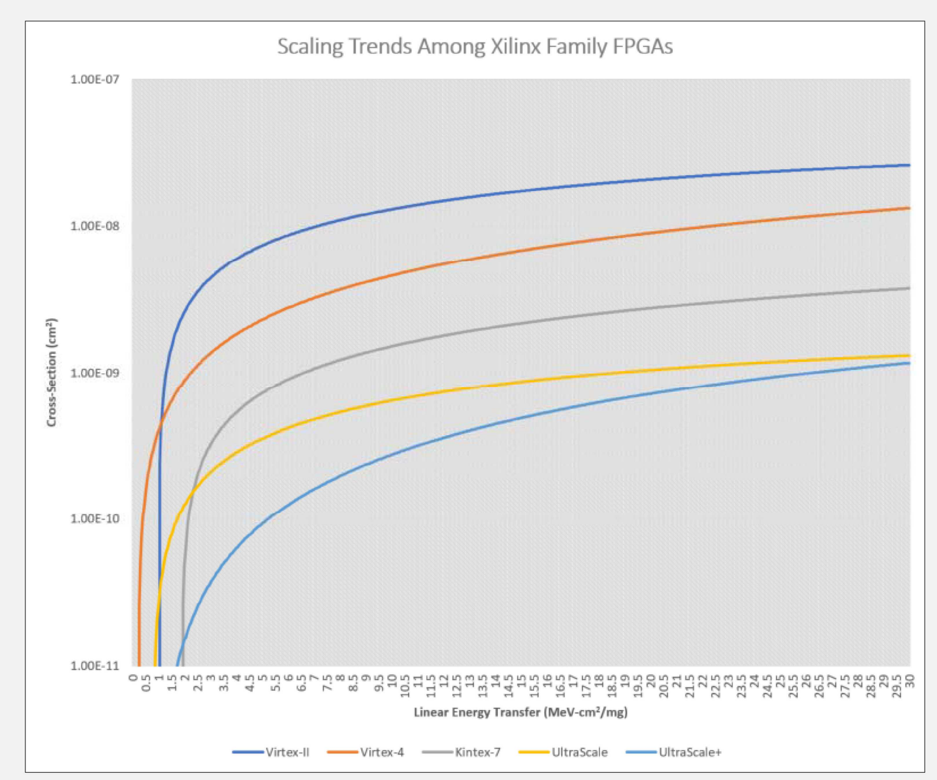
	per bit, per day	Improve-ment*	Node
Virtex-II	3.99E-07	1	130 nm
Virtex-4	2.63E-07	1.517	90 nm
Kintex-7	1.41E-08	28.298	28 nm
UltraScale	7.56E-09	52.778	20 nm
UltraScale+	1.33E-09	300.000	16 nm

** compared to Virtex-II*

Virtex-II and Virtex-4 data was gathered from:

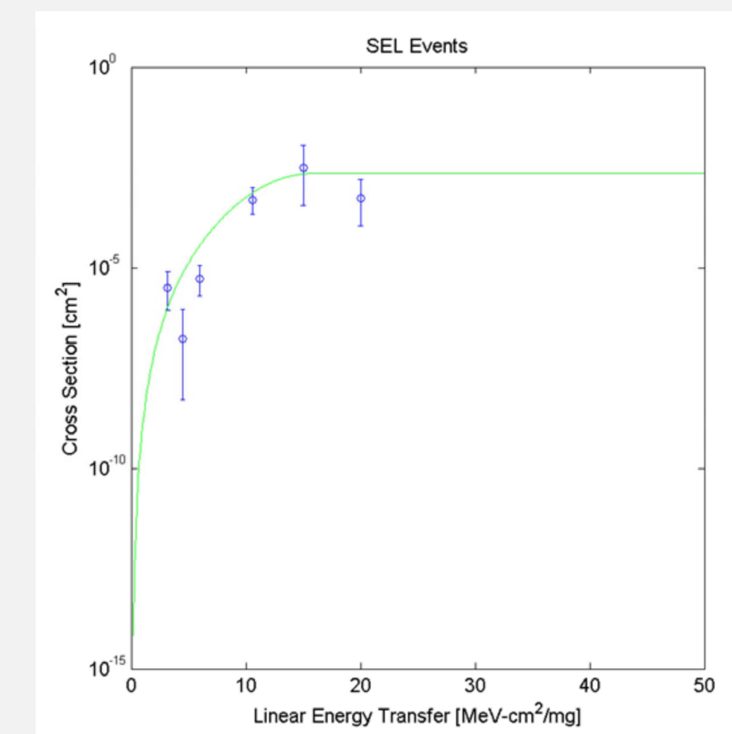
[Virtex-II] R. Koga, J. George, G. Swift, C. Yui, L. Edmonds, C. Carmichael, T. Langley, P. Murray, K. Lanes, and M. Napier, "Comparison of Xilinx Virtex-II FPGA SEE sensitivities to protons and heavy ions," *Nuclear Science, IEEE Transactions on,* vol. 51, no. 5, pp. 2825-2833, 2004.

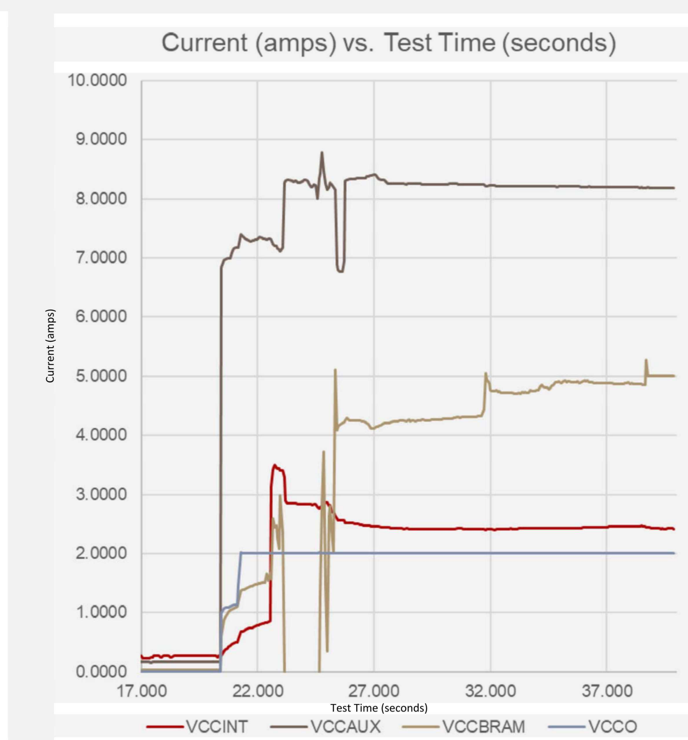
[Virtex-4] G. Allen, G. Swift, C. Carmichael, C. Tseng, and G. Miller, "Upset measurements on Mil/Aero Virtex-4 FPGAs incorporating 90 nm features and a thin epitaxial layer."



Single-Event Latch-up Results

- Single-Event Latch-up was observed at LET of 3.2 MeV-cm^2/mg at ambient temperature and normal voltage biases. (The actual LET threshold may be lower; testing was not performed below this LET)
- The VCCAUX power rail was always the first observed rail where a SEL event would begin.
- Latch-up-like behavior on other rails was observed, but always happened following a SEL on VCCAUX (probably due to die temperature increase).
- The device was non-functional following a SEL event where the current was not limited by the power supply and multiple latch-up sites were allowed to collect in the device. A graph of the current draw per power rail is shown below.





Event Rates

The event rates from CREME96 are listed below, assuming a GEO orbit, solar minimum conditions, and 100 mils of aluminum shielding:

	Configuration Memory	SEL Events
Per Bit	1.33E-9 / day	N/A
Per Device	0.28 / day (on 212M bits)	~0.01 / day

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