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Self-Aligned GaAs JFETs for Low-Power Microwave Amplifiers and RFICs at 2.4 GHz

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Abstract: Self-aligned GaAs JFET narrowband amplifiers operating at 2.4 GHz were designed and fabricated with both discrete JFETs as a hybrid amplifier and as RFICs. Enhancement-mode JFETs were used in order to be compatible with complementary digital logic. Hybrid amplifiers achieved 8-10 dB of gain at 2.4 GHz and 1 mW DC bias level. The RFIC achieved 10 dB of gain at 2.4 GHz and 2 mW DC bias level.

Introduction: Low power circuitry is very important for battery powered electronic components. While low power operation of digital circuitry is taken for granted due to the unique advantages offered by CMOS architecture, microwave circuits have no equivalent low power circuit configuration, require quiescent bias, and consequently have been reported infrequently in the literature. Commercial GaAs MESFET foundry technology was used to design and fabricate an amplifier with 15 dB of gain for 2-stages with 0.8 mW power at 1.25 GHz [1]. An HFET (heterostructure field effect transistor) amplifier RFIC (radio frequency integrated circuit) achieved 10 dB of gain at 0.5 mW and 900 MHz [2]. Amplifiers that operate at the 1 mW power level or lower have not been reported previously at higher frequencies.

Experimental: This work was adapted from a digital CHFET (complementary HFET) process [3] so as to ultimately provide for integrating microwave and digital functionality. Passive elements including ion implanted GaAs resistors, SiN dielectric capacitors with

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560 pF/mm^2 capacitance, and airbridge inductors were introduced into the CHFET process so as to make the RFIC fully compatible with digital ICs. Both discrete JFETs or RFICs were fabricated according to the process illustrated in Figure 1. Steps 1-5 illustrate the JFET fabrication. After alignment mark formation, the channel implants are performed using Si ions for the channel, Mg for backside confinement, and Zn for the p^+ region of the JFET gate [4]. The W refractory gate (0.7 x 100 μm^2 in this work) is defined and the p^+ region is etched away in the source and drain regions of the JFET. The Si ion implants for the self-aligned source/drain regions and the implant activation anneal then follow. JFET active regions are completed by ohmic contact formation. The implant and ohmic contact steps also serve to make the GaAs implanted resistors, with a sheet resistance of 400 Ω/square. Steps 6-11 are used to fabricate the transmission lines and the passive elements for a RFIC. The JFETs are passivated with SiN dielectric by plasma enhanced chemical vapor deposition (PECVD) and via holes are opened to contact the JFET gate and ohmic metals. A Ti/Pt/Au deposition and liftoff is used for the first metal which contacts the JFETs and also the GaAs substrate directly in the RFIC regions transmission lines and passive elements. The capacitor dielectric, SiN, is then deposited by PECVD. Patterning and deposition for the capacitor top electrode, a Ti/Pt/Au evaporation and liftoff then follows. Airbridge post definition followed by patterning and electroplating of the airbridge and transmission line metal complete the frontside processing. The final fabrication steps consist of wafer thinning to 100 μm, backside electroplating, die separation, and assembly. Frontside bond wires are used for grounding the RFIC. Microwave gain and return loss measurements were performed using an HP 8510C network analyzer using Cascade Microtech microwave probes calibrated using a TRL calibration.

Hybrid Amplifier An n-channel JFET was evaluated as a microwave device. This self-aligned JFET has previously been shown to operate with performance comparable to a

MESFET of the same gate length [4]. A narrow-band amplifier was selected as a test vehicle since its successful implementation demonstrates the feasibility of most RFIC functions. The low power digital applications require low bias voltages ($V_{DS} \approx 1$ V), a small positive gate threshold, and large gate turn-on voltages (>1 V). These design parameters are also ideal for low-power microwave applications. The voltages are very suitable for battery operation on a single cell and the positive gate threshold along with the large positive gate turn-on voltage, eliminates the need for a negative supply as commonly required with MESFETs. Though not explicitly designed for microwave operation, the JFET shows impressive low power microwave properties with $f_t > 13$ GHz and $f_{max} > 20$ GHz, measured at the 1 mW DC bias level.

S-parameters were measured at wafer level and used to design a narrow-band 2.4 GHz microstrip based amplifier. Amplifiers were fabricated on Rogers TMM-10 25 mil thick substrates. The measured gain vs. frequency is plotted in Figure 2 for three amplifiers using chip and wire assemblies. Peak gains between 8 and 10 dB were measured at 2.4 GHz and 1 mW DC power.

JFET RFIC: The hybrid amplifier was subsequently redesigned and fabricated as a RFIC with on-chip matching. The chip dimensions are 2.8 x 2.3 mm^2. After fabrication the RFIC was silver epoxied to a metal substrate along with chip capacitors for bias stability and alumina microstrip circuit adapters to facilitate microwave probing. The RFIC was designed for off chip bias control of the gate and drain so that it could be tested under various bias conditions. Shown in Figure 3 are plots of the gain (10 dB peak at 2.45 GHz, and input/output return loss (< -15 dB at 2.45 GHz) all measured at 2 mW DC bias condition ($V_{DS} = 2$ V, $I_D = 1$ mA). At 1 mW the gain drops to 7-8 dB. Good agreement with the earlier hybrid amplifier and the RFIC design goals was achieved.

Conclusion: Low power microwave technology results have been presented for 0.7 μm GaAs JFETs which are compatible with a digital CHFET technology. Both discrete and RFIC amplifiers were demonstrated which achieved 8-10 dB of gain at 2.4 GHz with 1-2 mW of DC power consumption.

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4. M. E. Sherwin, J. C. Zolper, A. G. Baca, R. J. Shul, A. J. Howard, D. J. Rieger, J. F. Klem, and V. M. Hietala, "An All Implanted Self-Aligned Enhancement Mode n-JFET with Zn Gates for GaAs Digital Applications," *IEEE Electron Device Letters*, 1994, **15**, pp. 242-244.

Figure Captions

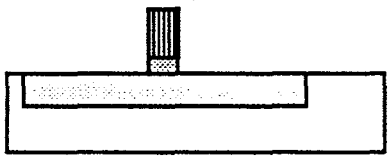
Figure 1. Process Sequence for JFET RFIC.

Figure 2. Gain characteristics of four packaged and three chip and die narrow-band amplifiers operating at 1 mW power.

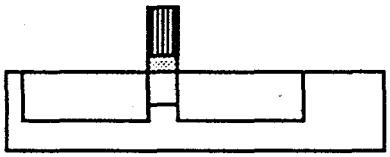
Figure 3. Measured gain and return loss of the JFET RFIC operated at a 2V, 1 mA (2 mW) bias level.

1-2. Alignment Mark and Channel Implants

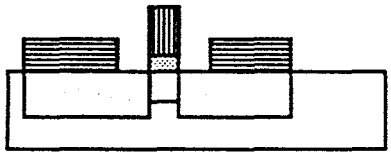
3. Gate and p^+ Etch



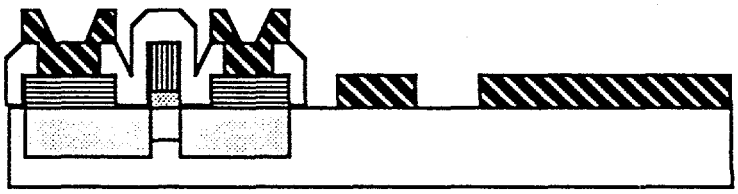
4. Source/Drain Implants & RTA



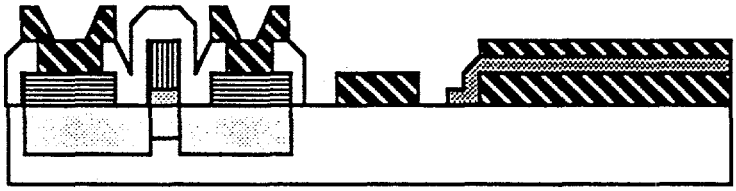
5. Ohmic Contacts



6-7. Via Dielectric and MET1



8-9. Capacitor Dielectric and Top Electrode



10-11. Aibridge Post and Plated Metal

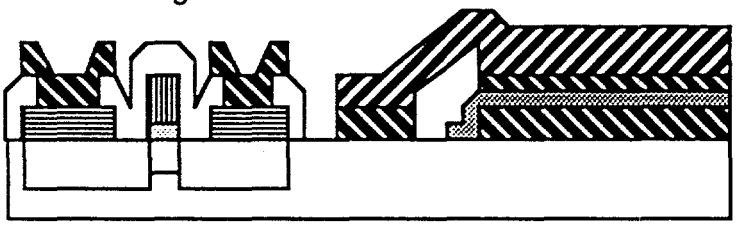


Figure 1.

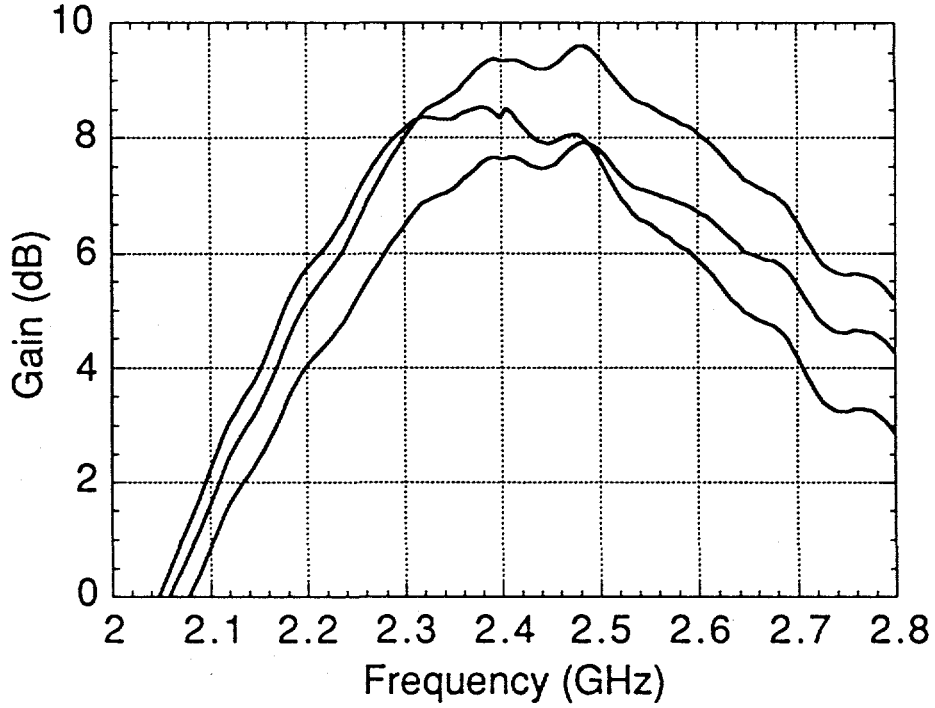


Figure 2

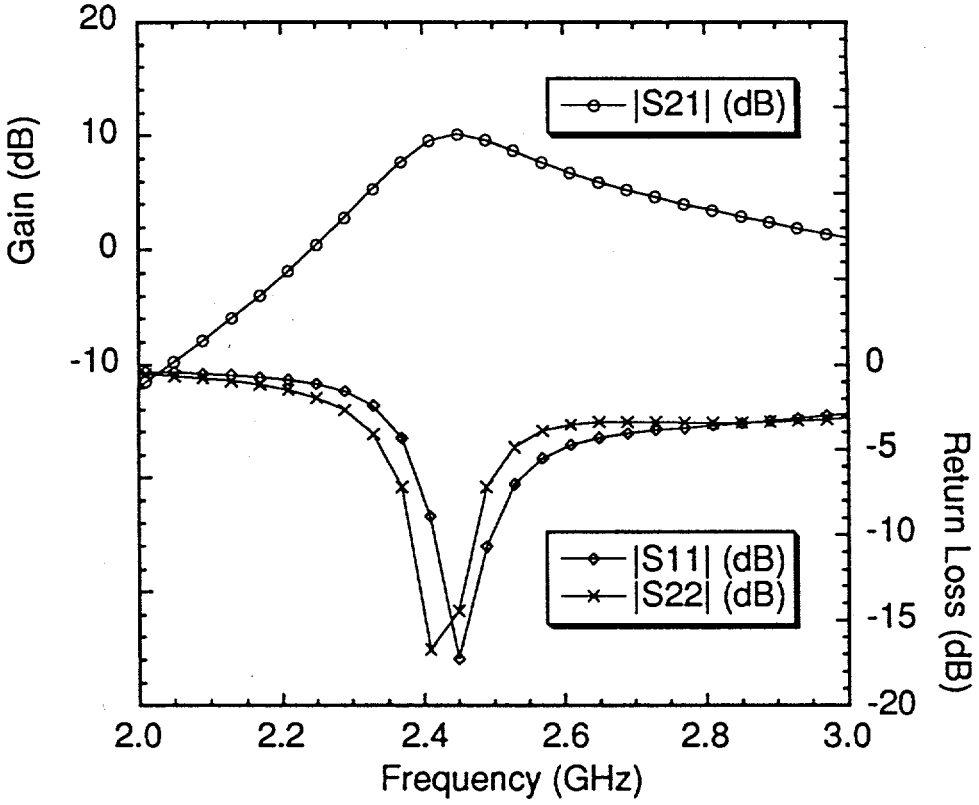

20
10
0
-10
Gain (dB)
|S21| (dB)
|S11| (dB)
|S22| (dB)
0
-5
-10
-15
-20
Return Loss (dB)
2.0
2.2
2.4
2.6
2.8
3.0
Frequency (GHz)

Figure 3.