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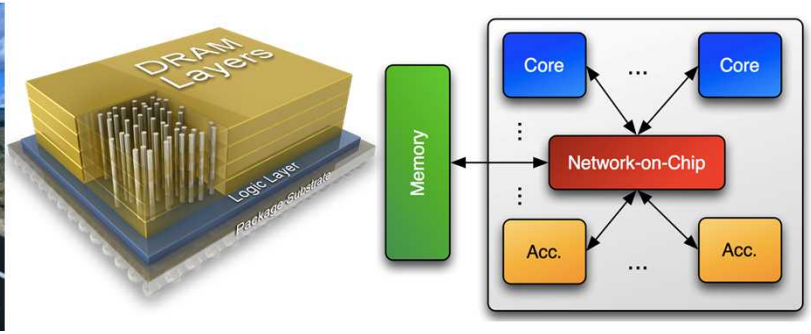

Impact of ECI on DOE Co-design Strategies

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Scalable Computer Architectures

The Salishan Conference on High Speed Computing

Gleneden Beach, OR

Random Access Talk, April 29, 2015

CENTER FOR COMPUTING RESEARCH

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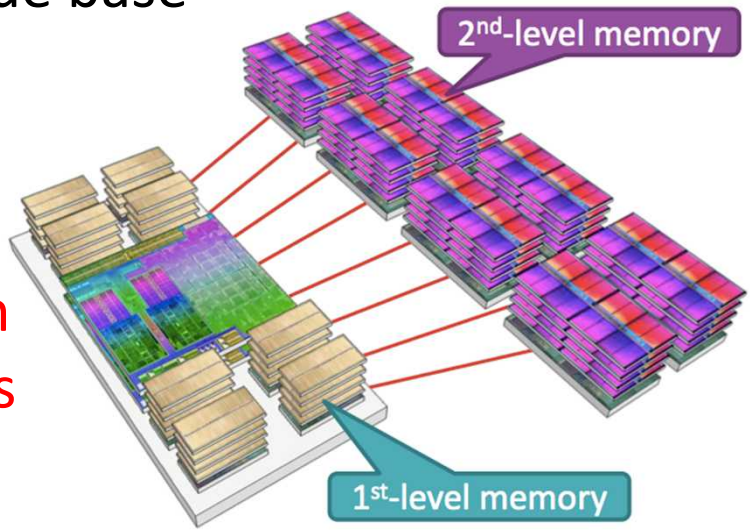
ECI Provides DOE a Key Opportunity

- Time frame and funding to:
  - Design hardware and system architectures
  - Modernize DOE's legacy applications portfolio
- ECI can support two complementary Co-design strategies
  - Hardware and System Architectures largely predetermined with a *clean sheet* on the application/algorithm side
  - Applications and Algorithms largely predetermined with a *clean sheet* on the hardware/system architecture side
- Both strategies require System Software R&D, but needed System Software capabilities may differ due to Application and Architecture differences

Clean Sheet development of Application/Algorithms with *a priori* defined HW/System Architectures

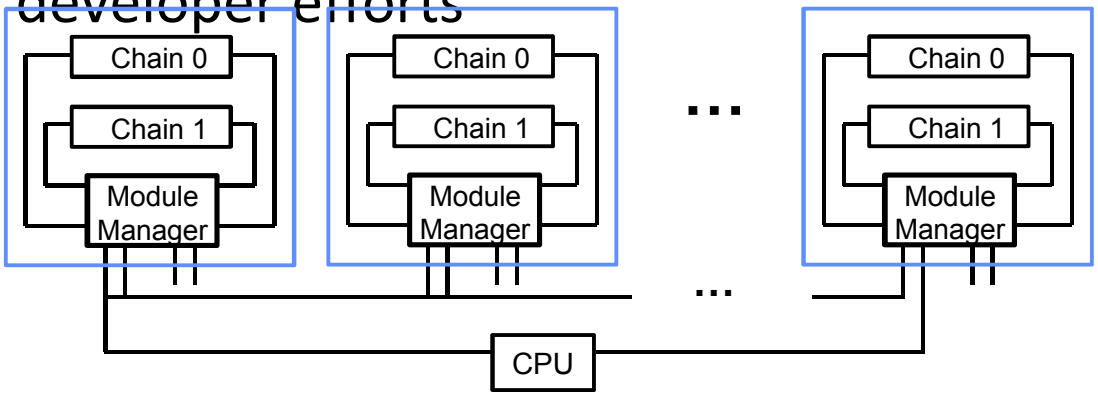
- This maps to an *Application-centric Proactive* Co-design path
- This approach has synergy with DOE/SC applications that are un-encumbered by a large legacy code base
- Note: Even if there were enough ECI budget to scale this strategy to the entire portfolio of DOE Legacy Applications, we do not have enough application and algorithm developers to rely solely on this strategy



e.g. AMD Two Level Memory Concept

Clean Sheet development of HW/System Architectures with *a priori* defined Applications/Algorithms

- ECI provides an opportunity to pursue a complementary strategy. This is an *Architecture-centric Proactive* Co-design path with a required "bridge" to DOE's portfolio of legacy applications.
- This strategy complements *Application-centric* by focusing Computer Industry R&D efforts on designs that reduce DOE application and algorithm developer efforts
- These two strategies, while *distinct* are not necessarily *independent*
- Progress in the strategies can inform each other, i.e., *Holistic* Co-design



e.g. Advanced Concept: *Modules of Chains of HMCs*

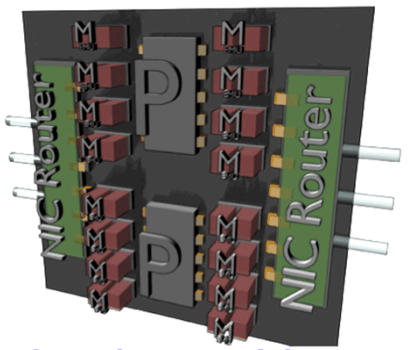
Final Thoughts about ECI Impact

- Despite misperceptions,
  ECI is not about reaching 10^{18} floating point operations per second
- We should not squander our ECI opportunity
- Prioritization criteria for DOE Exascale Co-design:
  - All Architecture R&D is not equal. Should prioritize efforts that ease the Application/algorithm developer burden.
  - All Application Development is not equal. Should prioritize approaches that can "bridge" to our legacy code base.
  - System Software Investments that support *these priorities* are critical to DOE Exascale Co-design

Backup Slides

Integration of commodity computing components into large scale MPPs

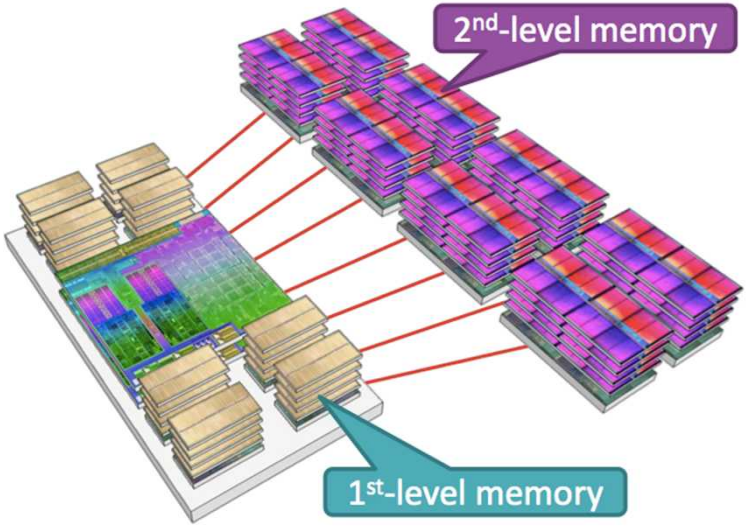
- Since the end of Dennard Scaling, and the subsequent introduction of multi-core processors and many-core accelerators, we have seen commodity computing capabilities depart further from DOE's needs for HPC.
- Our strategy of creating supercomputers from the integration of commodity computing components may still be valid, but we need to see *if* and *how* we can influence future commodity computing components.
- ***ECI provides the resources and time required to impact future commodity computing components***



Sandia Xcaliber Node Concept

Reactive Co-Design

- Proceed with the *status quo* – integrate commodity computing components into large scale MPPs
- Efforts focus on porting our application portfolio to architectures that integrate computing components that were originally design for other markets.
- Examples of technology HPC community is reacting to:
  - Multi and Many Core Processors
  - Heterogeneous Processors
  - Multi-tiered Memory
  - Commodity Interconnects

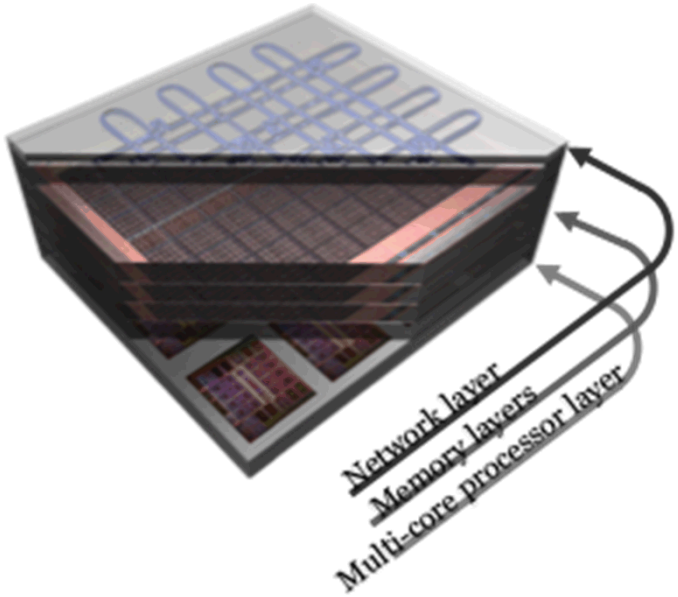


AMD Two Level Memory Concept

Proactive Co-Design

- In the absence of DOE Exascale Initiative, Risk Mitigation efforts are supported to develop new applications and algorithms for the known hardware and system architectures.

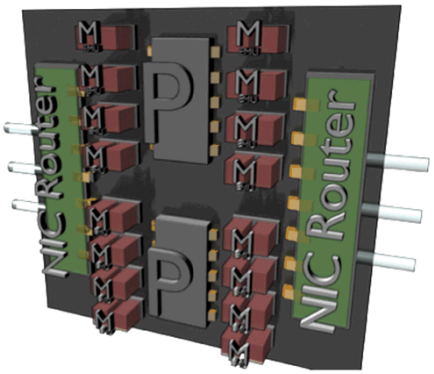
- DOE base program investments are also made with FF/DF and collaborations are established to influence the technology roadmaps for *future commodity* computing components and technology



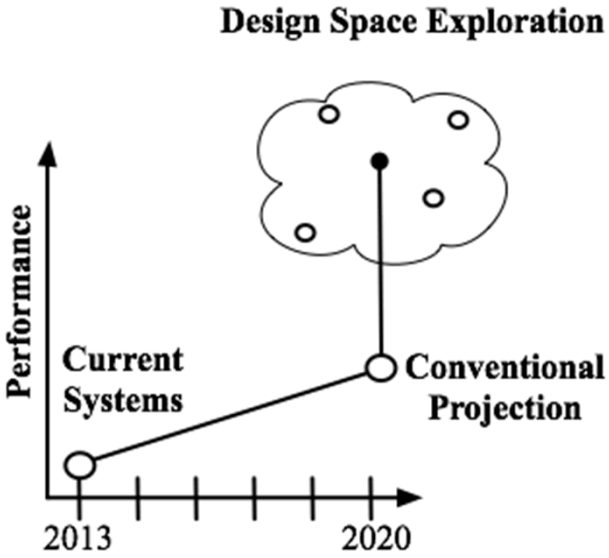
- Current and planned FF & DF projects establish a runway for future COTS

Holistic Co-Design

- The DOE Exascale initiative can also directly influence the design of both future computing components/systems for HPC and future applications/algorithms
- Leverage the System on Chip (SoC) Ecosystem to develop computing technology designs that are unconstrained by product roadmaps
- Develop *prototype* testbeds
  - Can lead directly to SoC products
  - Or be adopted by the COTS computing ecosystem



Sandia's Xcaliber Node Concept



Sandia's XGC Point Design/ Design Space Exploration