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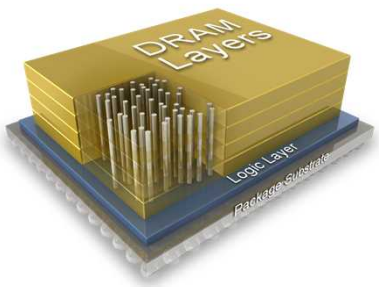

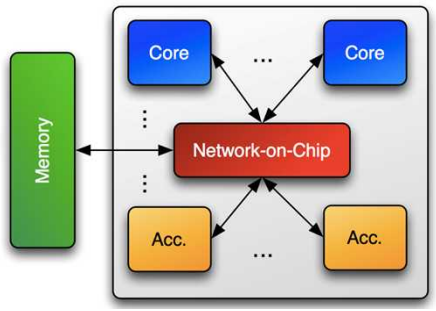

Impact of the Exascale Computing Initiative

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Scalable Computer Architectures

CENTER FOR COMPUTING RESEARCH

U.S. DEPARTMENT OF ENERGY | NNSA National Nuclear Security Administration

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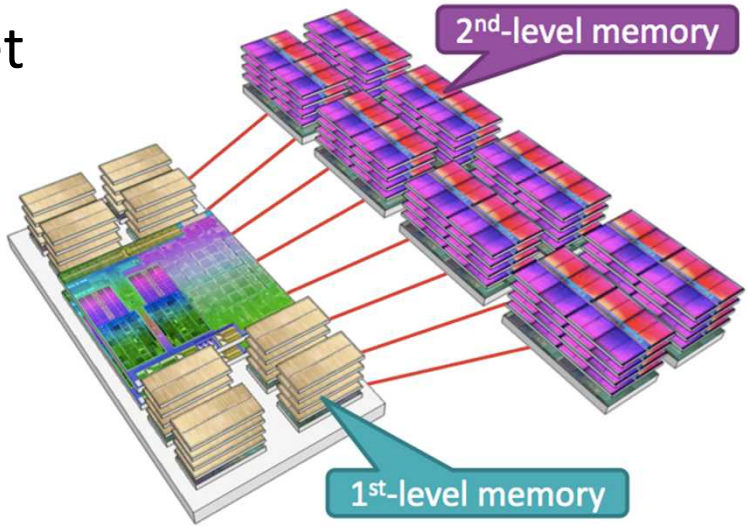
ECI Provides a Key Opportunity

- Time frame and funding to design hardware and system architectures
- DOE can pursue two complimentary Co-design strategies
  - Hardware and System Architectures largely predetermined with a *clean sheet* on the application/algorithm side
  - Applications and Algorithms largely predetermined with a *clean sheet* on the hardware/system architecture side
- Both strategies support System Software R&D, but required capabilities may differ due to Hardware/System Architecture differences

Clean Sheet development of Application/Algorithms with *a priori* defined HW/System Architectures

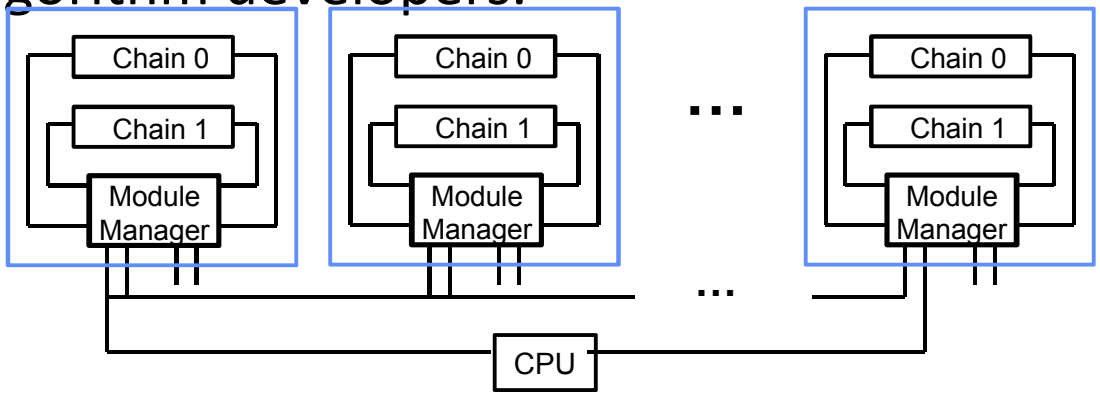
- ASC calls this strategy "Advanced Technology Development and Mitigation" (ATDM) and this maps to an Application-centric *Proactive* Co-design path
- This approach will have synergy with those ASCR applications that are un-encumbered by a large legacy code base
- Even if there were enough ECI budget to scale this strategy to the entire portfolio of ASC Legacy Applications, we do not have enough application and algorithm developers to rely solely on this strategy



AMD Two Level Memory Concept

Clean Sheet development of HW/System Architectures with *a priori* defined Applications and Algorithms

- ECI provides an opportunity to pursue a complimentary strategy to ATDM. This is an architecture-centric *Proactive* co-design path with a required "Bridge" to DOE's portfolio of legacy applications.
- This strategy compliments ATDM by focusing Computer Industry R&D efforts in a way that reduces the effort that will be required of DOE application and algorithm developers.
- These two strategies, while *distinct* are *not independent*
- Progress in one strategy can inform the other, and vice versa



Advanced Concept: *Modules of Chains of HMCs*

Final Comment about ECI Impact

- Despite recent Congressional language,

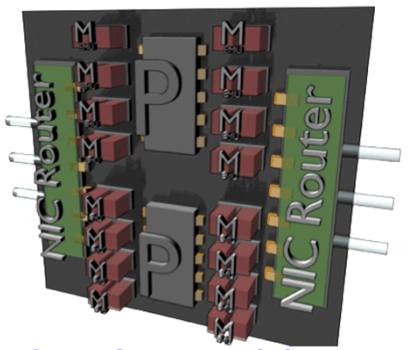
  ECI is <u>not</u> about reaching 10^{18} floating point operations per second

- We should not squander the ECI opportunity

Backup Slides

Integration of commodity computing components into large scale MPPs

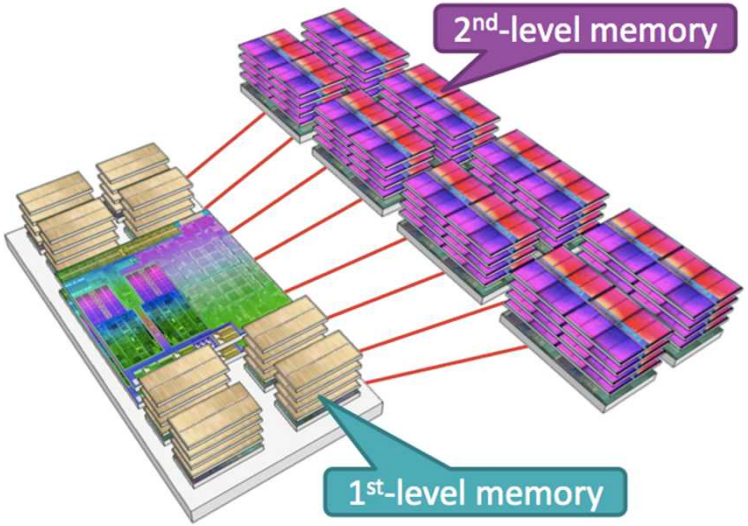
- Since the end of Dennard Scaling, and the subsequent introduction of multi-core processors and many-core accelerators, we have seen commodity computing capabilities depart further from DOE's needs for HPC.
- Our strategy of creating supercomputers from the integration of commodity computing components may still be valid, but we need to see *if* and *how* we can influence future commodity computing components.
- ***ECI provides the resources and time required to impact future commodity computing components***



Sandia Xcaliber Node Concept

Reactive Co-Design

- We proceed with the *status quo* – integrate commodity computing components into large scale MPPs
- DOE efforts focus on porting our application portfolio to architectures that integrate computing components that were originally design for other markets.
- Examples of technology we are reacting to:
  - Multi and Many Core Processors
  - Heterogeneous Processors
  - Multi-tiered Memory
  - Commodity Interconnects



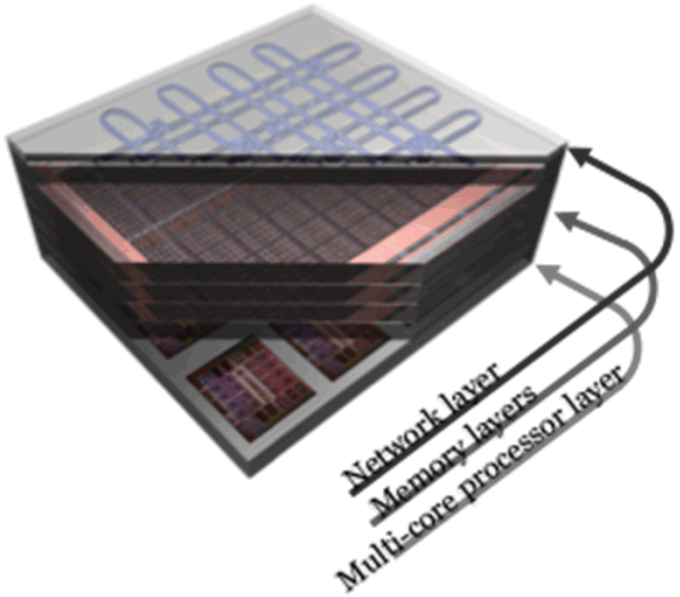
AMD Two Level Memory Concept

Proactive Co-Design

- In the absence of DOE Exascale Initiative, Risk Mitigation efforts are supported to develop new applications and algorithms for the known hardware and system architectures.

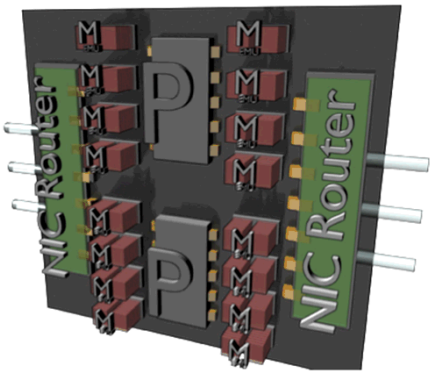
- DOE Investments are also made with FF/DF and collaborations are established to influence the technology roadmaps for *future commodity* computing components and technology

- Current and planned FF & DF projects establish a runway for future COTS

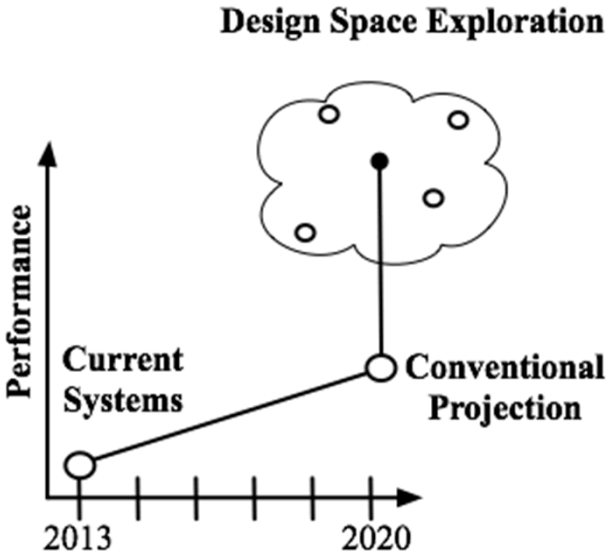


Holistic Co-Design

- The DOE Exascale initiative can also directly influence the design of both *future special purpose* HPC computing components/systems and future applications/algorithms
- Leverage the System on Chip (SoC) Ecosystem to develop computing technology designs that are unconstrained by product roadmaps
- Develop *prototype* testbeds
  - Can lead directly to SoC products
  - Or be adopted by the COTS computing ecosystem



Sandia's Xcaliber Node Concept



Sandia's XGC Point Design/ Design Space Exploration