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TWO-CHANNEL WAKEUP SYSTEM EMPLOYING ALUMINUM NITRIDE BASED MEMS RESONANT ACCELEROMETERS FOR NEAR-ZERO POWER APPLICATIONS

Robert W. Reger, Sean Yen, Bryson Barney, Michael Satches, Andrew I. Young, Tammy Pluym, Michael Wiwi, Matthew A. Delaney, and Benjamin A. Griffin
Sandia National Laboratories, Albuquerque, New Mexico, USA

ABSTRACT

The Defense Advanced Research Project Agency has identified a need for low-standby-power systems which react to physical environmental signals in the form of an electrical wakeup signal. To address this need, we design piezoelectric aluminum nitride based microelectromechanical resonant accelerometers that couple with a near-zero power, complementary metal-oxide-semiconductor application specific integrated circuit. The piezoelectric accelerometer operates near resonance to form a passive mechanical filter of the vibration spectrum that targets a specific frequency signature. Resonant vibration sensitivities as large as 490 V/g (in air) are obtained at frequencies as low as 43 Hz. The integrated circuit operates in the subthreshold regime employing current starvation to minimize power consumption. Two accelerometers are coupled with the circuit to form the wakeup system which requires only 5.25 nW before wakeup and 6.75 nW after wakeup. The system is shown to wake up to a generator signal and reject confusers in the form of other vehicles and background noise.

INTRODUCTION

Through the Near-Zero Power RF and Sensor Operations (N-ZERO) program, the Defense Advance Research Project Agency (DARPA) is addressing needs for near-zero-power wakeup systems that monitor activity in remote locations [1]. The power budget of deployed systems is presently dominated by their standby power consumption because events of interest are typically infrequent. Commercial-off-the-shelf (COTS) solutions to infrequent wakeup events have costly battery maintenance or replacement cycles on the order of weeks to months, making them infeasible for use in wide ranging, distributed system architectures.

Piezoelectric based microelectromechanical systems (MEMS) offer solutions for sensing infrequent events as they require zero input power to produce an electrical output. Therefore, the only power requirement comes from the external decision-making circuit. The complementary metal-oxide semiconductor (CMOS) application specific integrated circuit (ASIC) employs current-starvation and sub-threshold biasing to ensure that the decision-making circuit also operates at near-zero power, roughly defined as 10 nW or less.

In this work we employ aluminum nitride (AlN) as the piezoelectric material. AlN is commonly used in radio-frequency filter applications for cellular phones. Piezoelectric AlN is chosen over other piezoelectric thin films, such lead zirconate titanate (PZT), due to is superior open circuit sensitivity coefficient, larger signal-to-noise ratio, and established, large volume manufacturing base [2]. Unlike PZT or zinc oxide, AlN is also fully CMOS compatible allowing for future CMOS integration leading to increased performance gains [3].

Here, we develop a near-zero-power sensor system employing AlN based MEMS resonant accelerometers (Figure 1) coupled with an ASIC operating at sub-threshold, designed for infrequent wakeup applications. Two accelerometers are employed simultaneously to increase system robustness to false positives. We start with the design, fabrication, and characterization of the resonant accelerometer. Then we discuss the CMOS ASIC in a piecewise manner, beginning with the bias cell, moving to the comparator and concluding with the self-latching comparator circuit. We then discuss the integrated system level performance and conclude with future work.

ACCELEROMETER

Design

While conventional accelerometers are designed to operate over a large bandwidth below resonance, resonant accelerometers operate with a narrow bandwidth near resonance [4]. A high quality factor resonant response increases sensitivity over that of a flat-band accelerometer and attenuates undesirable out-of-band signals. Thus, the sensors act as passive filters in the mechanical domain.

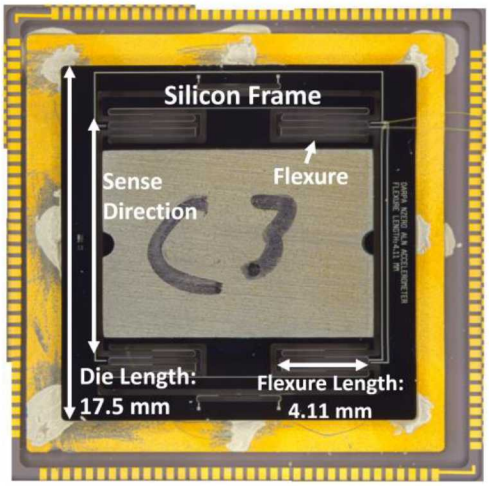

Figure 1 - Packaged resonant MEMS accelerometer with tungsten proof mass.

The resonant accelerometers discussed herein are full-wafer thickness and consist of an outer silicon frame connected to a large proof mass by four single-crystal silicon compliant tethers. Each tether is a double-folded flexure with AlN incorporated for zero-power transduction of physical strain into an electrical output. The resonant frequency of the devices is set by the stiffness of their flexures (k) and the proof mass (m),

$$f_r = \frac{1}{2\pi}\sqrt{\frac{k}{m}}.$$

Instead of using a silicon proof mass defined exclusively by microfabrication processes, we incorporate *macro*-machined tungsten plugs (with 10× the density of silicon) during packaging. These tungsten plugs provide two advantages: 1.) They enable higher quality factors due to increased mass ($Q \propto \sqrt{km}$) and 2.) They allow tuning of the resonant frequency post-fabrication due to the modularity.

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Fabrication

The fabrication process for the resonant accelerometers is provided in Figure 2. (a) Start with a 675 µm high-resistivity silicon wafer with 1 µm oxide. Etch 200 nm into the oxide, deposit tungsten, and performed a chemical mechanical polish to form tungsten plugs for via formation. (b) Pattern 20/50/100 nm titanium/titanium nitride/aluminum bottom metal for electrodes. (c) Deposit 750 nm AlN. (d) Etch through the AlN to form vias to the tungsten, then deposit and pattern the top electrode (100/25 nm aluminum/titanium nitride). (e) Pattern to form the frame and flexures and etch films down to silicon then (f) DRIE through the full silicon wafer.

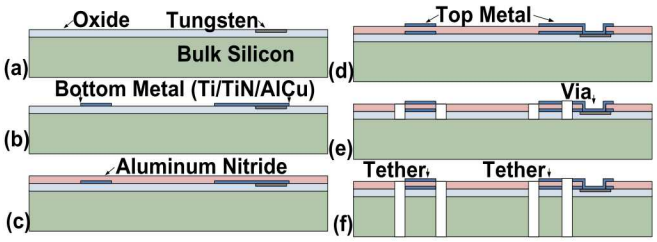

Figure 2 - Accelerometer fabrication process.

Characterization

The MEMS accelerometers are characterized without the CMOS present on a Data Physics Corporation S-011 shaker. A broadband reference accelerometer is included on the shaker for calibration. Figure 3 shows the time series response of the MEMS and reference accelerometers provided a Honda 6500 personal generator as the input signal. The MEMS accelerometer filters the frequency content contained in the reference signal to such a degree that the MEMS output appears to be purely sinusoidal.

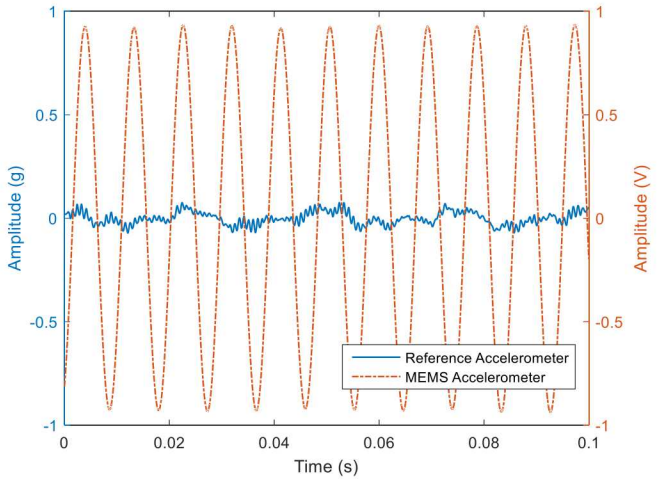

Figure 3 - Comparison of the time series output from a reference accelerometer and the MEMS accelerometer given the generator input. The MEMS accelerometer mechanically filters the generator input to the frequency of interest.

Shown in Figure 4 is a sample transfer function (V/g) utilizing the MEMS and reference accelerometers. The resonant MEMS accelerometers have been demonstrated with resonant frequencies as low as 43 Hz, resonant sensitivities as high as 490 V/g, and quality factors over 12,500.

CMOS ASIC

A near-zero-power ASIC fabricated in Sandia's CMOS7 process interrogates the electrical output of the piezoelectric accelerometer. Sandia's CMOS7 is a 0.35 µm trench-isolated silicon-on-insulator process. The power consumption is minimized using low-current, long-channel transistors (W/L = 2 µm/20 µm) in sub-threshold biasing, and current starvation in the circuits (bias current 0.75 nA). In addition, the power supply is reduced to V_{DD} = 1 V. The ASIC contains a pair of comparator/latch circuits (Figure 5) connected to a pair of accelerometers. The two comparator/latch outputs are connected to an AND gate. Each circuit compares the output from the accelerometer to a pre-defined threshold voltage and has self-latching positive feedback. When both comparators latch, the ASIC outputs a 1 V wakeup signal. The comparator thresholds are set by mirroring the bias current across resistors. In measurement, the two-channel ASIC requires only 5.25 nW while alert and 6.75 nW after wakeup.

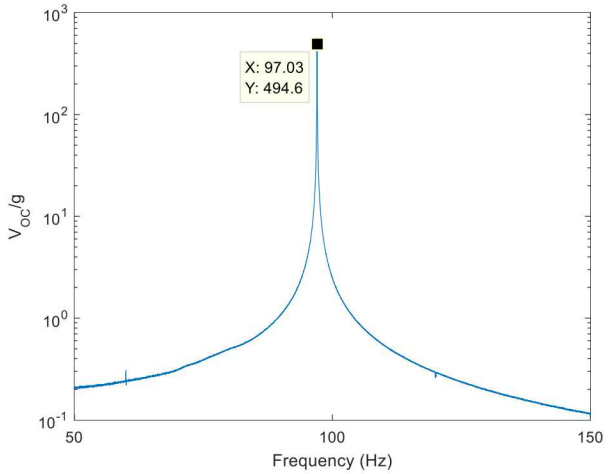

Figure 4 - Sample transfer function illustrating resonant MEMS accelerometer sensitivity.

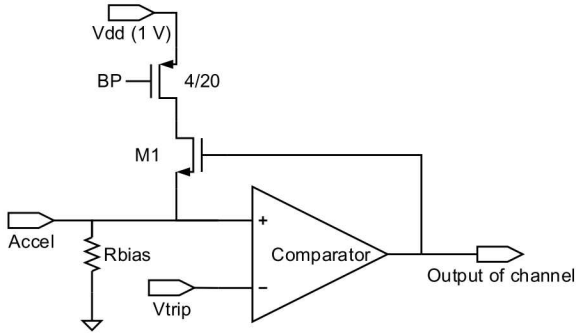

Figure 5 - CMOS comparator/latch unit.

Bias Cell

The bias cell, shown in Figure 6, generates a supply-independent 0.75 nA bias current, which is key to the lower power consumption in the ASIC. The bias cell consists of PMOS and NMOS current mirrors in a bootstrap configuration, with the current inversely proportional to the external bias resistor R_{BIAS}. The transistors are sized with very long channels (L = 20 µm) and biased in the subthreshold regime ($|V_{GS}| < |V_{TH}|$), which allows the supply voltage to be lowered to 1 V while retaining high drain resistance of the mirrors. R_{BIAS} is typically in the 100 MΩ range in order to set

nA-level currents. The "BP" and "BN" nodes are the gate voltages for P- and N-type current mirrors used throughout the ASIC. Additional mirrors (not shown) are provided in the bias cell to produce the trip voltages for the comparators by running 0.75 nA across an external resistor.

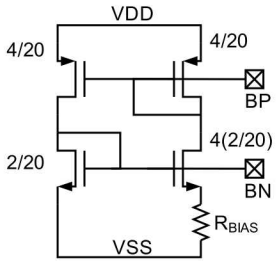

Figure 6 - Schematic of the bias cell with W/L noted. Startup circuit not shown.

Comparator

The comparator consists of a differential pair followed by a common-source stage. The two tail PMOS connect to "BP" from the bias cell such that about 0.75 nA flows through each branch, for a total of about 1.5 nW. The input is designed such that the comparator achieves gain while the inputs are biased near *VSS*. Figure 8 shows the input and output of a standalone comparator, showing successful operation at 200 Hz at a 100 mV trip point. The circuit experiences a slight offset at the input (it trips at about 10-25 mV higher than V_{trip}) due to both manufacturing mismatch and circuit bandwidth.

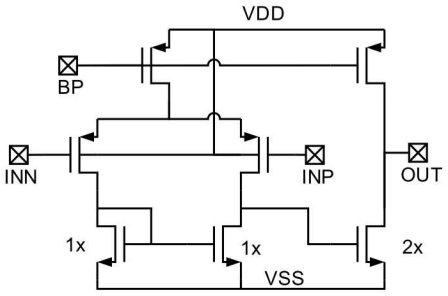

Figure 7 - Schematic of the comparator. The PMOS connected to BP have W/L = 4/20

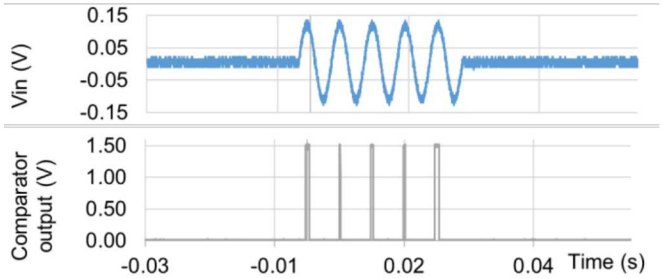

Figure 8 - Measured comparator input (top) and output (bottom) in for a 200 Hz 130 mV sinusoid compared to a 100 mV threshold.

Self-latching circuit

A positive feedback loop, wrapped around the comparator (Figure 5), performs latching. When the comparator output rises, transistor M1 turns on, allowing the 0.75 nA (current-starved by BP) to flow into the positive input node. Therefore, the power consumption of the self-latching comparator post-wakeup is 0.75 nW greater than pre-wakeup. To provide a bias to *VSS* for the input prior to latching but generate a latching voltage under positive feedback, R_{bias} is sized such that R_{bias}×0.75 nA > V_{trip} for values of V_{trip} we expect to use in the system. Figure 9 shows the measured input and output of the self-latched comparator as the input is dialed from about 124 mV to 125 mV at the time of the vertical cursor. The input rises as the feedback pumps current into the input (the input is a benchtop current source so it does not enforce the DC voltage level). The feedback takes several cycles to latch because the feedback current needs to charge parasitic capacitance at the positive input node.

INTEGRATED SYSTEM PERFORMANCE

The wakeup system (Figure 10) is realized by combining two MEMS resonant accelerometers with the ASIC on a custom printed circuit board (PCB), which we mounted on a shaker table to test performance. The power consumption is tabulated in Table 1.

A generator's vibration signature was targeted with characteristic frequencies of 80 and 160 Hz. Confusers from urban environment background noise and a truck signal were used to assess false positives. Figure 11 shows the results of the wakeup tests using the generator signal with (a) the 160 Hz filtered, (b) the 80 Hz signal filtered, and (c) the entire generator vibration profile present, as shown by the provided spectrum. We observe that when filtering either of the two targets below threshold, no wakeups occur. When the entire target signature is present a wakeup event occurs in each of the 30-second time blocks, returning to zero once a reset signal is provided.

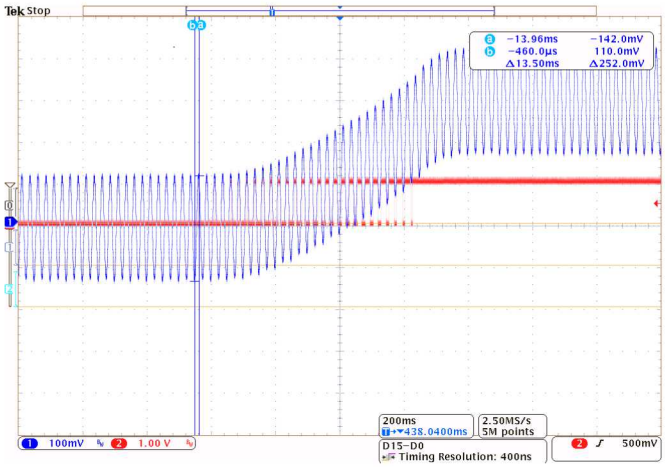

Figure 9 – Measured input (blue) and output (red) of the self-latched comparator for a 40 Hz 125 mV input compared to a 100 mV threshold. The vertical scale is 100 mV/div for the input and 1 V/div for the output; the horizontal scale is 200 ms/div. The input was dialed from about 124 mV to 125 mV around the time of the vertical cursors.

Table 1 - Power consumption of system components before and after wakeup. The total power consumption for a two-channel system therefore would be 5.25 nW before and 6.75 nW after wakeup.

Component	Before wakeup	After wakeup
Bias cell	1.5 nW	
Self-latched comparator	1.5 nW/channel	2.25 nW/channel
V_{trip} generation	0.75 nW shared by 2 channels	
AND logic	Below measurement floor	

To characterize the margin between false alarms and probability of detection, we set a threshold value and record when

the wakeup occurs under diminishing generator signal levels and increasing background levels, then we repeat this process for a higher threshold. Results are shown in Figure 12 (a) and (b). We observe margins between the generator and background noise of over 2000× with margins comparing the generator and truck of ~100×.

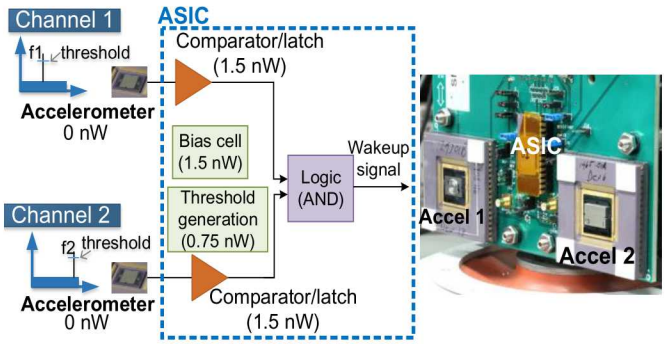

Figure 10 - Notional diagram and image of dual-channel wakeup system.

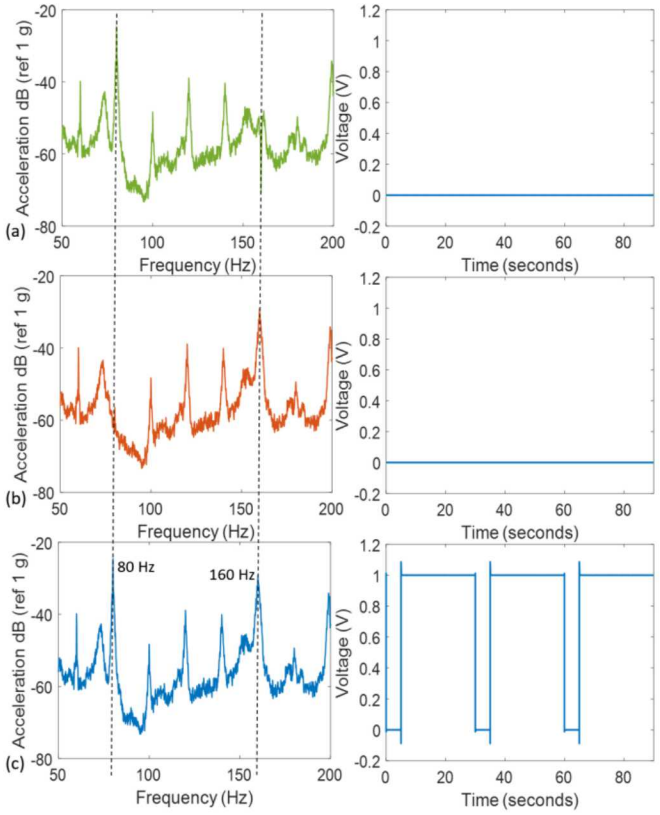

Figure 11 - Measured 2-channel wakeup results, (a) 160 Hz filtered, (b) 80 Hz filtered, (c) entire generator vibration profile. 5-second reset provided every 30 seconds.

SUMMARY AND CONCLUSIONS

We designed a near-zero power system to wake up to physical inputs from the environment employing two MEMS resonant accelerometers coupled to a CMOS ASIC. The MEMS accelerometers require zero power by utilizing piezoelectric AlN to transduce physical strain in the flexures to an electrical output signal. Accelerometers have demonstrated resonant frequencies as low as 43 Hz, sensitivities as large as 490 V/g, and quality factors upwards of 12,500.

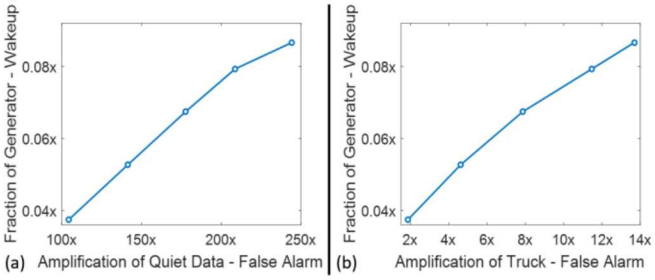

Figure 12 – Measured fraction of generator signal to trigger wakeup at various thresholds versus (a) amplification of background noise and (b) amplification of truck data (at the same comparator trip point) to trigger a false alarm.

The CMOS ASIC receives the electrical output from the accelerometers and compares them to the threshold with self-latching comparators. When the signal from both accelerometers exceeds the programmable threshold, the ASIC produces a 1 V wakeup. The CMOS ASIC requires only 5.25 nW of power before wakeup and 6.75 nW of power post-wakeup. The full system is able to selectively wakeup to a generator signal and successfully reject confusers in the form of urban background noise or a truck.

In future work, we intend to investigate shock and temperature hardness of this system needed for deployment.

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CONTACT

*B. Griffin, tel: +1-505-844-7370; bagriff@sandia.gov