SAND2017-12372PE

High Voltage Re-Grown GaN P-N Diodes Enabled by Defect and Doping Control

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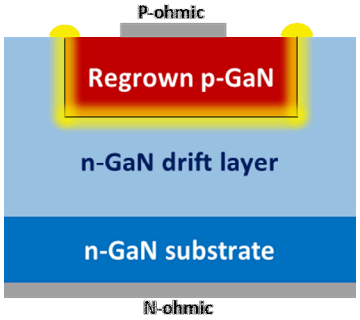
Overall goal and metrics

Project Goals

A) *Develop a mechanistic understand of selective area epitaxy (SAE) of p-GaN by MOVPE regrowth processes*

B) *Demonstrate a GaN PN diode formed by SAE of p-GaN that is electrically equivalent to "as grown" PN diodes*

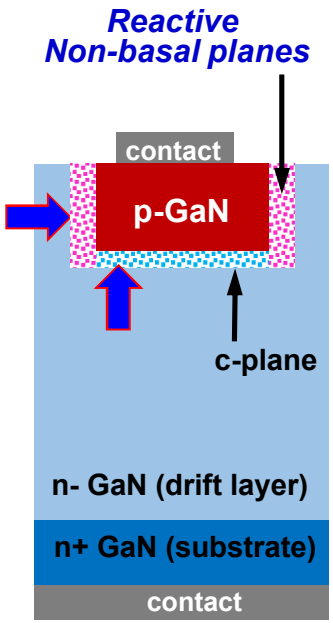
Key Performance Metrics



- Identify and reduce both impurity concentrations and point defects (traps) at the regrowth interface
- Quantitatively correlate mitigation strategies for identified impurities and defects with electrical properties of SAE□PN diodes
- Demonstrate SAE□PN diode with:
  - Reverse leakage < 1nA @ 600V
  - V_{br} > 1200V with avalanche capability

➡ Understanding of SAE provides the foundation for GaN-based vertical power transistors and diodes

Challenges in SAE



- *CL/PL*
- *DLOS/DLTS*
- *STEM/EDX*
- *EBIC/OBIC*
- *SIMS/XPS*
- *IV/CV*

Electrically active impurities

- Silicon, oxygen from common regrowth masks (SiN_x, SiO_2)
- Sidewalls of p-well (non-basal planes) have higher impurity incorporation rate than bottom of p-well

Point defects (e.g. vacancies)

- *Ex-situ* etch damage (ion bombardment) forming p-well
- Surface damage during start of regrowth

Concurrent regrowth on different crystal planes

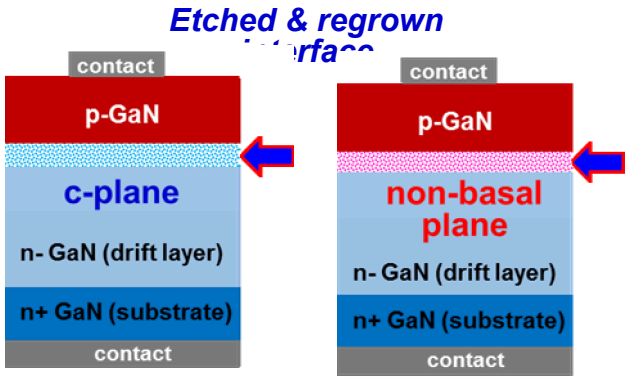
- Different growth conditions are optimal for different crystallographic planes
- Defect formation during regrowth at intersection of crystallographic planes in p-well

➡ Quantitatively measure energy level and concentrations of defects and impurities through defect spectroscopy

➡ Quantitatively correlate mitigation of specific defects and electrical performance of SAE-PN diodes

Year 1 & 2 Goals

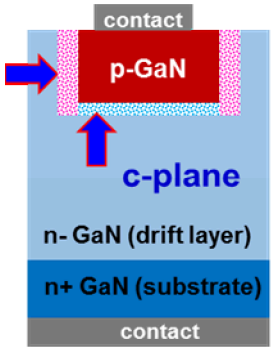
Year 1 Goals



- Characterize and control electrically active defects and impurities at the regrown interface
- Quantify diode characteristics and correlate with the nature of interfacial impurities and defects (trap)
- Demonstrate regrown PN diode on etched GaN drift layer (c-plane only) equivalent to as-grown diode

➡ *Reverse leakage < 1nA @ 600V, 200um dia.*

Year 2 Goals



- Establish mechanistic understanding of how crystallographic plane- and etch-mediated impurity and defect incorporation impacts SAE□PN diode performance.
- Demonstrate 1.2 kV diode by patterned regrowth of p-GaN

➡ *Reverse leakage < 1nA @ 600V, 200um dia.*

Team

Sandia National Laboratories

THE UNIVERSITY of NEW MEXICO

- **PI and POC: Dr. Andrew Armstrong (aarmstr@sandia.gov)**
- **Dr. Daniel Feezell (dfeezell@chtm.unm.edu)**

Team

Material Growth

- Andrew Allerman (SNL) ➡ Growth of c-plane diodes
- Dan Feezell (UNM) ➡ Grown of non-basal plane diodes

Fabrication & Characterization

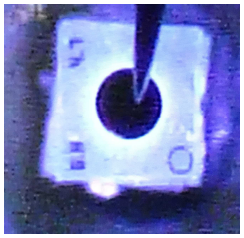
- Greg Pickrell (SNL) / Dan Feezell (UNM) ➡ ICP, PEC, wet chemical etching and diode fabrication
- Mary Crawford (SNL) ➡ PL, EL, CL, optical spectroscopy
- Andrew Armstrong (SNL) ➡ DLTS/DLOS, defect spectroscopy
- Alec Talin / Francois Leonard (SNL-CA), OBIC/EBIC,SPCM, CL electron beam characterization
- Bob Kaplar (SNL) ➡ High-voltage testing, electrical characterization
- Paul Kotula (SNL) ➡ STEM, EDX, EELS, advanced microanalysis
- SIMS (commercial), XPS (SNL)

Optical and defect spectroscopy

Optical Spectroscopy

(Mary Crawford, SNL)

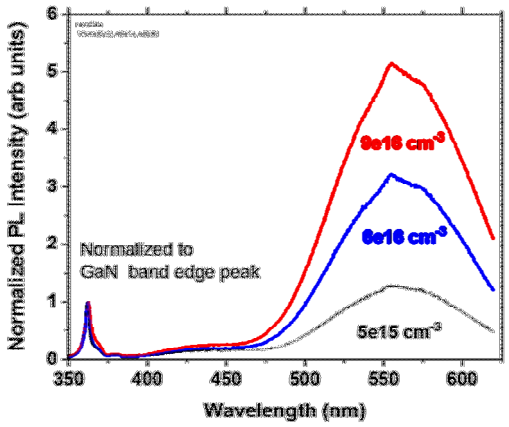
Electroluminescence probes operative junction defects under relevant bias conditions



Forward

Avalanche

Photoluminescence of Si doped GaN

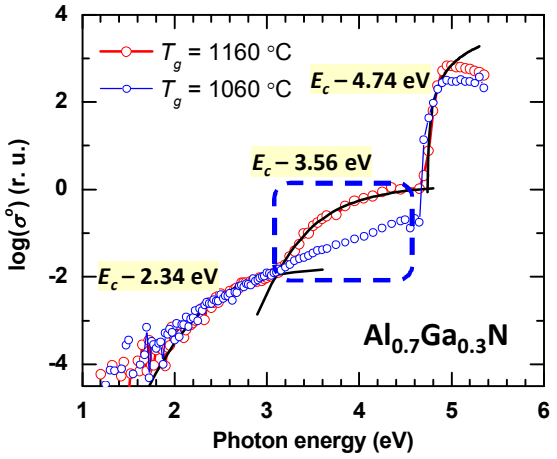


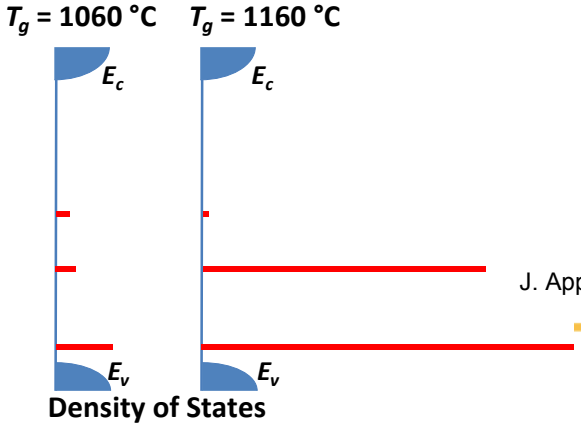
Dickerson *et al.*, IEEE TED **63**, 419 (2016)

Defect Spectroscopy

(Andrew Armstrong, SNL)

Quantify impact of growth and fabrication on junction defect energy level and density





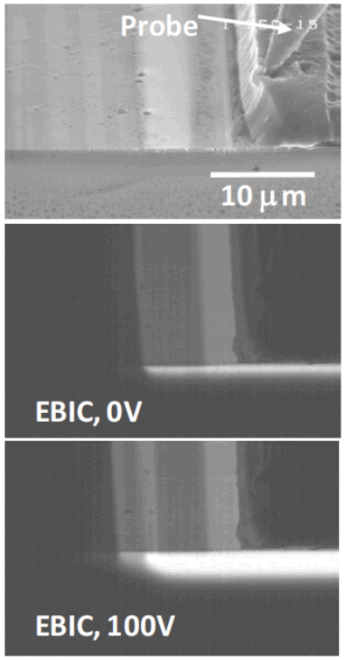
Armstrong *et. al.*, J. Appl. Phys. **117** (2015)

Electron Beam and Microanalysis

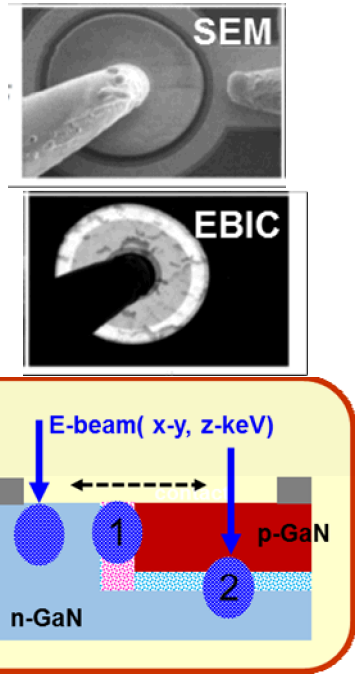
Electron Beam Characterization

(Alec Talin / Francois Leonard , SNL)

EBIC/CL correlates local leakage and defectivity at junction high voltage



EBIC of JTE of 30%AlGaN p/n diode (no implant)

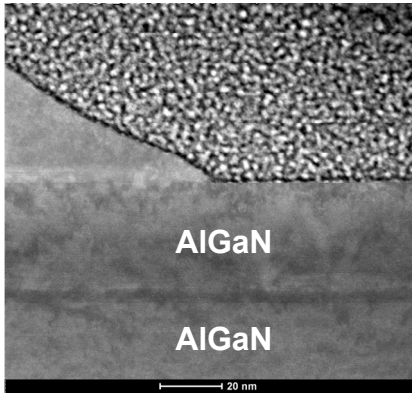


Advanced Microanalysis

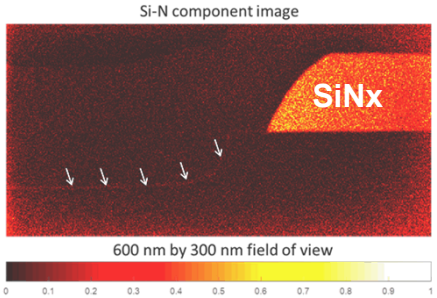
(Paul Kotula, SNL)

STEM techniques to assess dislocations, defects and impurities

STEM shows interface of AlGaN regrowth



EDX identifies Si at regrowth interface

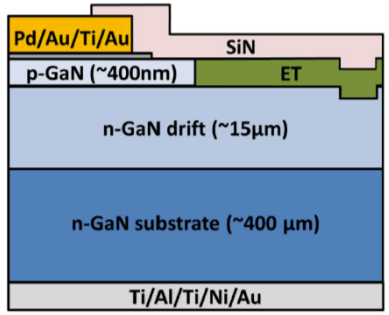


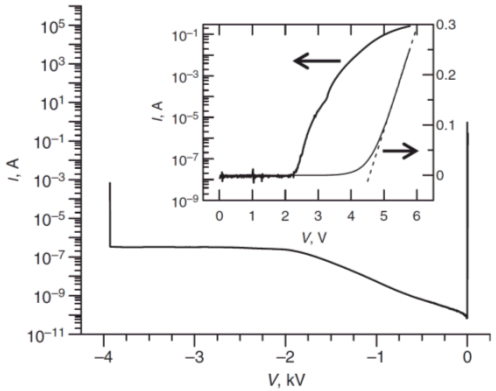
Device Fabrication and Testing

Diode Fabrication

(Greg Pickrell (SNL), Dan Feezell (UNM))

3.9 kV GaN diode demonstrated



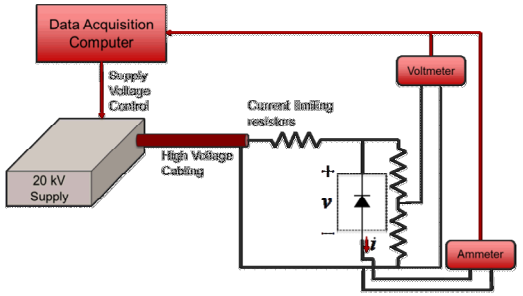


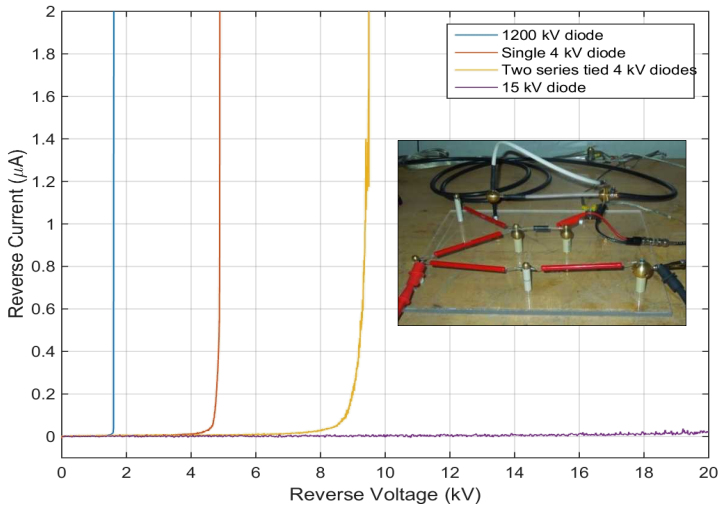
Armstrong et al. Electronics Letters **52**, 1170 (2016).

Electrical Characterization

(Bob Kaplar, SNL)

20 kV diode testbed





Technology-to-Market

Technology Transfer is an essential element of the Sandia Laboratories mission

Cooperative Research and Development Agreement (CRADA)

- **Collaborate and share the results of a jointly conducted research and development projects**
- **Partners can be domestic or foreign and generally come from industry, nonprofit organizations or academia.**

Commercial License Agreement

- **Sandia transfers intellectual property rights to a non-federal partner through a license agreement. Intellectual property includes patent applications, patents, copyrights, and trademarks**

Strategic Partnership Projects

- **Sandia performs work on a reimbursable basis for a non-federal entity from private industry, state/local government, nonprofits, or academia.**

Technology Transfer Ombuds

- **Assists in addressing issues related to technology partnerships, patents, and technology licensing.**

Center for Collaboration & Commercialization (C3)

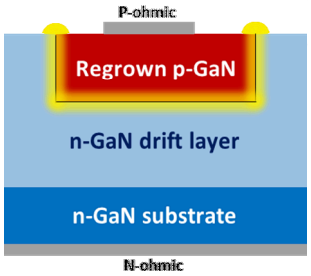
- **C3 serves as the "front door" to Sandia National Laboratories, providing access to the Labs where Sandians and their industrial, academic, and government partners can easily interact.**

http://www.sandia.gov/bus-ops/partnerships/index.html

Summary

Project Goals

- ***Develop a mechanistic understand of selective area epitaxy (SAE) of p-GaN by MOVPE regrowth processes***
- ***Demonstrate a useful SAE - GaN PN power diode***



Key Performance Metrics

- **Identify and reduce both impurity concentrations and point defects (traps) at the regrowth interface using a suite of electrical, optical, and structural characterization techniques**
- **Quantitatively correlate mitigation strategies for identified impurities and defects with electrical properties of SAE□PN diodes**
- **Demonstrate SAE□PN diode with:**
  - **Reverse leakage < 1nA @ 600V**
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