Effects of Charge-Induced Damage on SOI Wafers

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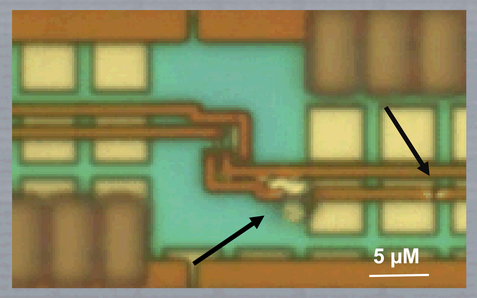
Problem: Systematic leakage in wafer-level test structures and packaged devices causing significant yield loss

BACKGROUND

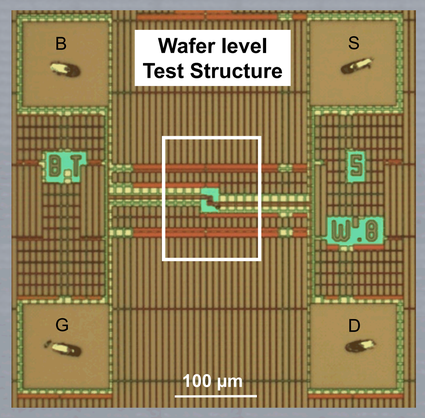
- Gate leakage in discrete test structure transistors at center of wafer
- Problem existed across multiple lots
- Die failures also indicated a wafer center failure trend only after packaging

Optical Inspection

- Quick way to localize/characterize damage
- Not all failing transistors had optical damage

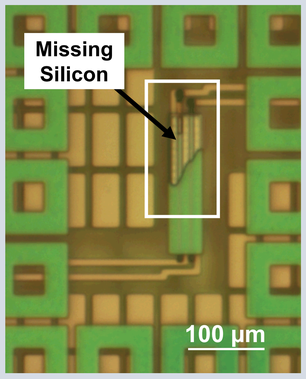


Cracking, metal extrusion on test structure

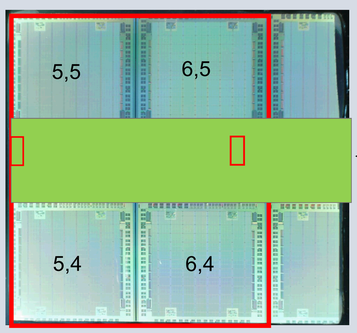


Backside Thinning

- Complete removal of the backside Si to the BOX layer
  - Technique involves lapping and final XeF_2 chemical etch
- Allows for quick optical screening of the backside of the wafer or die
- Advantages compared to FIB cross-sections include time and analysis of large areas
- Technique applied to both wafers and packaged die



Optical image of the backside of a discrete transistor (wafer level) with the substrate Si removed. Etched silicon indicates the presence of a BOX defect.

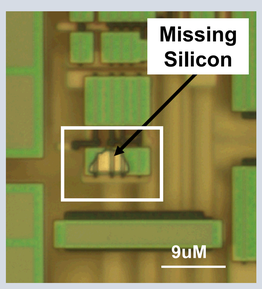


Test structure strip

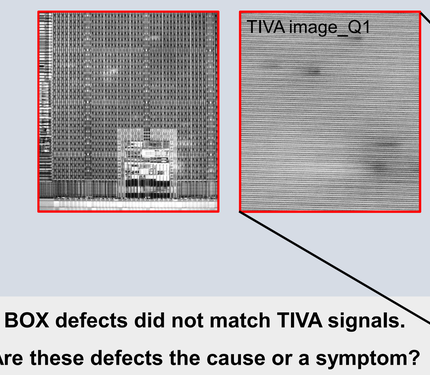
Optical image through the backside of a wafer post thinning

Backside optical screen for BOX defects

- Defects provide a pathway through the BOX layer where the chemical etchant attacks the Si island
- Islands missing silicon indicate the presence of BOX defects



Chemical etch highlighting the presence of a BOX defect



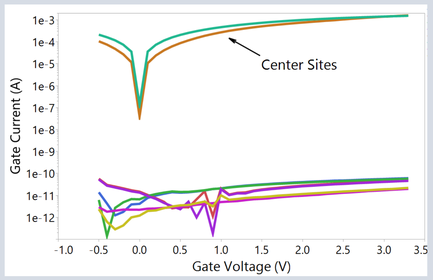
BOX defects did not match TIVA signals.

Are these defects the cause or a symptom?

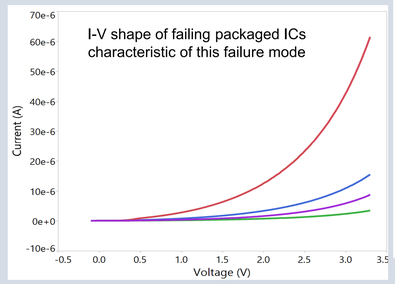
RESULTS

Electrical

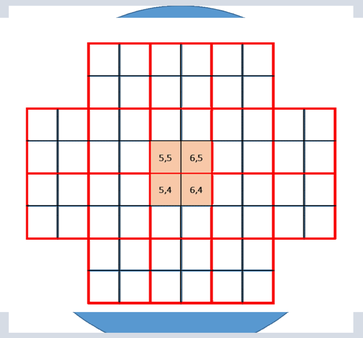
- Wafer center discrete transistors consistently failed > 1 mA gate current at 3.3 V (~nA nominal)
- Packaged die from wafer center positions (as shown in schematic) also indicated leakage-type failures that ranged from µA to mA
- Although absolute failing current varied, characteristic shape of IV curve emerged



Gate leakage from die sites across the wafer; center sites consistently fail



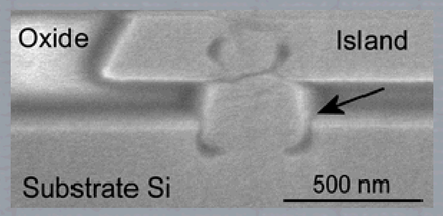
IDDS I-V sweeps of packaged failing ICs

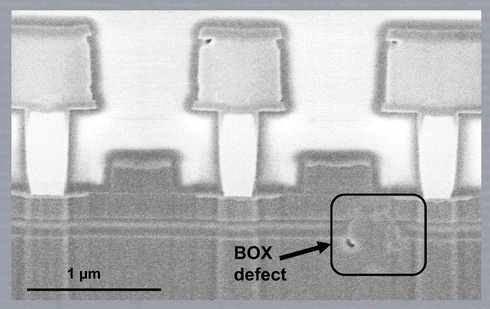


Wafer schematic of x,y die locations

FIB Cross section

- Silicon filament observed between Si island and substrate (BOX defect)
- Provides electrical connection between island to substrate
- Present in all failing discrete transistors



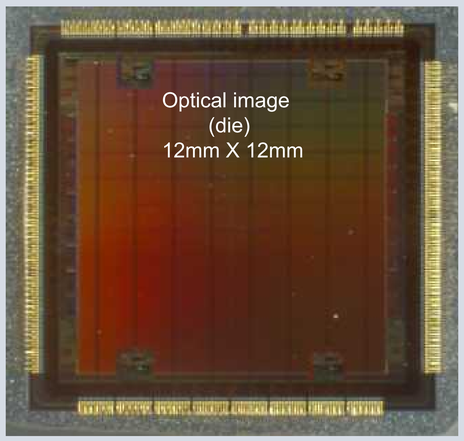


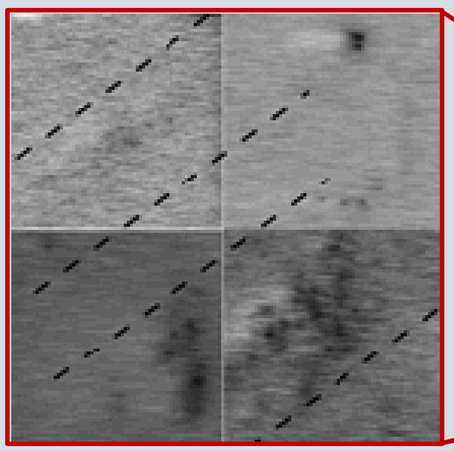
Cross-section through discrete transistors with optical damage

Laser-based Techniques: Thermally-Induced Voltage Alteration (TIVA)

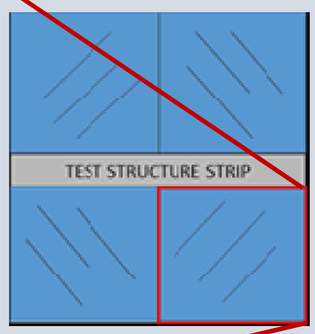
Characteristic TIVA (1340 nm) pattern observed in failing packaged parts

- The TIVA signals were directional with respect to the center of wafer. Depending on the die location of the packaged parts, the vector would change as depicted in the graphic
- The TIVA signals were consistently diffuse and dark





Schematic of four center die showing TIVA signal directionality



Characteristic TIVA pattern from packaged IC showing diffuse, dark, and directional signals

CONCLUSIONS

The cause of the leakage in both the test structures and packaged parts was found to be charge-induced damage from a high-velocity DI water spray nozzle within the chemical mechanical planarization tool.

- During this step, the spray nozzle is positioned at the wafer center during a high-speed rotational rinse.
- The charge-induced damage manifested itself as breakdown behaviors (BOX defects and suspected gate oxide defects) between the high potential surface of the wafer and the grounded backside. It is believed that the directional TIVA signals were due to gate oxide defects.

The characterization of the IV sweeps and TIVA imaging trends enabled quick identification of another process generating charge-induced damage post fab. Quick resolution of the issue mitigated another significant yield loss.

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