Development of Discrete Components

Kansas City Division

R. J. Brown

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Final Report

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DEVELOPMENT OF DISCRETE COMPONENTS

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Abstract

AlliedSignal, Inc., Kansas City Division, the production agency, was provided with funding to maintain the capability to procure discrete components for various applications. A development project was undertaken to procure transistor die from one supplier for assembly into finished components by a different supplier. These components would be "SA-equivalent" with appropriate preconditioning, testing, and certification. The methodologies developed herein go far to ensure the future availability of discrete components.

Summary

During periods of reduced military procurement, semiconductor suppliers who traditionally maintained production capacity for military products have converted significant portions of this capacity to commercial use. In order to maintain the capability to procure components, a project was undertaken to examine the feasibility of third-party packaging for Sandia apparatus (SA) devices.

Assembly concerns regarding bond wire and die attach integrity were eliminated as a result of this project. Initial radiation testing, however, revealed that the packaging supplier's current small-signal die is significantly less tolerant than that of the previous manufacturer.

With the assembly concerns eliminated, the result has been a highly agile packaging capability which goes far to ensure the future availability of discrete components fabricated using previously-qualified die.

Future work, in conjunction with Sandia Laboratories and the packaging supplier, will likely be focused on improving the radiation tolerance of both the supplier's small-signal and power die.

Discussion

Scope and Purpose

This project, *Development of Discrete Components*, was initiated due to continuing decline in the number of suppliers qualified to manufacture SA discrete transistor components. Specific business policy changes by suppliers directly affecting the procurement of SA transistors included 1) standardization of dual-use (joint commercial and military) specifications for component lead material which allowed solder dip over defect-prone electroless nickel plating; 2) reluctance to accept source-controlled drawings (SCDs); 3) elimination of "sunset technologies" devices through "life-of-type buys;" and 4) introduction of plastic-encapsulated devices as replacements for hermetic military products.

These directions posed significant concerns due to the variety of weapon systems in the stockpile built using SA devices. In addition, the need for replacement devices was being driven by ongoing retrofit and telemetry programs.

As a result, this project was initiated with the intent of qualifying a third-party packaging facility to manufacture SA transistors. The supplier previously had wafer fabrication capability and was approved by Defense Electronics Supply Center (DESC) to supply Joint Army-Navy (JAN) product. This project was designed to be the vehicle whereby this supplier could eventually build SA devices using the supplier's own die.

This nontraditional approach posed increased risk for both the user [AlliedSignal Inc., Kansas City Division (ASKCD)] and the third-party packaging supplier. First, the user must ensure that high-quality die is available. Second, the packaging supplier must often develop alternate processes for wire bonding and die attach to accommodate foreign die. Third, the user must realize that third-party packaging is an effective but temporary solution. Suppliers who have exited the military semiconductor business generally loose all expertise in the production of radiation-tolerant and radiation-hardened devices.

Since both Sandia Laboratories and ASKCD had significant prior experience with qualified die, further investigations of the die itself were not required. The remaining areas of risk involved in the packaging of die at a third-party supplier were determined to be:

- wire bond integrity,
- die attach integrity, and
- radiation margin of current die.

The assembly-related results obtained from these investigations were incorporated into product and assembly specifications used in actual assembly of SA devices. Nonproduction activities are reported herein.

Activity

Wire Bond Integrity

The supplier's initial focus was on header characteristics. The gold plating typically used on an SA device was thinner than that produced by the supplier's header source as shown in Table 1.

Table 1. Header Gold Thickness Comparison

Location	Supplier Source Plating Thickness (microns)	Typical SA Device Plating Thickness (microns)	Thickness Ratio (Supplier: Typical SA)
Header	*3.52*	*2.60*	*1.35:1*
Post	*3.20*	*2.08*	*1.54:1*
Leads	*5.28*	*3.08*	*1.71:1*

An accelerated aging evaluation was conducted to determine the severity of purple plague formation on devices assembled with headers containing relatively thick gold. The expected outcome was that thick gold under the aluminum wire bond would accelerate the formation of gold-aluminum intermetallics at elevated temperatures.

It was considered that activation energies above 150°C might be significantly different from those at temperatures above 300°C. An acceleration aging temperature of 200°C was selected to provide margin over the 150°C HTRB temperature normally seen during preconditioning. The intent was to not introduce temperature-dependent activation energy concerns into the evaluation.

Three approaches were used to conduct this evaluation: nondestructive electrical contact resistance, destructive bond pull, and final visual.

Electrical Contact Resistance Testing

Backside collector die attach construction places both base and emitter wires in contact with the posts. Test equipment was programmed to pass a constant base current through the base-emitter junction during which time V_{BE} was measured. The V_{BE} measurement reflects the lumped resistance of the base-emitter diode bulk, bond wire, and post contact. The assumption was made that at sufficiently high currents, the effects of intermetallic formation could be seen as an increase in contact resistance manifested by proportional increases in V_{BE}.

A sample of ten devices packaged without preconditioning was first tested to verify conformance to room temperature electrical specifications. Eight of the ten devices, serial numbers 1-8, were baked in an oven at 200°C for four hours. Following a 30-minute minimum cool-down period to room temperature, each device was subjected to base-emitter current pulses of 0.2, 0.5, and 1.0 amperes. Reverse leakage current (I_{EBO}) measurements were performed. Results were compared pre- and post-pulse to verify that the junction had not been damaged due to the current pulse. Two devices, serial numbers 9 and 10, were used as control devices and not exposed to elevated temperature.

The bake cycle was repeated an additional six times for a total exposure of 28 hours at 200°C. The experimental activation energy for gold-aluminum intermetallic formation is in the vicinity of 1.0eV. Using this estimated figure, each 4-hour bake would represent approximately 5 years of continuous field

operation at a field junction temperature of 70°C.

Figures 1, 2, and 3 show maximum, mean, and minimum values of V_{BE} based on measurements of the eight samples over the 28-hour period.

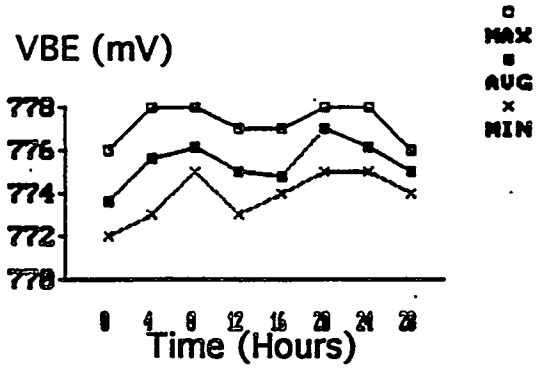

Figure 1. V_{BE} vs. Cumulative Hours of Aging at 200°C ($I_B = I_E = 0.2$ Amp)

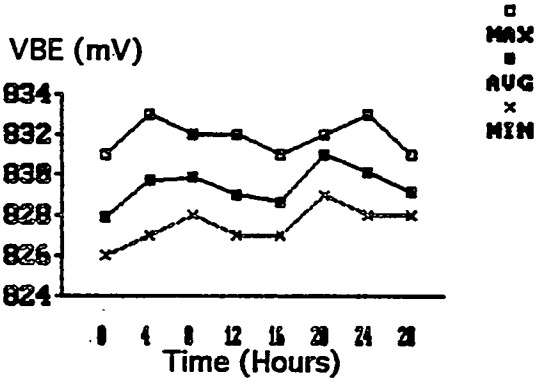

Figure 2. V_{BE} vs. Cumulative Hours of Aging at 200°C ($I_B = I_E = 0.5$ Amp)

Results from pulses of 0.2 and 0.5 ampere, Figures 1 and 2 respectively, are similar. A distinction can seen in Figure 3 for the 1.0-ampere pulse. The sample minimum value of V_{BE} increased linearly for the first 8 hours and then stabilized.

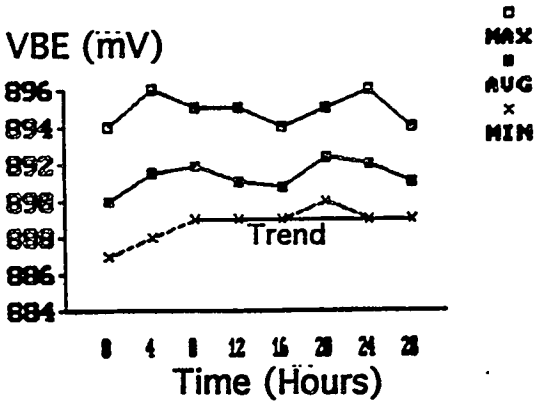

Figure 3. V_{BE} vs. Cumulative Hours of Aging at 200°C ($I_B = I_E = 1.0$ Amp)

Bond Pull Strength Testing

Post-aging bond pull strength was tested in accordance with MIL-STD-750, Method 2037. The intent was to pull each wire to destruction with particular attention paid to any separations which occurred at the posts. These results are shown in Table 2.

Table 2. Post-Aging Bond Pull Strength[a]

Serial Number	Wire #1 Strength (grams)	Wire #2 Strength (grams)
1	243	243
2	242	243
3	242	242
4	242	242
5	243	243
6	242	242
7	244	242
8	245	244
9 (Control)	244	242
10 (Control)	119[b]	121[b]

NOTES:

a. No separations occurred at the post.

b. These samples were the first tested and a 100-gram beam was used. The minimum post-seal pull strength for 10-mil wire in accordance with Mil-Std-750, Method 2037, is 80 grams. A larger beam was used on the remaining samples to improve accuracy. Due to equipment limitations, actual readings may be beyond those recorded.

Die Attach Integrity

Thermal impedance (commonly referred to as "Sage testing") is a nondestructive die attach evaluation technique. For bipolar transistors, $V_{BE}(on)$ is the temperature-sensitive parameter. The $V_{BE}(on)$ is initially measured on a sample of devices over a temperature range to establish correlation coefficients.

All measurements are performed on an independent semiconductor tester programmed to a low duty cycle at the measuring current to minimize self-heating during correlation. Parametric $V_{BE}(on)$ variation between individual devices from the same wafer or wafer lot is typically insignificant. The *average* value of $V_{BE}(on)$ when plotted on linear graph paper against temperature (Figure 4) is a straight line whose slope is the temperature coefficient for the device at measuring current I_M.

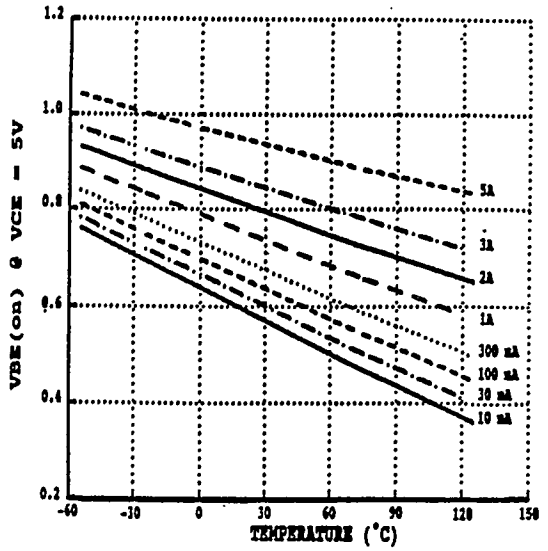

Figure 4. V_{BE} vs. Temperature for Increments of Collector Current, I_M

Through use of thermal impedance testing, ΔV_{BE} can be correlated to both transient and steady state heat flow characteristics. These characteristics are an inherent signature of die adhesion, assembly materials, and heat transfer properties of a given die in a given package.

During thermal impedance testing, the device is turned on by I_M, maintained on by heating current I_H for t_H seconds, turned off, and turned on for the final time by I_M. This technique is further defined by Table 3.

Table 3. Thermal Impedance Test Sequence

Time	Event	Effect	Measure-ment or Compu-tation
t_0		Device junction is at room ambient	None
t_1	Apply I_M		Measure $V_{BE}(on)_1$ at near ambient
t_2	Apply I_H for t_H seconds ($I_H >> I_M$)	Junction temperature increases as a function of I_H and t_H	Measure on voltage at I_H
t_3	Drop I_H and reverse bias junction	Quit heating and remove excess charge from junction	None
t_4	Wait for several micro-seconds	Allow transients to decay before junction starts to cool	None
t_5	Reapply I_M	Device junction temperature a function of heat retained in package	Measure $V_{BE}(on)_2$ at elevated temperature and compute $\Delta V_{BE}(on) = \lvert V_{BE}(on)_1 - V_{BE}(on)_2 \rvert$

To make optimal use of thermal impedance testing, heating time (t_H) must be adjusted to reflect the thermal time constant of the die attach region. This heat transfer region and others of interest are depicted in Figure 5.

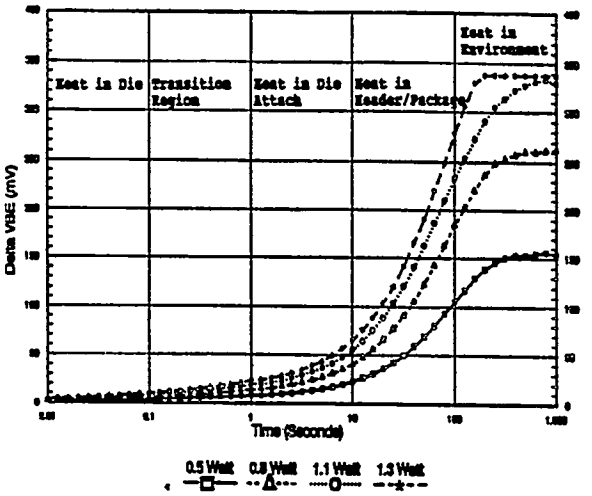

Figure 5. ΔV_{BE} vs. Log_{10} (Time) for Varying Wattage (V_{CE} x I_H) Input Levels

Of note, the time axis of Figure 5 is plotted on a logarithmic scale. This is standard practice for representation of the heat transfer characteristic. The problem, however, is one of determining where the transition region ends and the die attach region begins.

One graphical solution is to re-plot both axes of Figure 5 on linear scales as shown in Figure 6. Hence, a distinction can be made via the logarithmic die heat transfer characteristic giving way to the piece-wise linear die attach transition characteristic. In this case, a t_H of 1.5 seconds would be recommended to detect any potential die attach concern. Testing at a power input of 1.0 watt or greater would be adequate to provide the needed resolution for pass-fail determination by the thermal impedance tester.

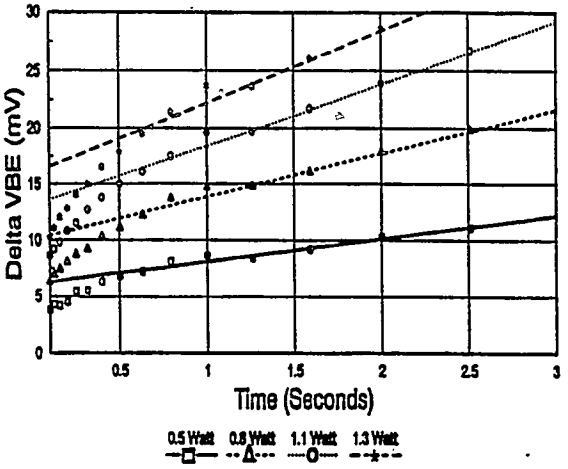

Figure 6. ΔV_{BE} vs. Time for Varying Wattage (V_{CE} x I_H) Input Levels

Radiation Margin of Current Devices

In order to establish radiation margin of the supplier's die, radiation testing was performed in the final phase of this project. Representative device types were selected as shown in Table 4.

Table 4. Current Supplier Die Types Selected for Radiation Testing

Type	Polarity	Category
2N2484	NPN	Small-signal
2N2907A	PNP	Small-signal
2N5339	NPN	Power

Initial electrical measurements were performed on groups of 50 devices from each devices from each device type. Samples for radiation testing were allocated as shown in Table 5.

Table 5. Allocation of Device Samples for Radiation Testing (n=50)

Radiation Test/ Controls/Spares	Quantity
Neutron	20
Total dose gamma	5
Photocurrent	5
Controls	10
Spares	10

Neutron Testing

Neutron testing on the three device types was performed at Sandia National Laboratories' SPR III facility in Albuquerque, New Mexico. As with all radiation testing, results obtained are dependent on both the facility and established test procedures for that facility. The devices received pre-radiation electrical tests at +25°C, +125°C and -55°C. Post-radiation electrical testing was performed in the sequence of +25°C, -55°C and +125°C to preclude temperature-related annealing effects. The devices were irradiated to a target fluence of 1E14 neutrons/(cm^2s), E > 1 MeV silicon equivalent. The actual dosage received was 10.9E13 (1.09E14).

The most significant number of electrical limit failures occurred post-neutron. *All three current device types failed the maximum V_{CE}(sat) limit.* Of the three devices tested, the 2N2907A type manufactured by the previous supplier had been fully characterized by Sandia Laboratories for post-neutron V_{CE}(sat) performance at levels from 8.9E12 to 1.9E14.

Figure 7 shows the pre- and post-neutron V_{CE}(sat) versus collector current characteristic of the previous manufacturer's 2N2907A type. The curve at 9.7E13 or approximately 1E14 was used to spot-compare post-neutron V_{CE}(sat) performance to that of the current supplier's 2N2907A type depicted in Figure 8.

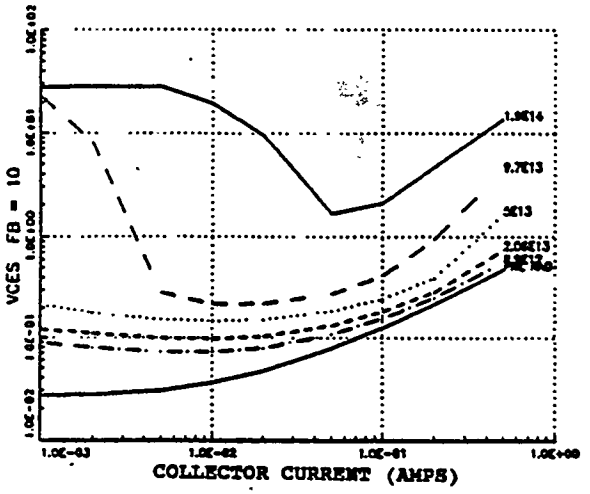

Figure 7. Pre- and Post-Neutron V_{CE}(sat) Performance of the Previous 2N2907A Type

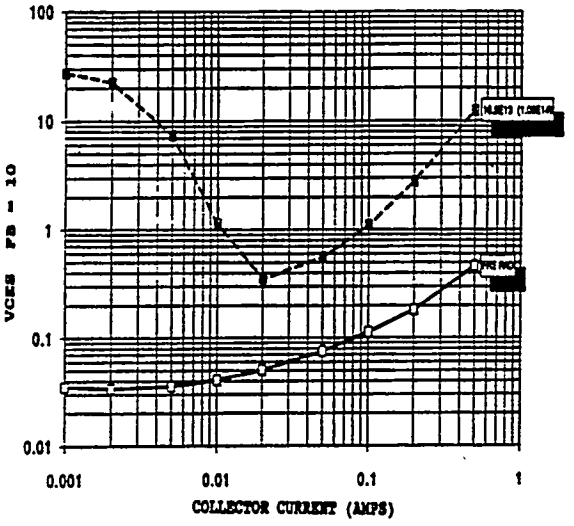

Figure 8. Pre- and Post-Neutron V_{CE}(sat) Performance of the Current 2N2907 Type

The consistency of these results provided additional assurance that no significant testing anomalies had occurred during or following neutron exposure.

The post-neutron DC current gain (h_{FE}) characteristics of all three devices were then plotted against type data available from Sandia. Obsolete devices, devices from the previous supplier as well the current devices, are compared in the graphs at ambient, hot, and cold as shown in Appendices A, B, and C.

Total Dose Testing

The three device types were irradiated at a target total dose of 1000 krads (Si) at Alliance Technologies' Gamma Cell (Cobalt-60) in Albuquerque. Dosimetry was measured with multiple thermoluminescence dosimeters (TLDs) during three shots of 333.33 krads each. The test strategy was to achieve an acceptable accuracy/cost tradeoff by limiting the number of shots. Dosimetry readings taken by Sandia's Dosimetry Laboratory were higher than the levels targeted by Alliance Technologies. TLDs, however, may be inaccurate for individual shots exceeding 100 krads. The average TLD readings were 355, 486, and 513 krads per shot for a total dose of 1,354 krads.

The 2N2484 type devices showed limit failures of V_{CE}(sat) during post-gamma electrical testing. The other two device types showed no failures.

Photocurrent Testing

The devices were transported by Alliance Technologies to Boeing's Radiation Effects Laboratory in Seattle, Washington. A linear accelerator (LINAC) was used to expose the devices to target dose rate of 1E8 rads/s (Si) at a 4-μs pulse width. Dosimetry readings indicated that the actual dose was acceptably close to the targeted dose rate.

Post-LINAC electrical testing showed no electrical failures on any of the three device types.

Accomplishments

Initial concerns raised by the current supplier regarding header gold plating thickness for wire bond integrity were shown not to be of significance. High temperature aging, post-aging bond pull testing, and visual examinations based on representative samples yielded acceptable results.

Thermal impedance test methods were improved to focus exclusively on the die attach region. As this method is nondestructive, 100% thermal impedance to be gradually replaced by sampled process monitors could be established as part of the supplier's assembly process control. Incorporation of thermal impedance testing would significantly reduce the risk of die attach concerns raised by utilization of foreign die.

Radiation testing of the current types revealed that the 2N2484 and 2N2907A device types are more susceptible to h_{FE} (gain) degradation when compared to previous device types at levels near 1E14. The 2N5339 may have sufficient tolerance for tactical applications. It is useless (peak h_{FE} <2 at -55°C) for strategic applications at levels of 1E14 or greater.

Appendix A

2N2484 Type Post-Neutron h_{FE} Performance at 25°C/125°C/-55°C

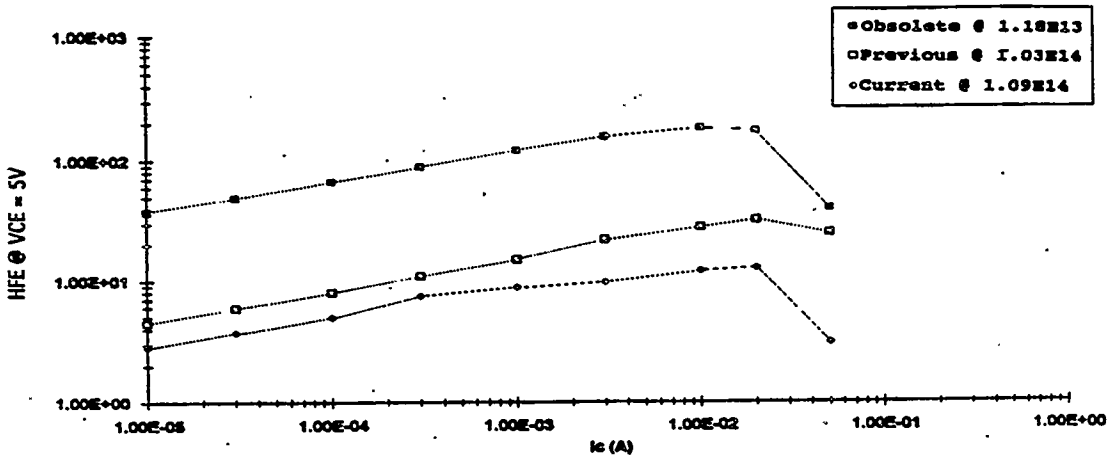

Figure A-1. 2N2484 Type Post-Neutron h_{FE} Performance at +25°C

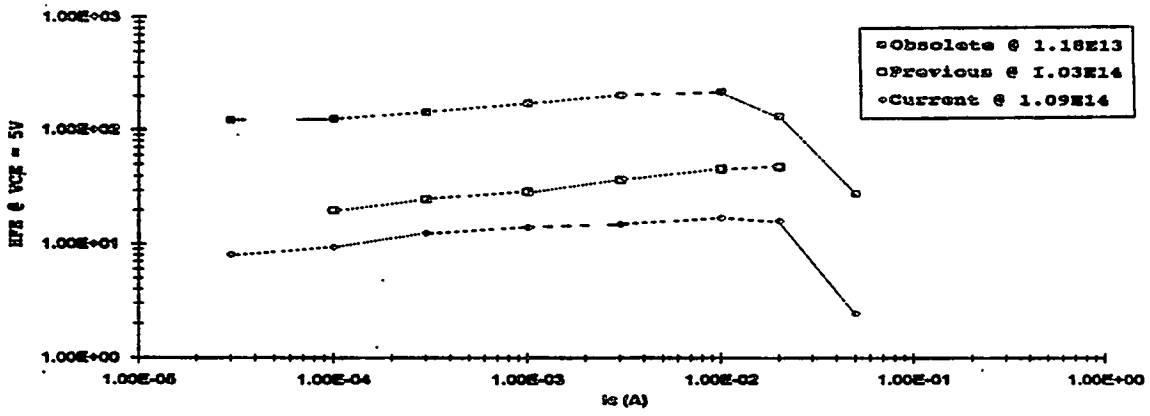

Figure A-2. 2N2484 Type Post-Neutron h_{FE} Performance at +125°C

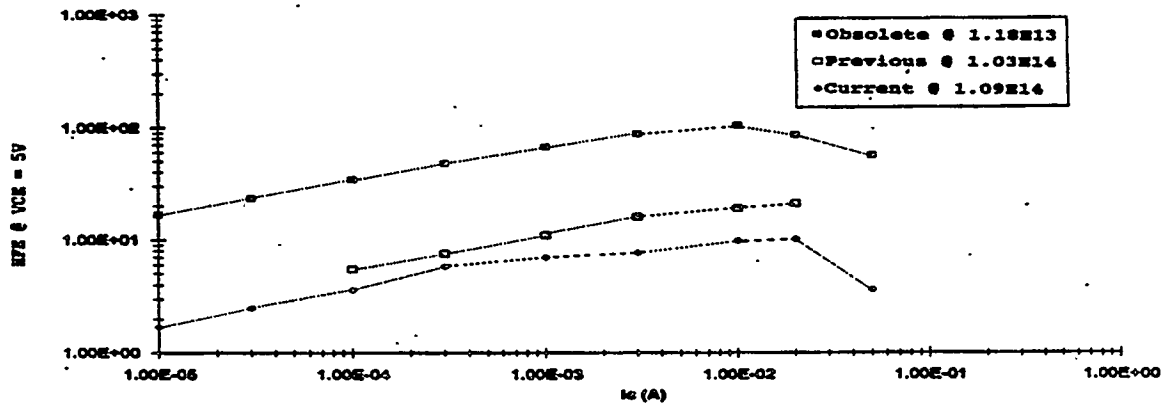

Figure A-3. 2N2484 Type Post-Neutron h_{FE} Performance at -55°C

Appendix B

2N2907A Type Post-Neutron h_{FE} Performance at 25°C/125°C/-55°C

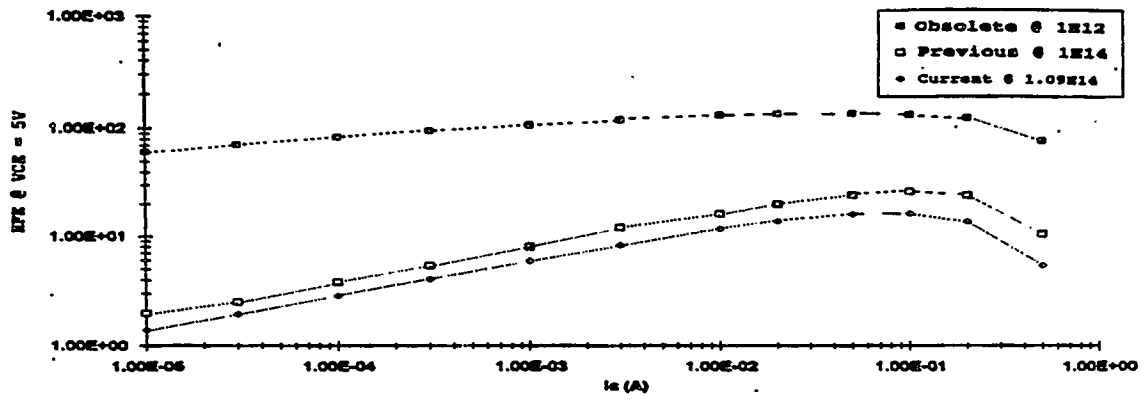

Figure B-1. 2N2907A Type Post-Neutron h_{FE} Performance at +25°C

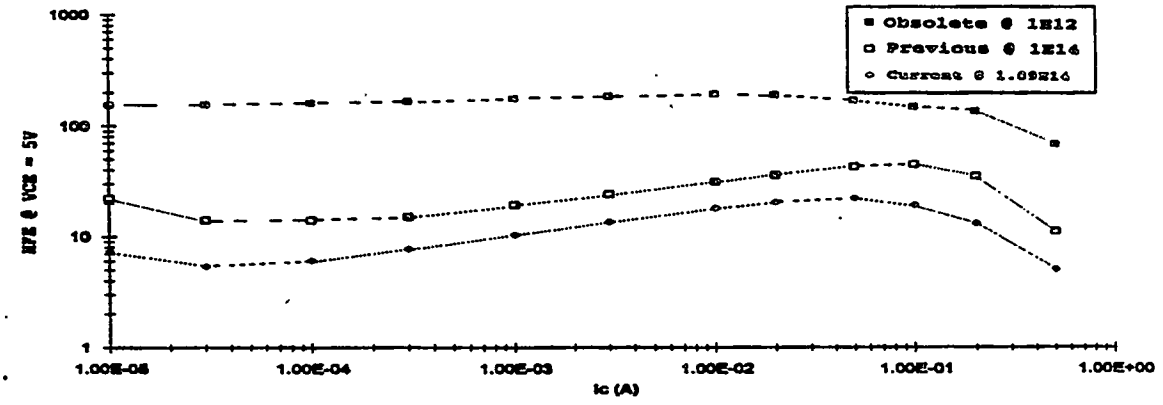

Figure B-2. 2N2907A Type Post-Neutron h_{FE} Performance at +125°C

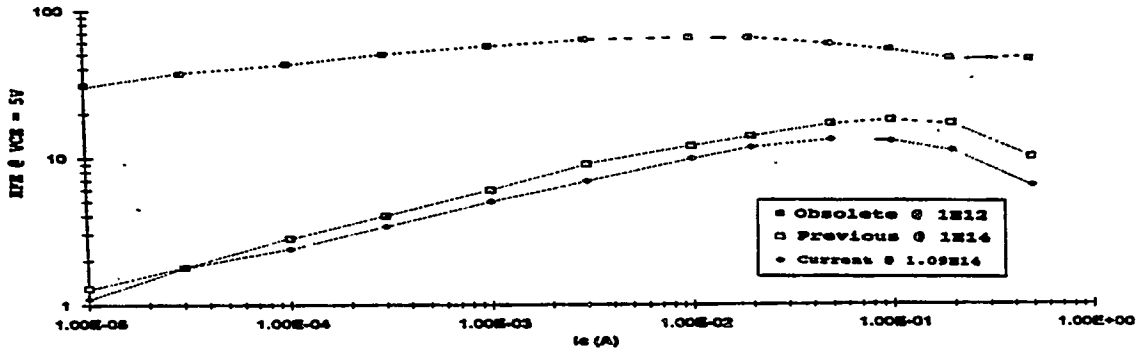

Figure B-3. 2N2907A Type Post-Neutron h_{FE} Performance at -55°C

Appendix C

2N5339 Type Post-Neutron h_{FE} Performance at 25°C/125°C/-55°C

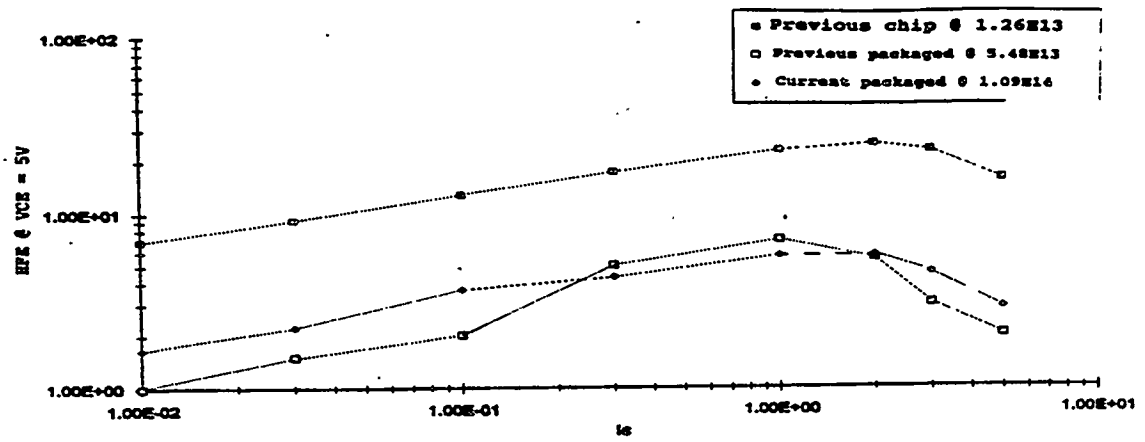

Figure C-1. 2N5339 Type Post-Neutron h_{FE} Performance at +25°C

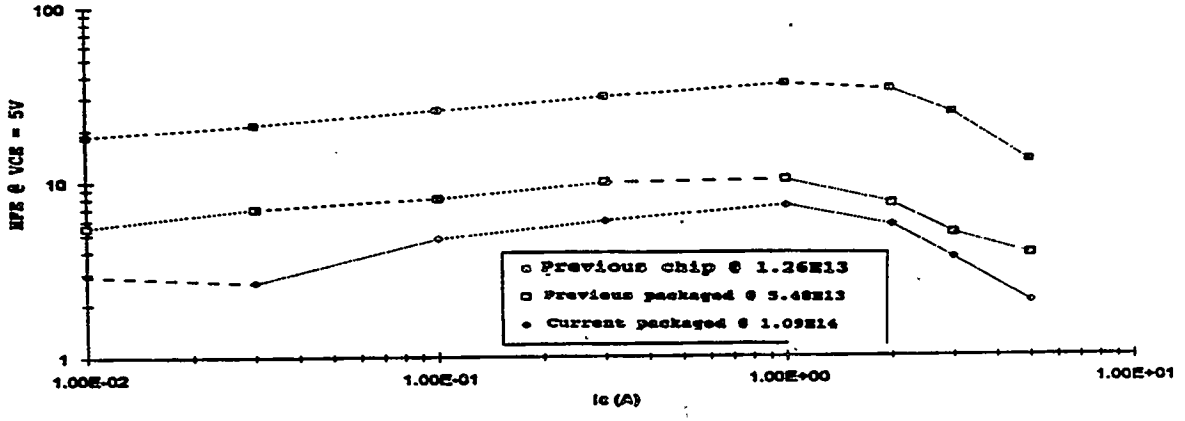

Figure C-2. 2N5339 Type Post-Neutron h_{FE} Performance at +125°C

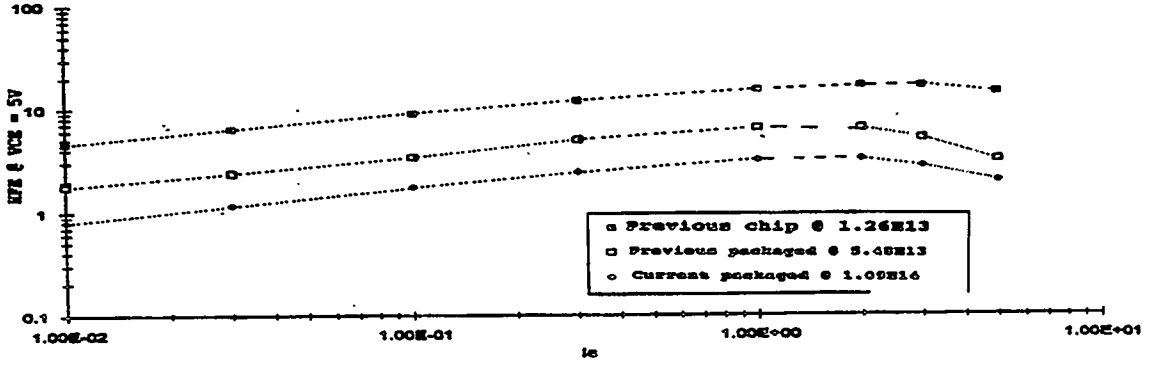

Figure C-3. 2N5339 Type Post-Neutron h_{FE} Performance at -55°C