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The Mechanical Performance of Sn-Pb Solder Joints on LTCC Substrates

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Introduction

- The development and operational sustainment of down hole **renewable (geothermal)** and **non-renewable (fossil fuel)** energy resources will be challenged by increasingly higher costs factors:

  - Site preparation ($B)
  - Loss of site operations ($M/day)
  - Liability – environmental restoration ($B)

Courtesy of Dept. of Energy

Courtesy of Dept. of Energy

Courtesy of NASA

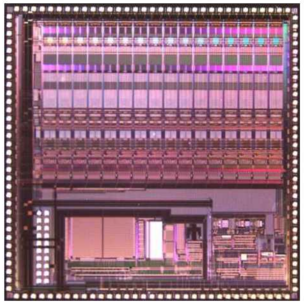
Introduction

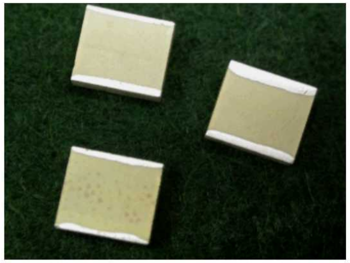
- Downhole sensor electronics can significantly improve the efficiency and reliability of well exploration and production.
- Oil, gas, and geothermal wells present some of the harshest service conditions for electrical equipment.
    - **Temperatures:** 300°C continuous; 350°C peak
    - **Pressures:** 15,000 to 30,000 psi
    - **Vibration:** PDS (g^2/Hz), 0.01 – 0.1 (0.6 – 3 kHz)
    - **Corrosion:** H_2S, H_2, brine, superheated steam.

Courtesy of Sandia National Labs.

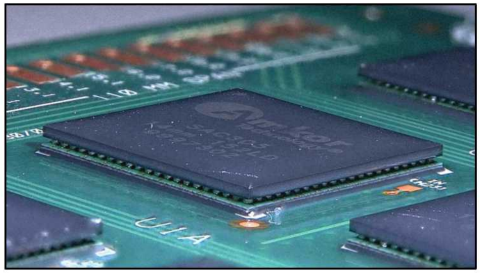
Introduction

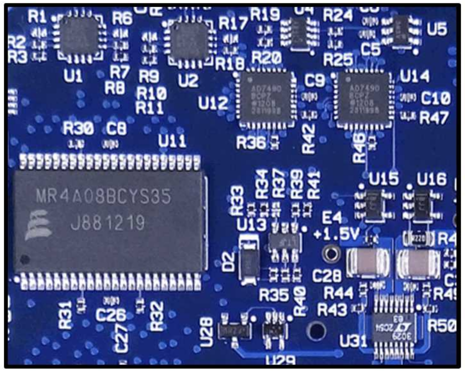
- Advances have been made in the development of high temperature, electronic components.
  - Increased functionality enhances the information flow from the hole to the field engineer.

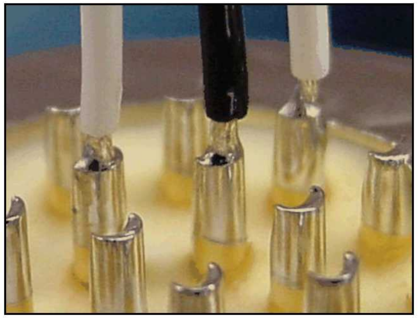




- However, the benefits to well production can only be realized with similar advances in electronic packaging technology.



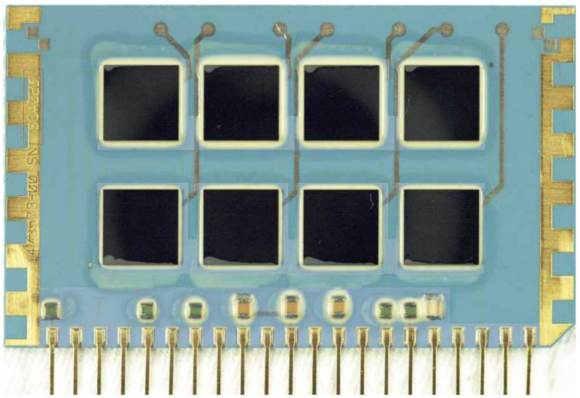


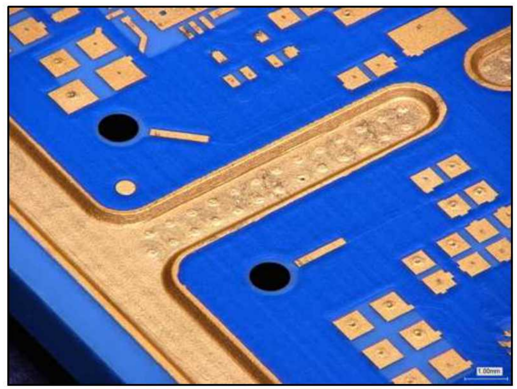


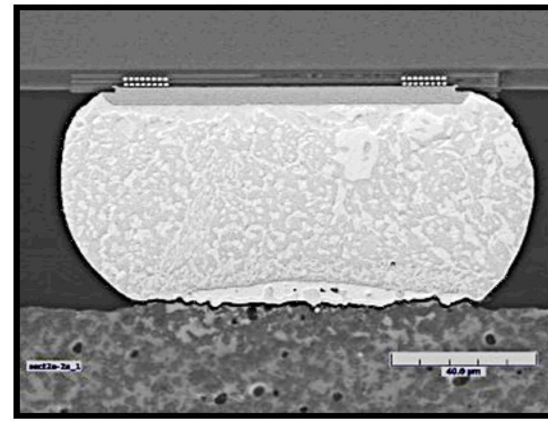
Organic printed circuit boards are approaching their mechanical and temperature limitations vis-a-vis downhole environments.

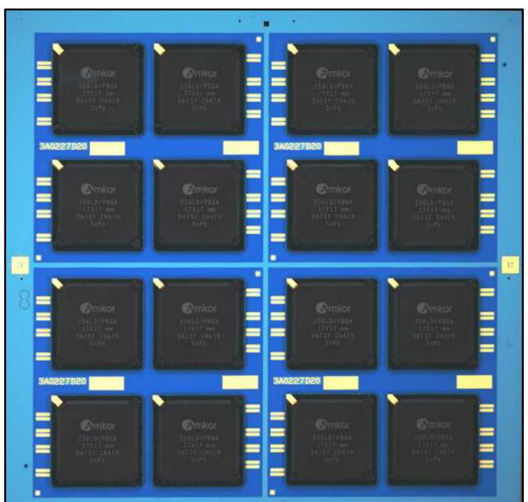
Introduction

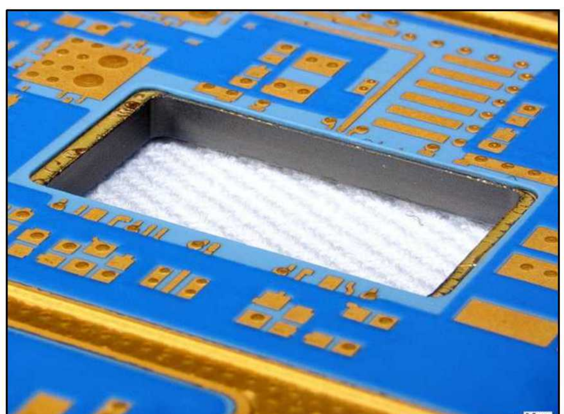
- **Low-temperature co-fired ceramic (LTCC) technology can provide the functionality of (organic) printed circuit boards *as well as withstand the high-temperature service of downhole conditions*.**

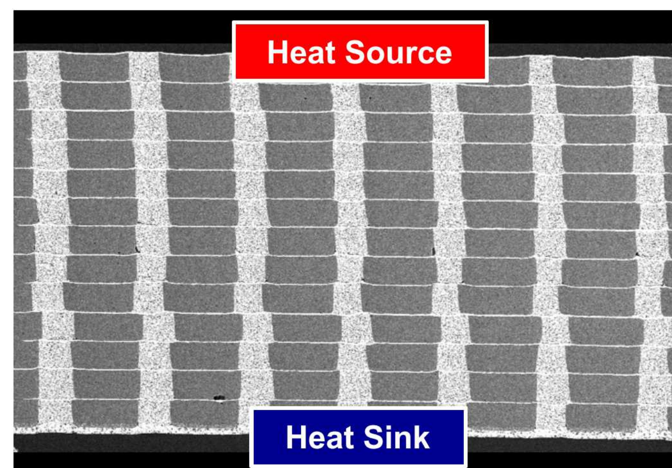






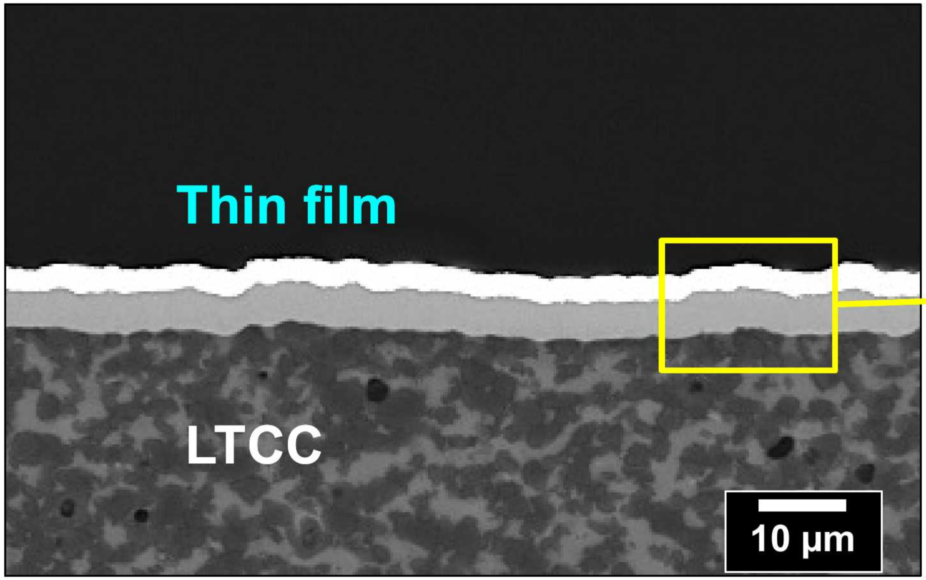


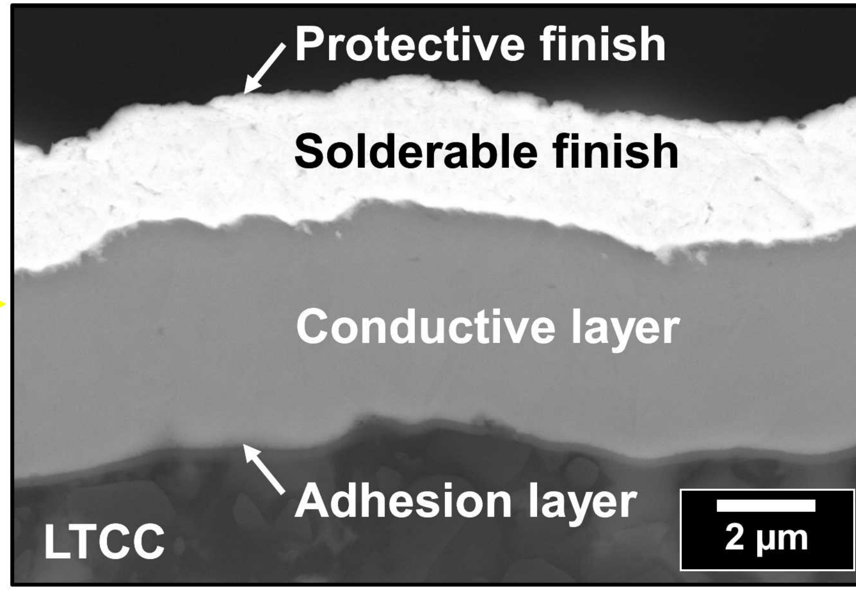


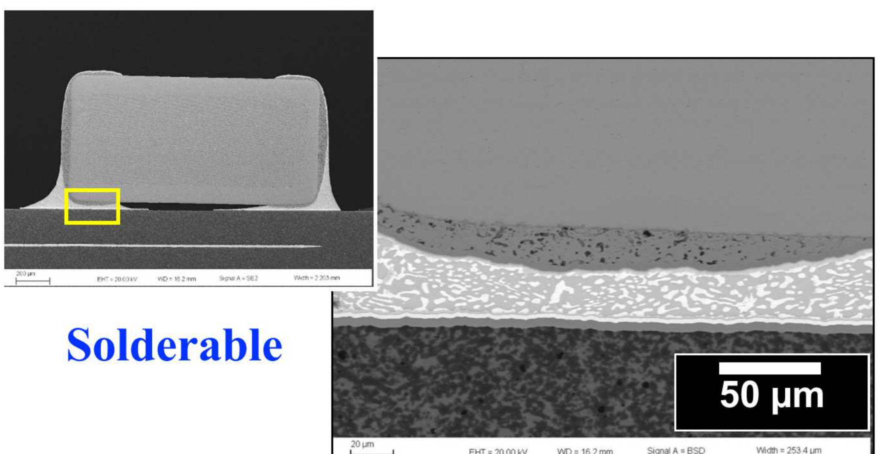


Introduction

- **Thin film conductors** provide the *interconnection technology*.

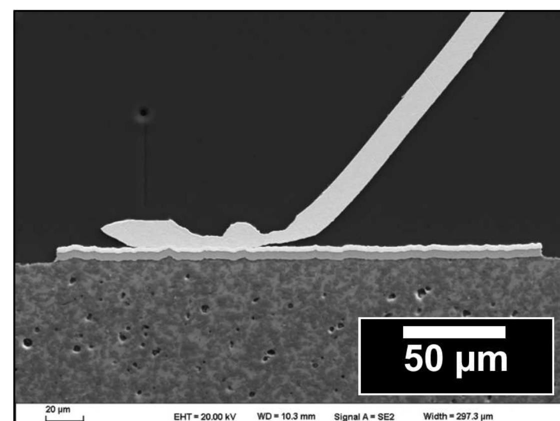






Solderable

Wire and ribbon bondable

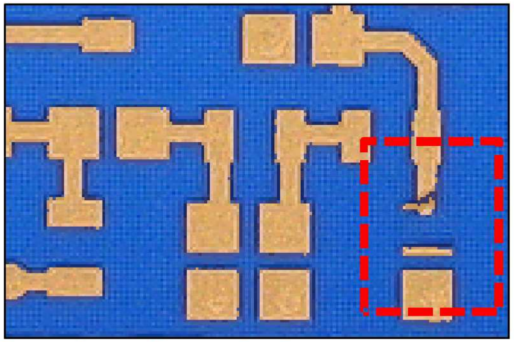


Path-Forward

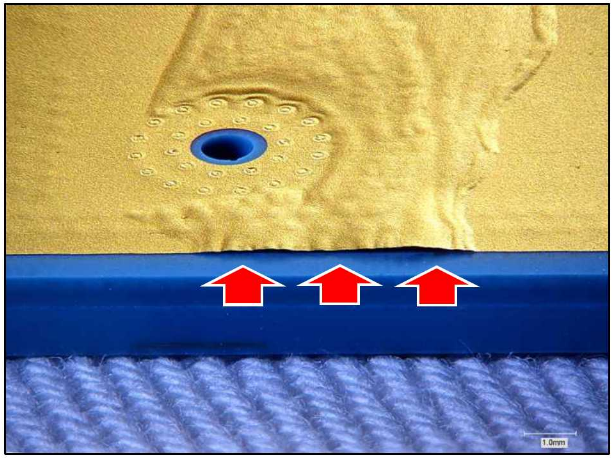
- **Problem:**

  Thin film performance and reliability are sensitive to numerous factors:

  - **Choice of layers (the "stack")**
  - **Interface adhesion**
  - **Surface contamination**



Delamination defects



> ***Cost-effective product yields necessitate a means to optimize the performance of thin films on LTCC.***

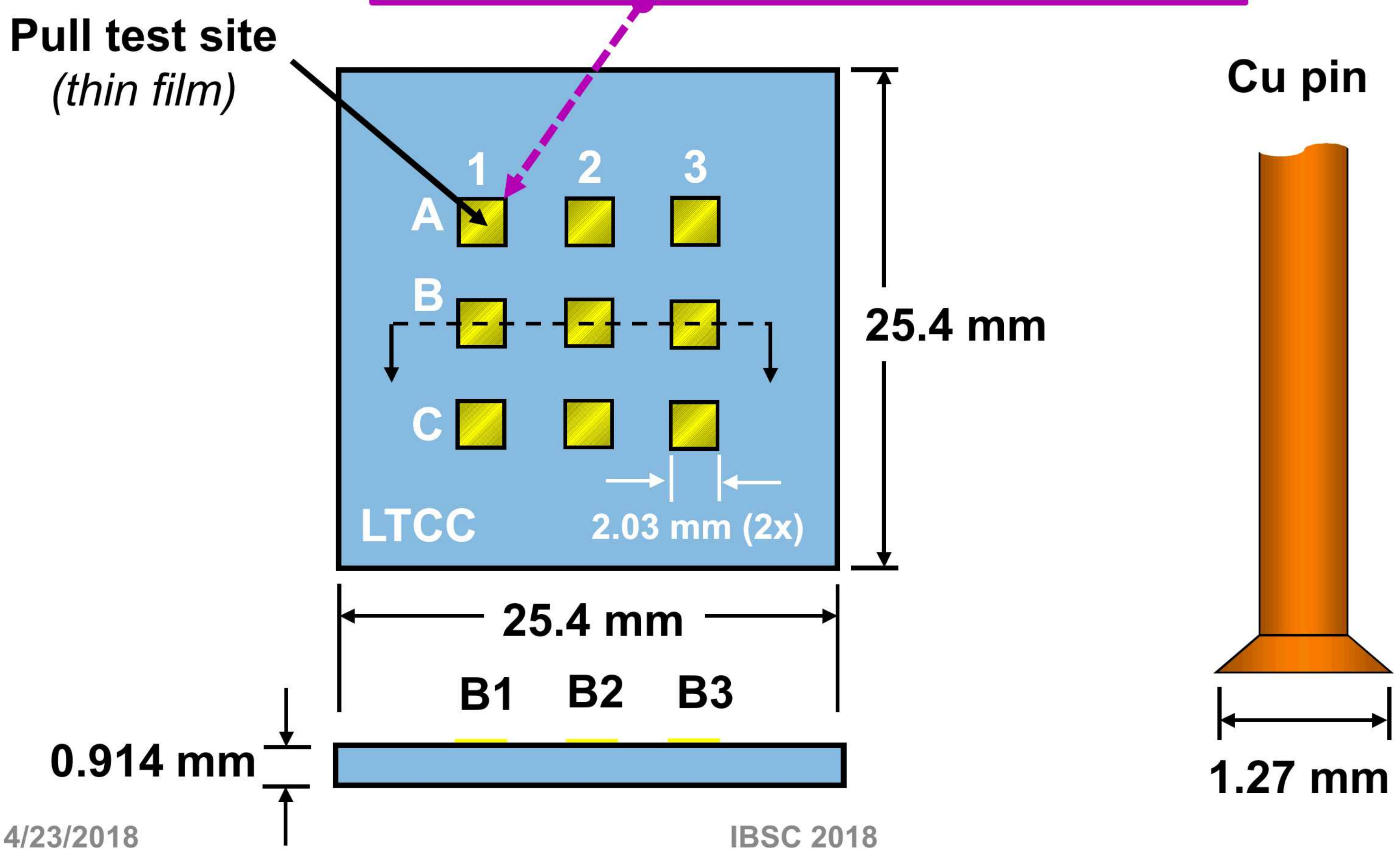
- **Objective:**

  Develop a test methodology and assess the fundamental strength of solder joints made to thin films on LTCC.

Experimental Procedure

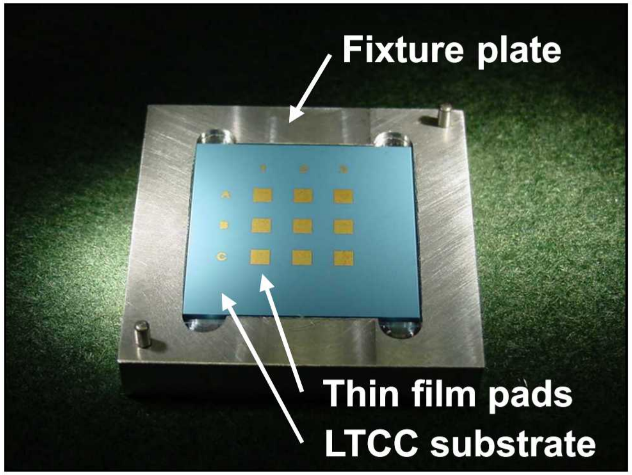
- A **pin pull test** was developed to measure the tensile strength of **solder joints** made to thin film conductors on LTCC substrates.

The pattern was created by evaporation of the thin film through an aperture mask.

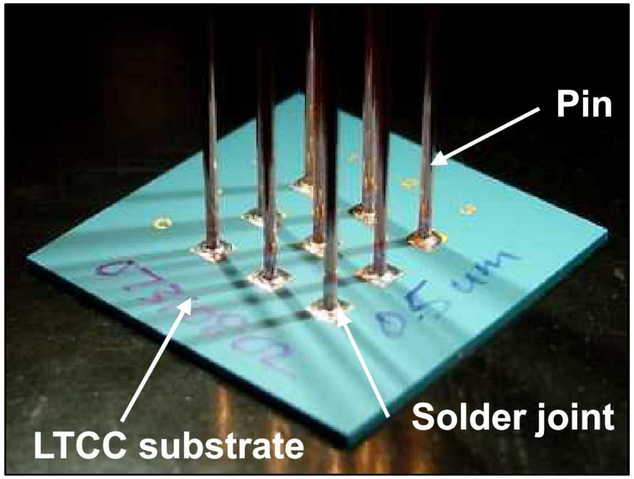


Experimental Procedure

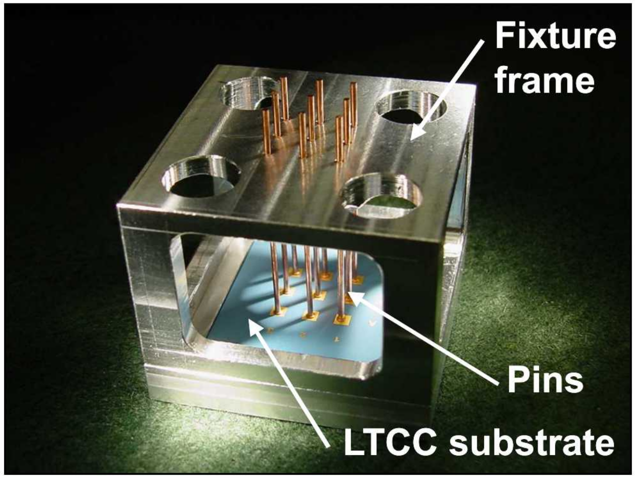
- The test assembly was fabricated by soldering a pin to each of the nine (9) thin film pads, using a conduction furnace.



Substrate is placed on the fixture plate.



Completed test specimen



Fixture frame and pins are put into place.

Experimental Procedure

- The low-temperature, co-fired ceramic (LTCC) substrate is fabricated from the DuPont™ 951 tape*
- The thin film is … 0.20 Ti/W - 4.0 Cu - 2.0 Pt - 0.38 Au (µm)
- The solder alloy (wt.%) … 63Sn-37Pb (Sn-Pb)
- Soldering times (seconds) and temperatures (°C):

	15s	60s	120s
215°C			
240°C			
260°C			
290°C			

* *DuPont™ is a registered trademark of E.I. DuPont de Nemours Corp., Wilmington, DE.*

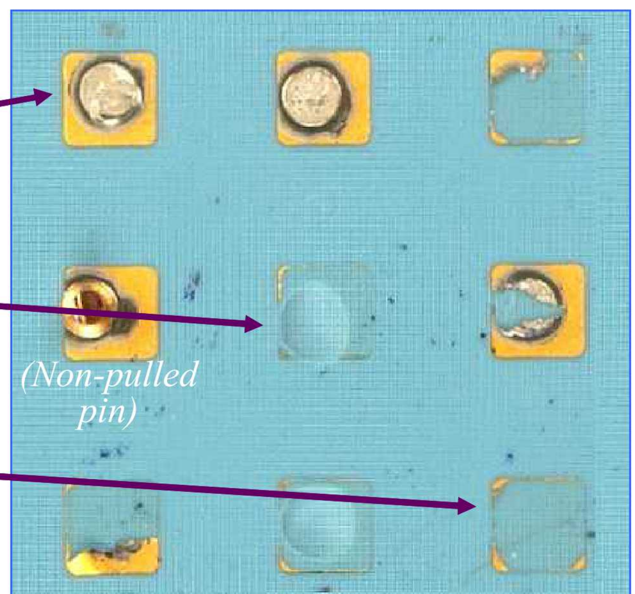
Experimental Procedure

- The pin pull test was performed at **10 mm/min**.
- Eight (8) of nine (9) pins were pull tested on duplicate test specimens per condition, for a total of **sixteen (16) data points**.
- Fracture mode analysis is a *critical* step in this study.
  - There were four predominant failure modes:

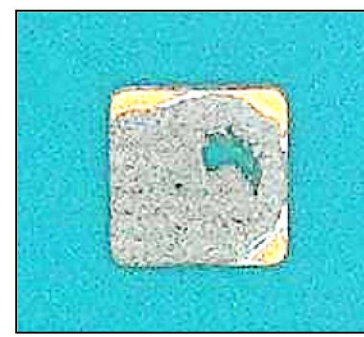
Solder failure

Divot failure

Thin film delamination failure

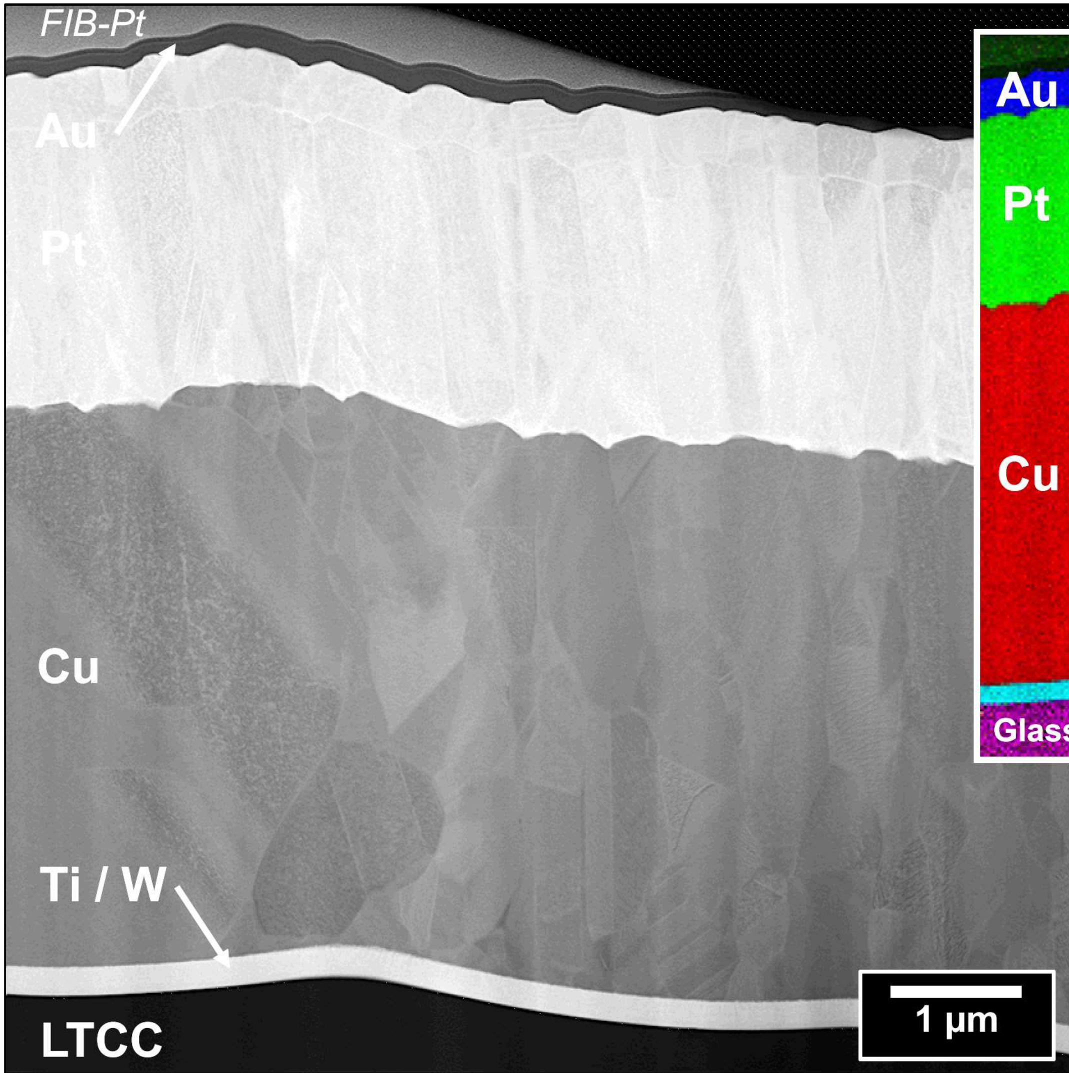


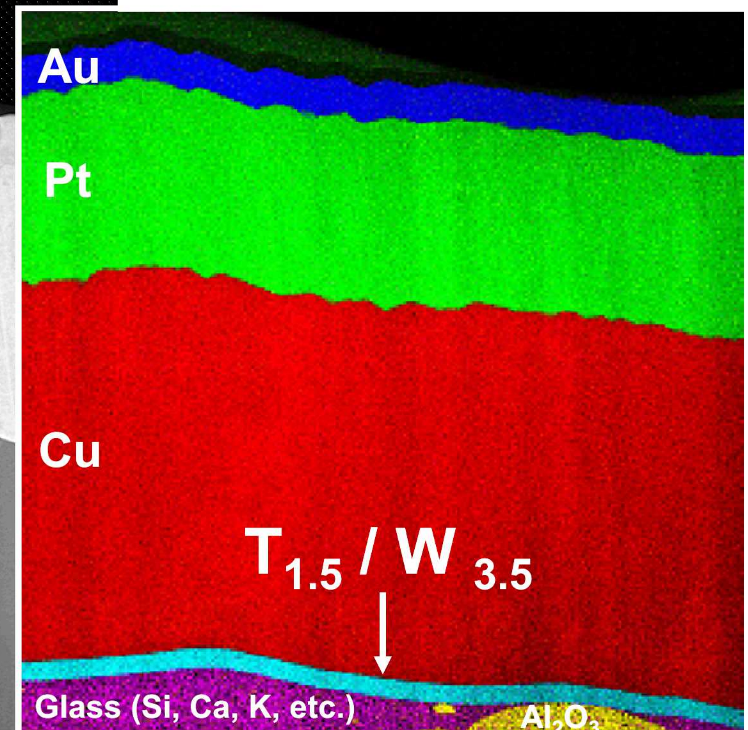
Thin film peeling



Results – Analysis of the Ti/W – Cu – Pt – Au Thin Film

- **Microanalysis methods documented the thin film structure.**

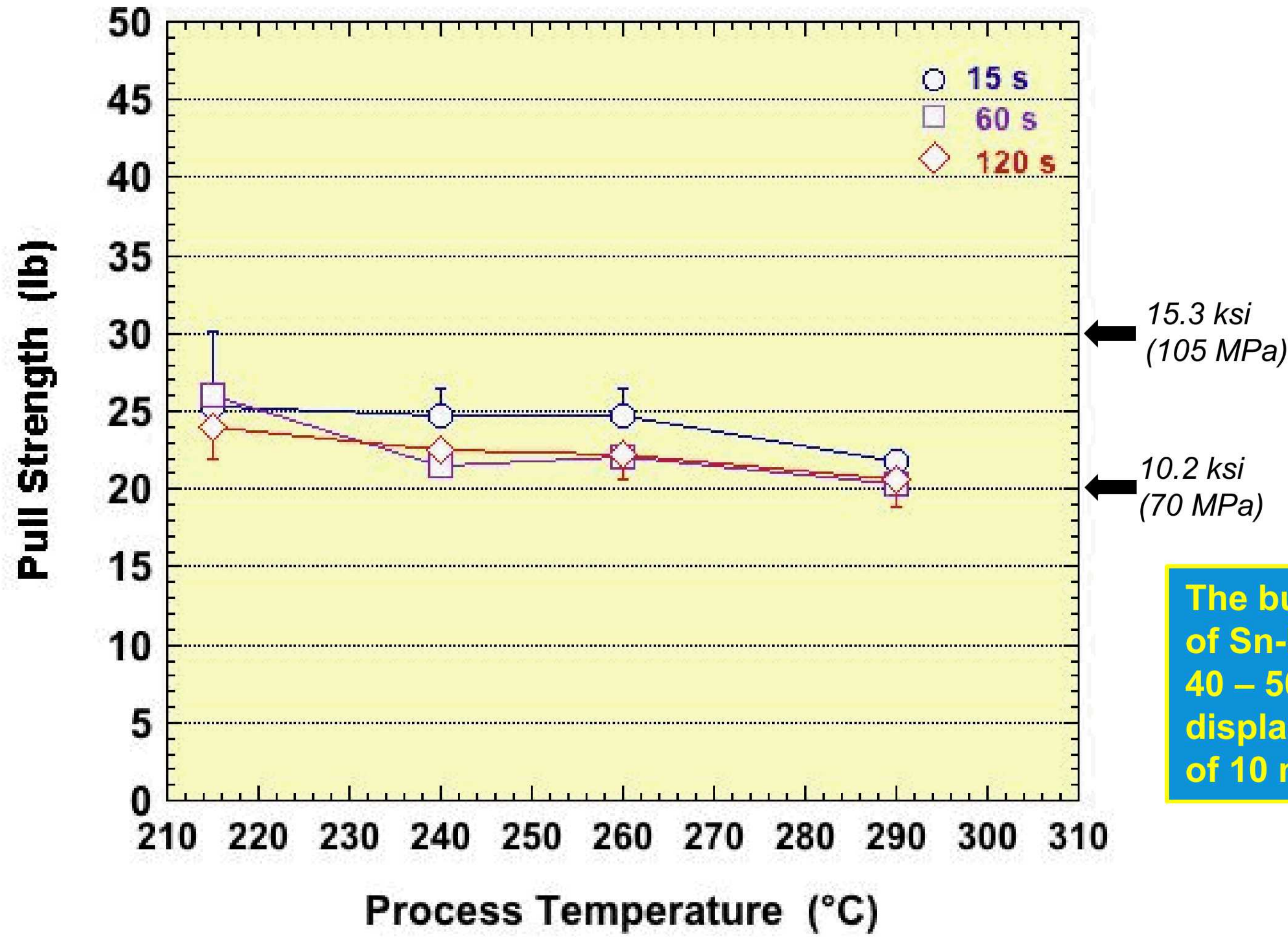




Focused ion-beam (FIB) sectioning and annular spectral analysis confirmed the microstructure and chemistry of the layers.

Results – Pull Strengths of the Sn-Pb Solder Joints

- The pull strengths are shown as a function of soldering temperature.

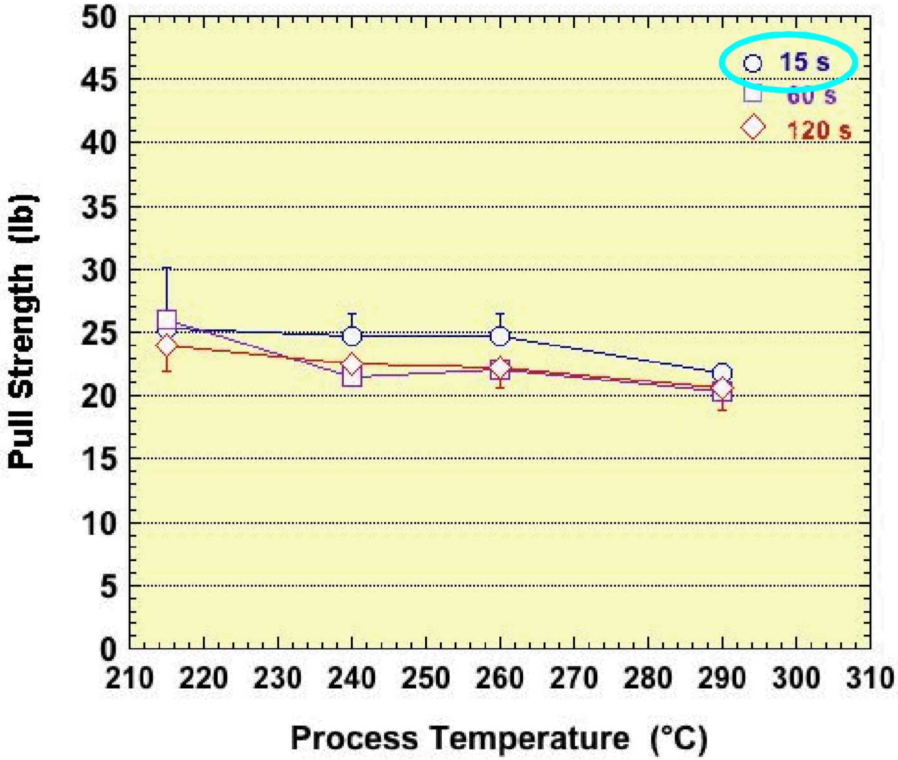


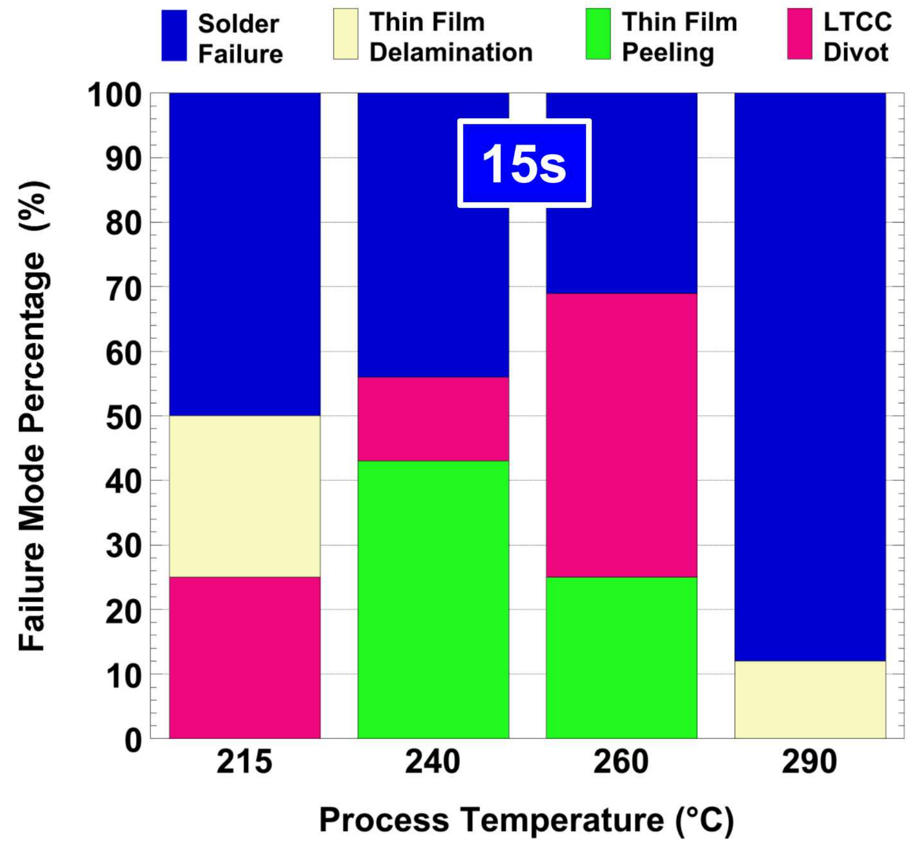
The bulk strength of Sn-Pb solder is 40 – 50 MPa at the displacement rate of 10 mm/min.

- The 60 s and 120 s values were lower than 15 s at 240°C and 260°C.

Results – Failure Mode Analysis – 15 s

- **The pull strengths were correlated to the failure mode trends.**

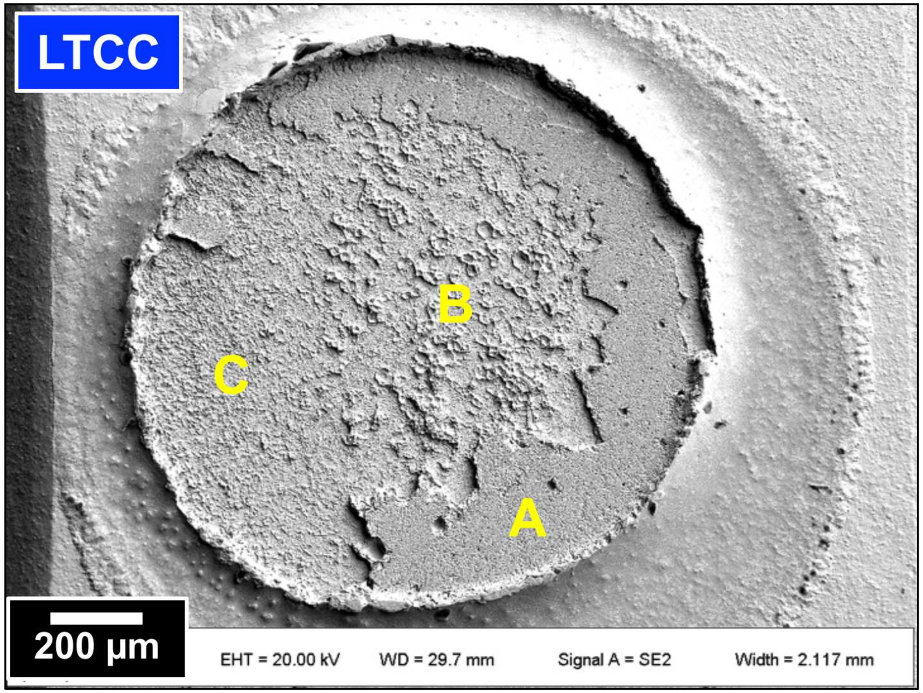


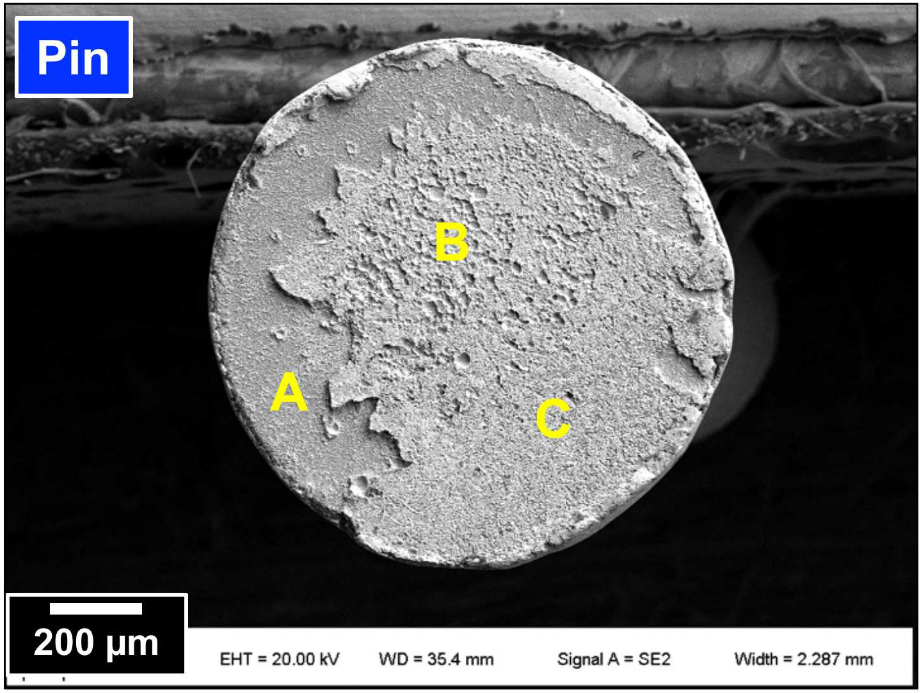


- **215°C – 260°C:** *significant failure mode change accompanied the relatively limited changes in pull strength.*
- **290°C: ………..** *solder failure dominated the fracture surfaces.*

Results – Failure Mode Analysis – 15 s

- The SEM images show matching surfaces of the solder failure mode.
- Three morphologies A, B, and C characterized the fracture surfaces.



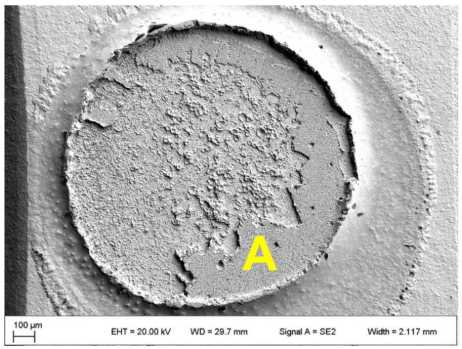


(9051301-08, As-fab 215°C; 15 s; C1)

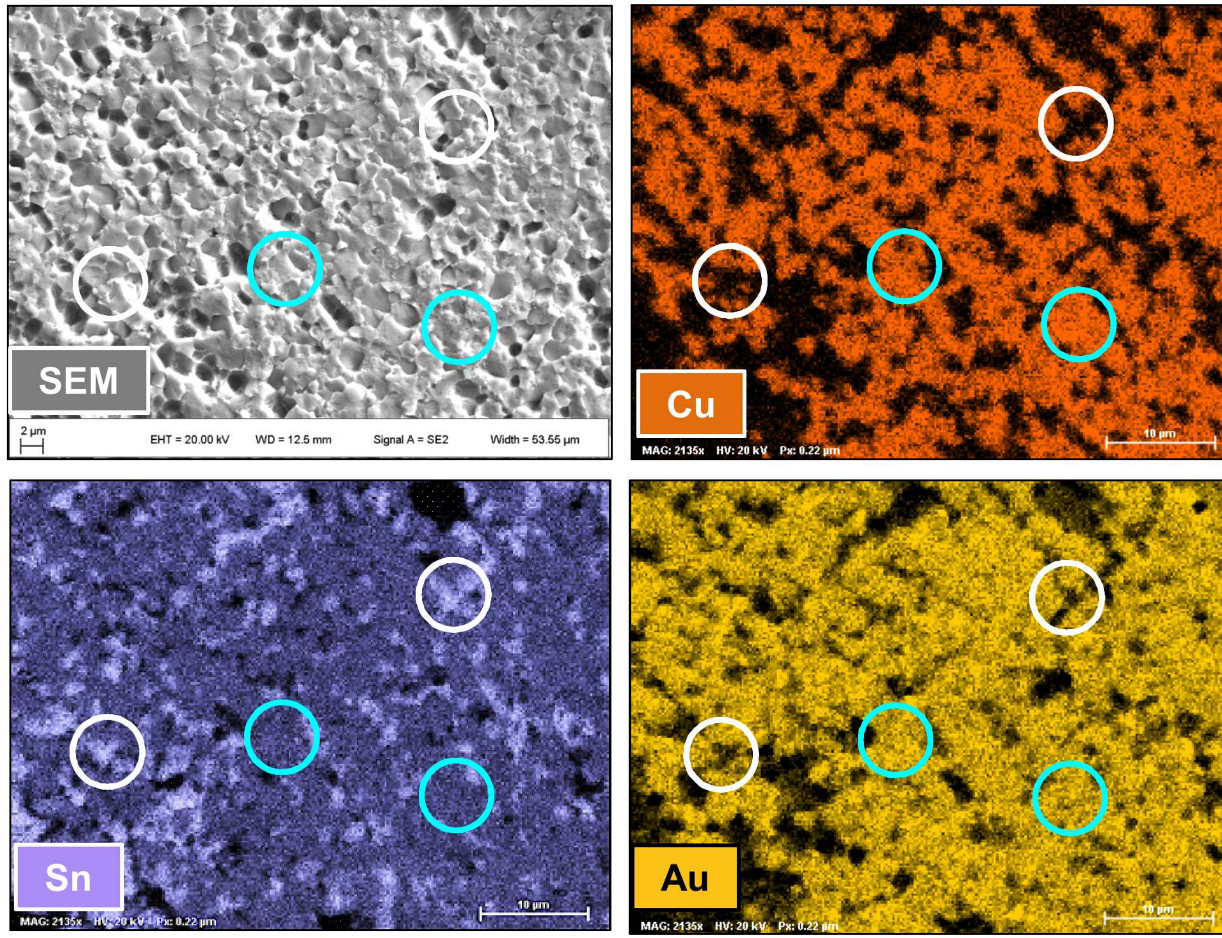
- Energy dispersive x-ray (EDX) analysis was used to determine the chemical signatures of the fracture surfaces.

Results – Failure Mode Analysis – 15 s

- **Area A** has an intergranular morphology, indicating ***brittle fracture***.



(9051301-08, As-fab 215°C; 15 s; C1)



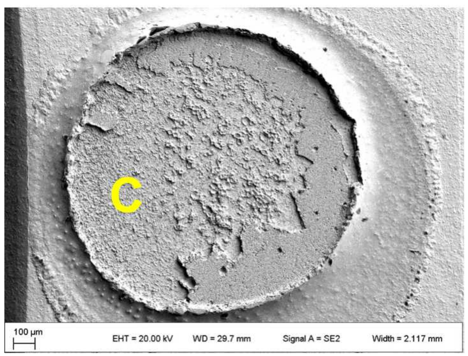
○ **Sn, only**

○ **$(Au, Cu)_xSn_y$ intermetallic compound (IMC)**

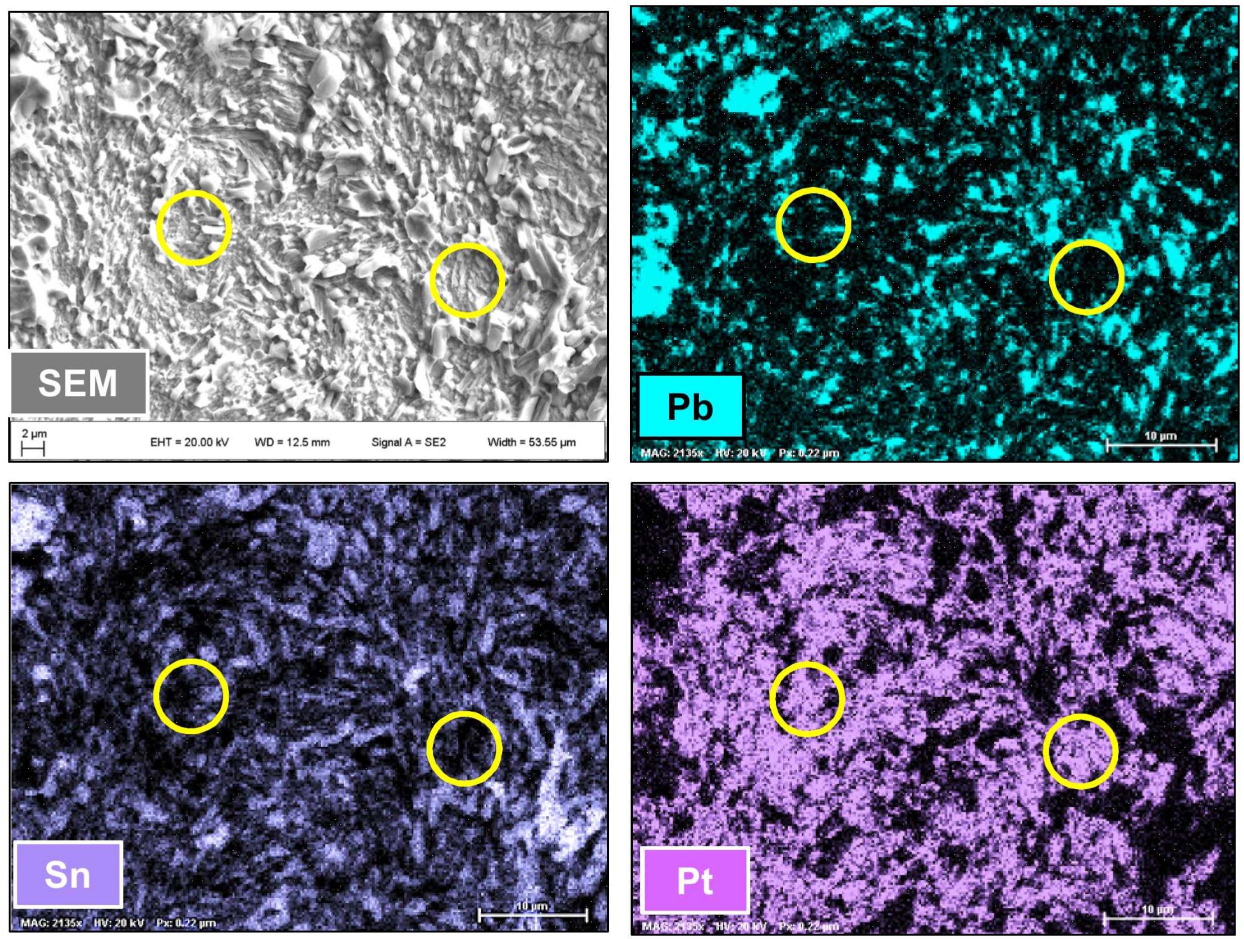
- **The *same morphology and chemistries* were observed on the pin.**

Results – Failure Mode Analysis – 15 s

- **Area C exhibited more deformation, indicating a *ductile fracture*.**



(9051301-08, As-fab 215°C; 15 s; C1)



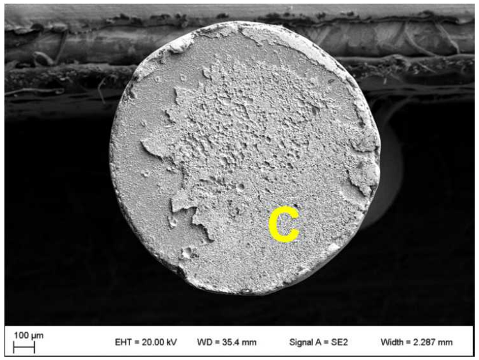
Largely 100Pt

Islands of 100Pb are also present.

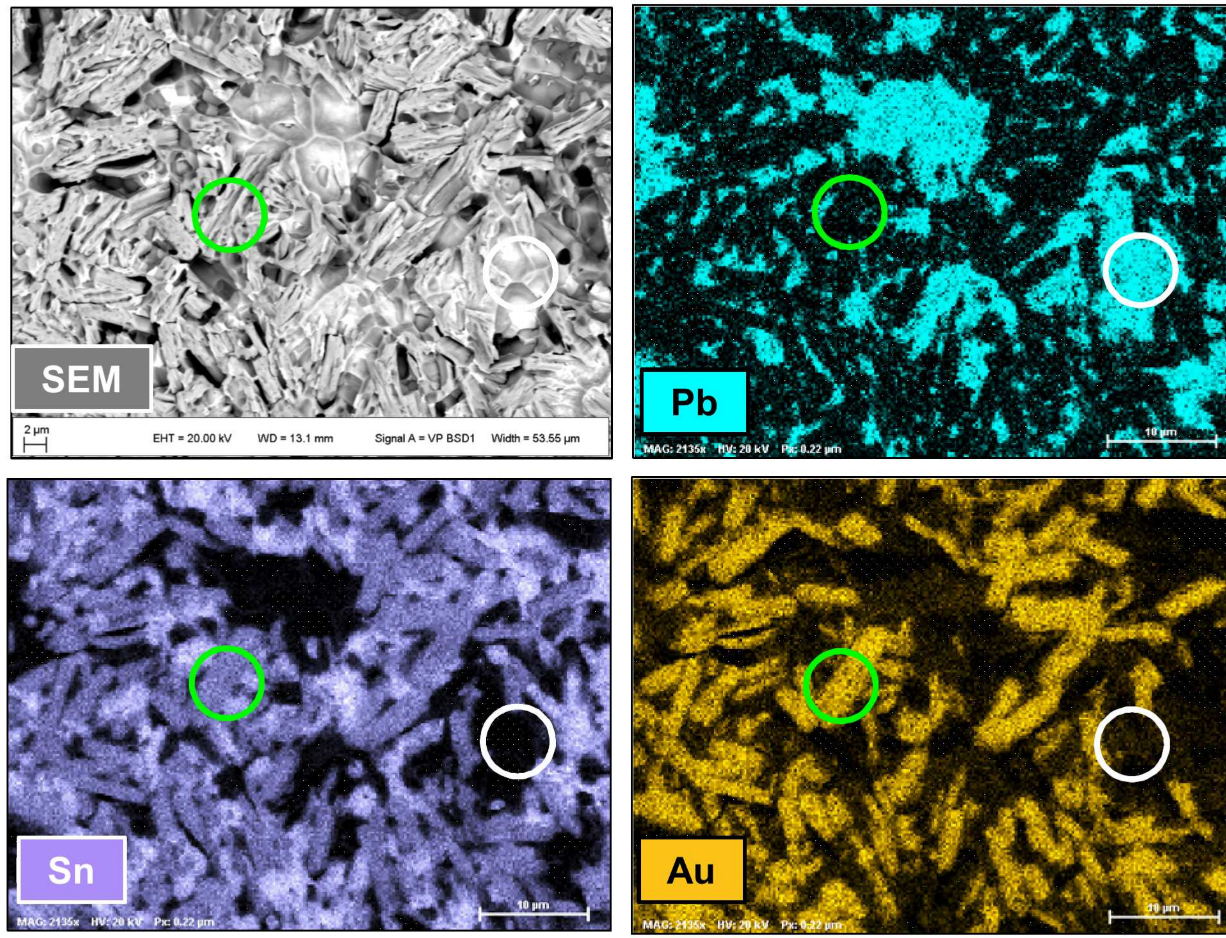
- **Area B was similar to area C, but with more Pb-rich phase.**

Results – Failure Mode Analysis – 15 s

- The corresponding **Area C** was examined **on the pin.**



(9051301-08, As-fab 215°C; 15 s; C1)



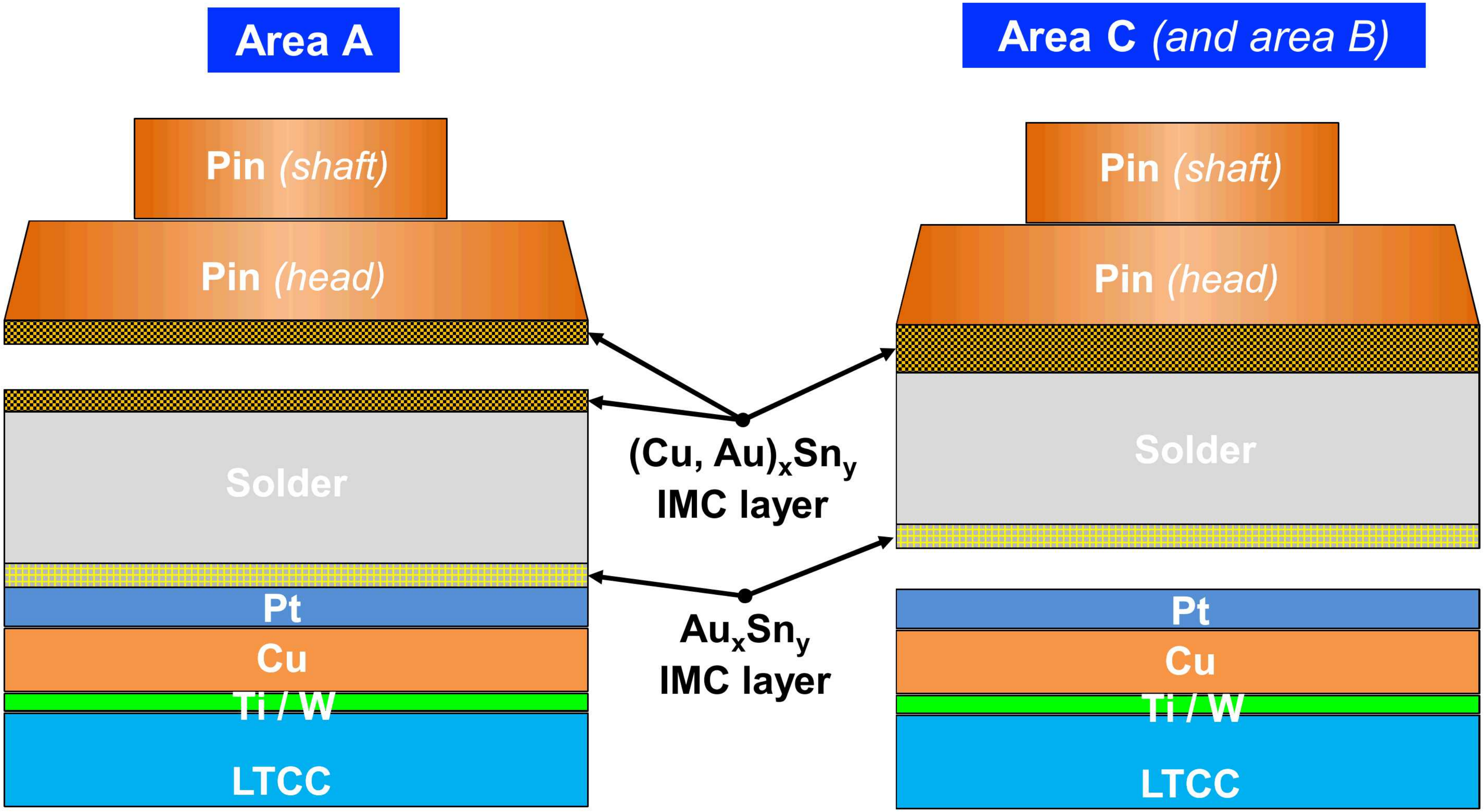
Au_xSn_y IMC

100Pb

- The fracture **area C** showed a crystalline morphology **on the pin.**

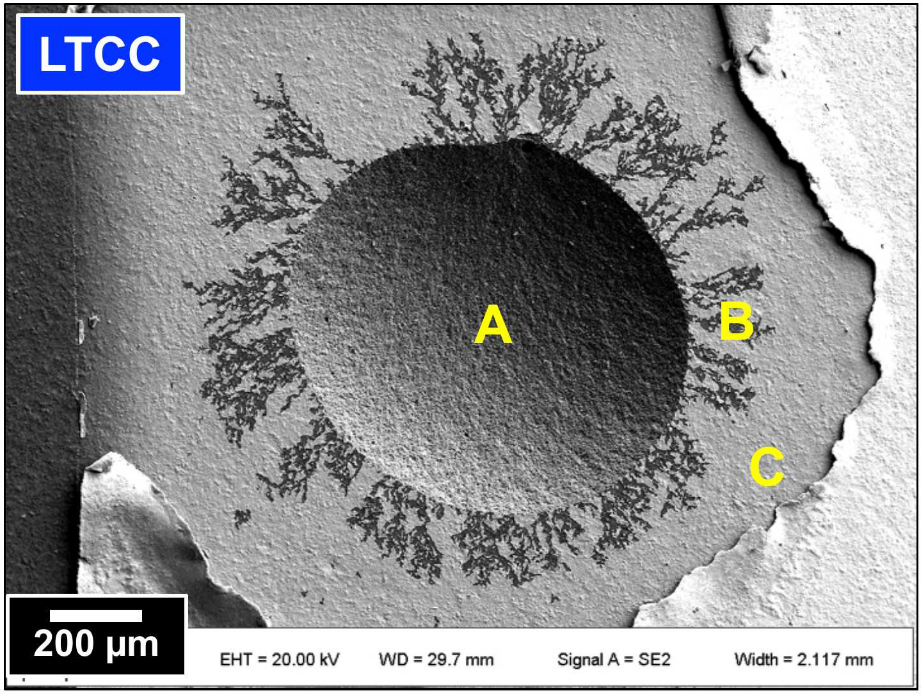
Results – Failure Mode Analysis – 15 s

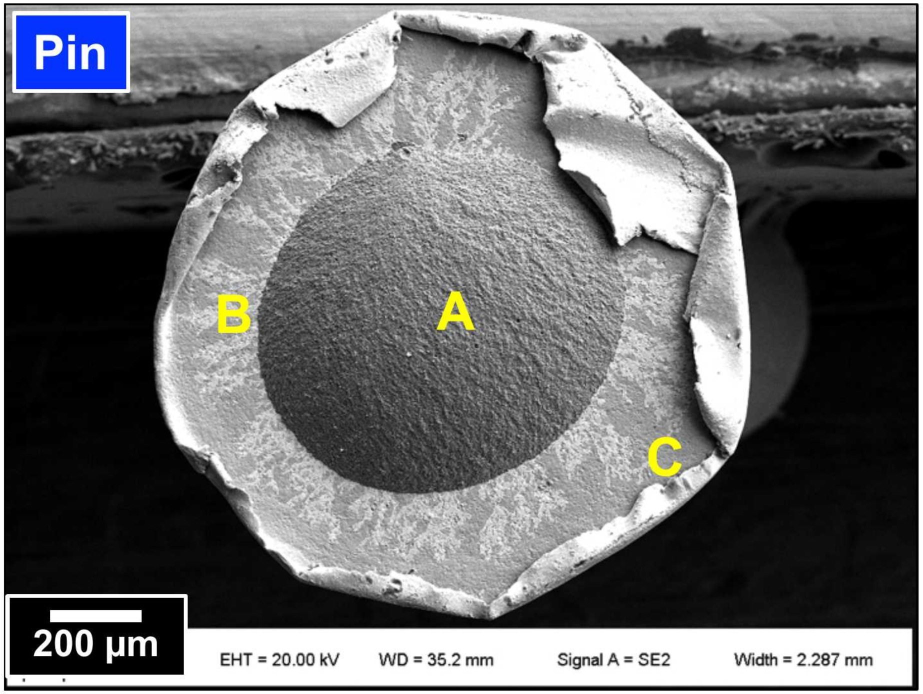
- The crack paths are illustrated by these schematic diagrams.



Results – Failure Mode Analysis – 15 s

- The **divot failure** exhibited three crack paths.
  - A … bulk fracture in the LTCC
  - B … combination of thin film delamination and peeling
  - C … thin film delamination

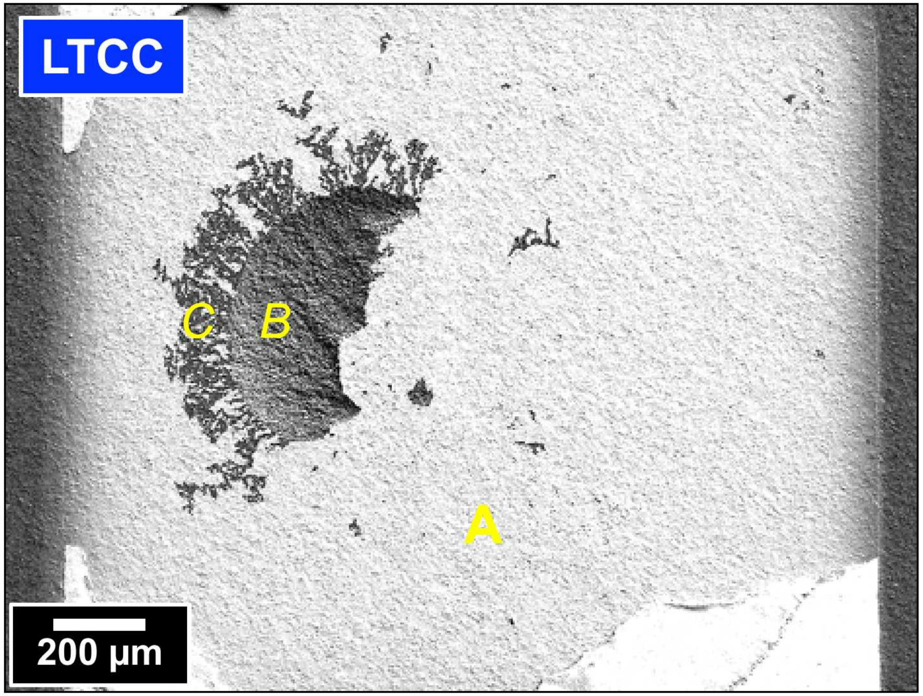


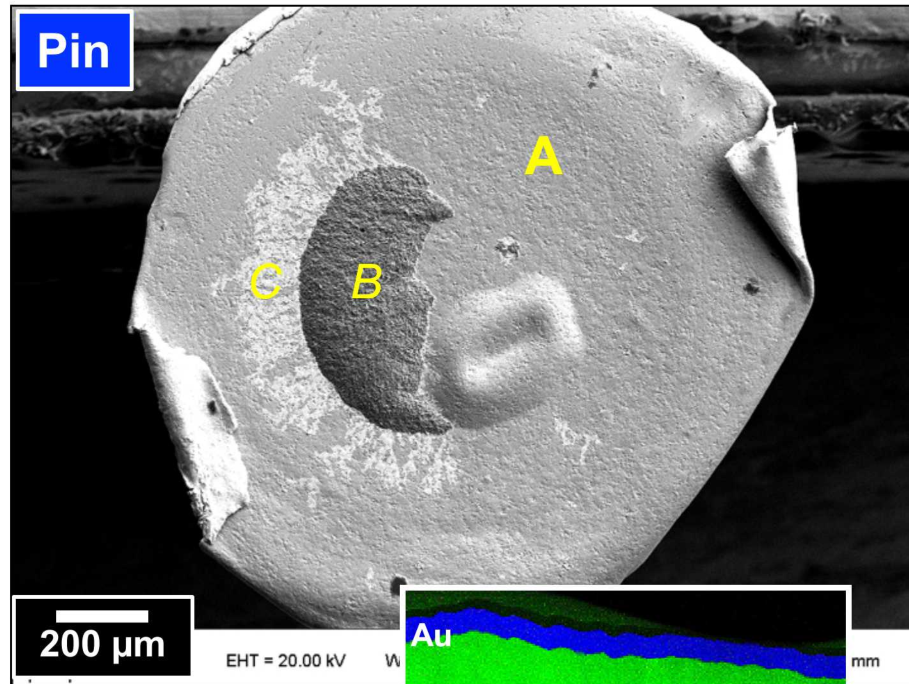


(9051301-08, As-fab 215°C; 15 s; C1)

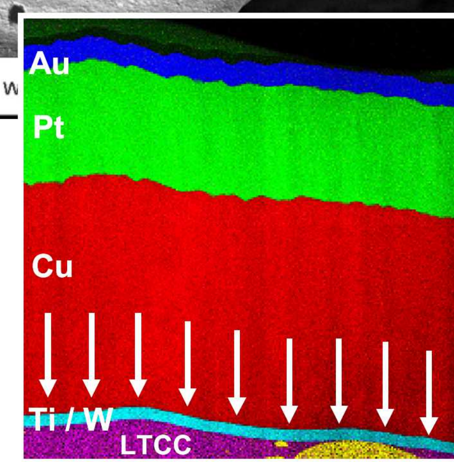
Results – Failure Mode Analysis – 15 s

- **Thin film peeling failure (A) was caused by fracture *within* the film.**





9091325-32, As-fab 245°C; 15 s; C1

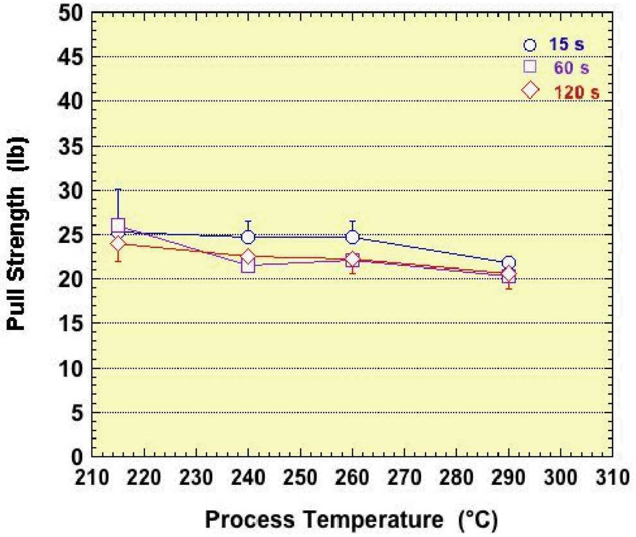


- **The EDX analysis determined that separation occurred, specifically, at the Ti/W - Cu interface.**

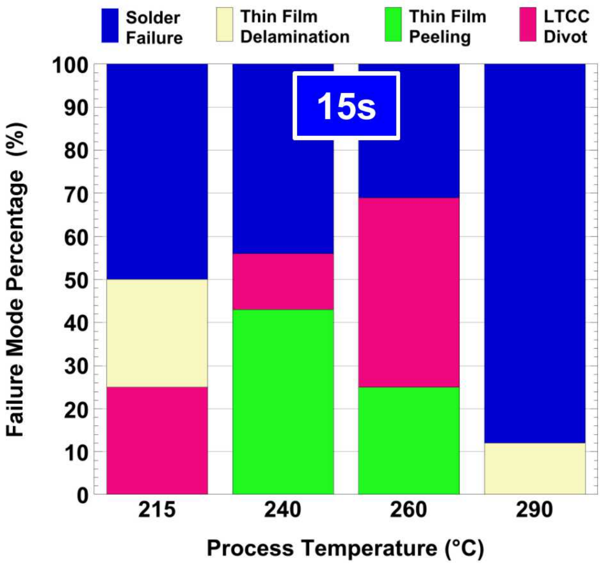
Results – Failure Mode versus Strength

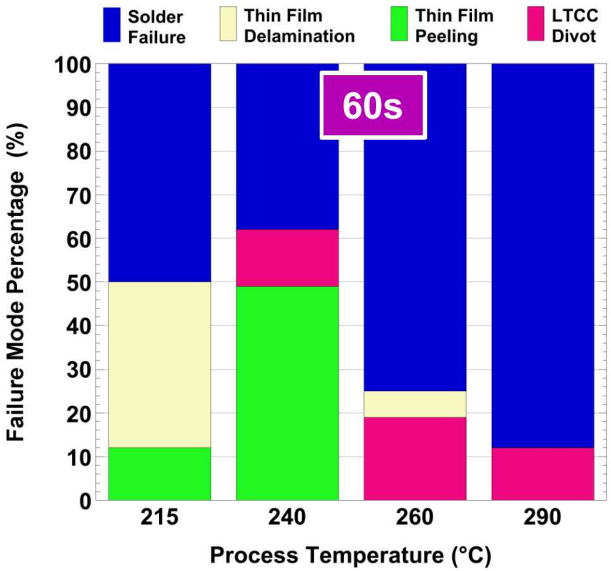
- The three failure modes:
  - Thin film delamination
  - Thin film peeling
  - LTCC divots

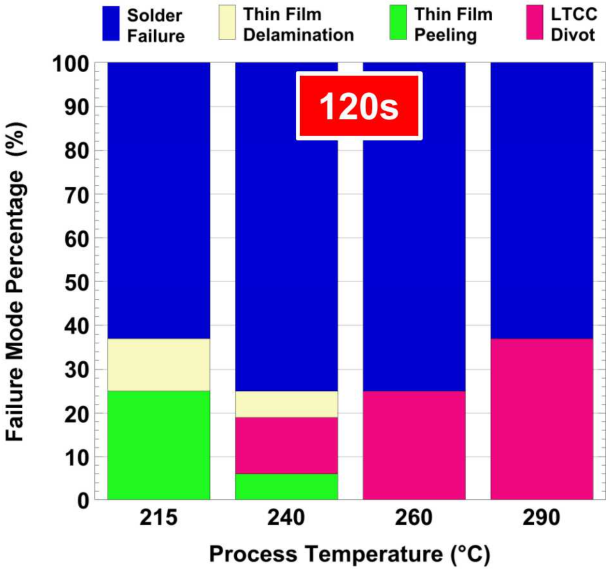
  did not correlate with the strength trends.



- These failure modes shifted to the lower process temperatures and lesser presence.

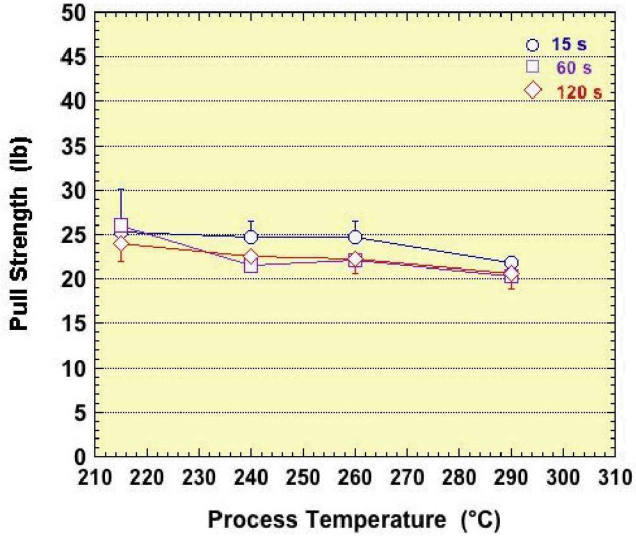


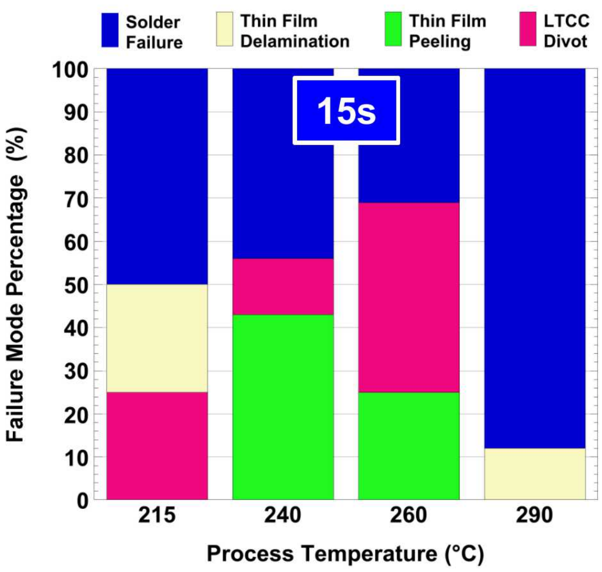


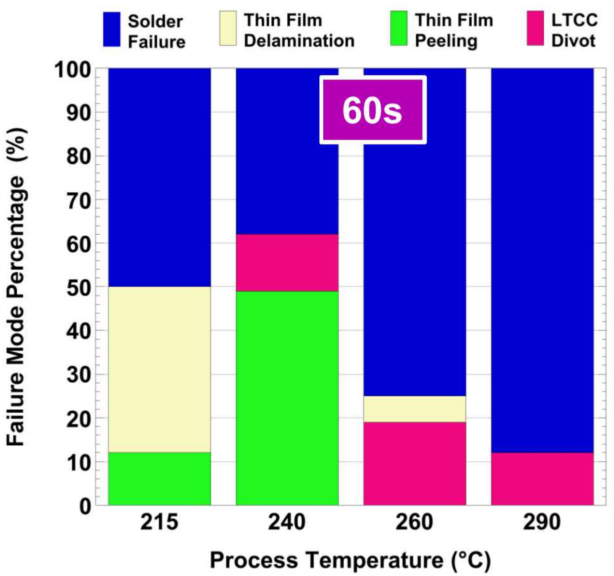


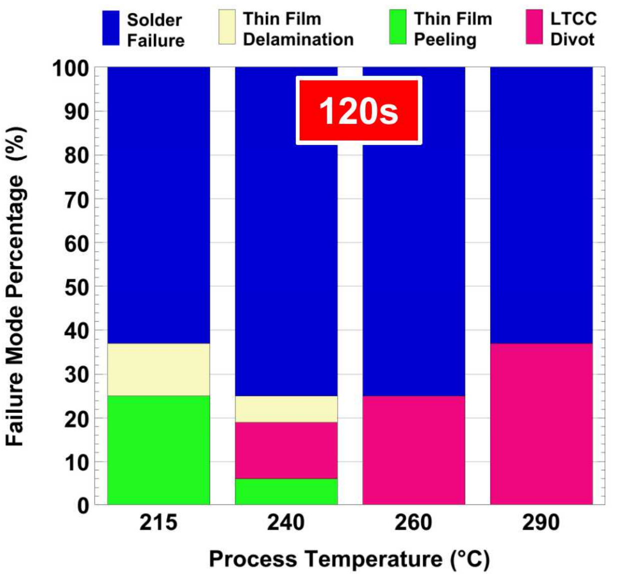
Results – Failure Mode versus Strength

- The **solder failure mode** exhibited a significant presence at 290°C, 15s
- As soldering time durations increased, the solder failure mode became *more prevalent at lower soldering temperatures*.
- The increase of the solder failure mode *generally* correlated to a loss of strength.



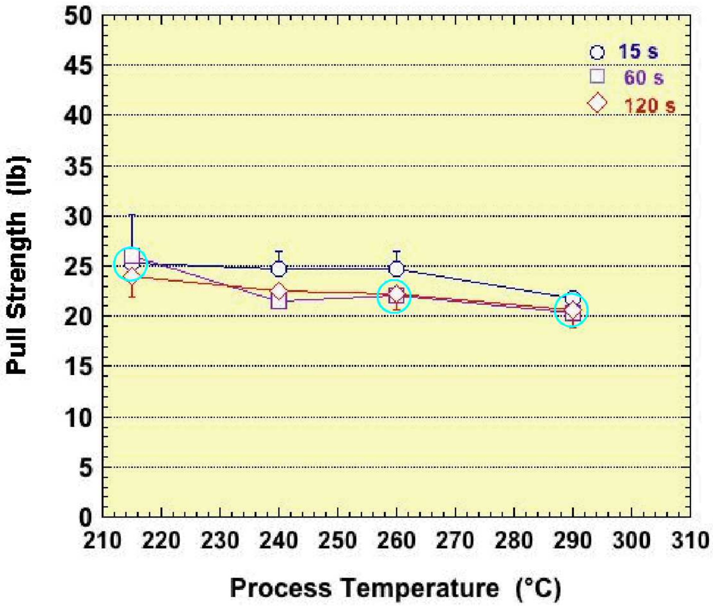


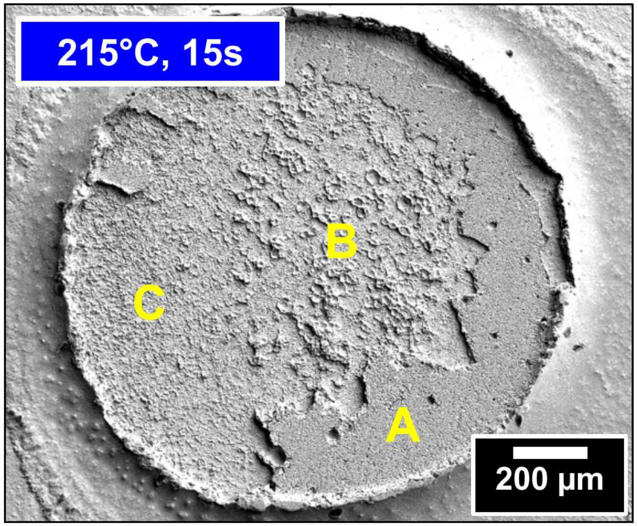


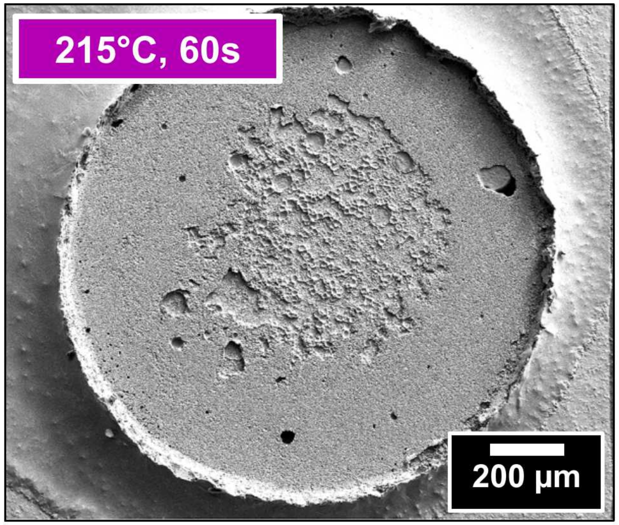


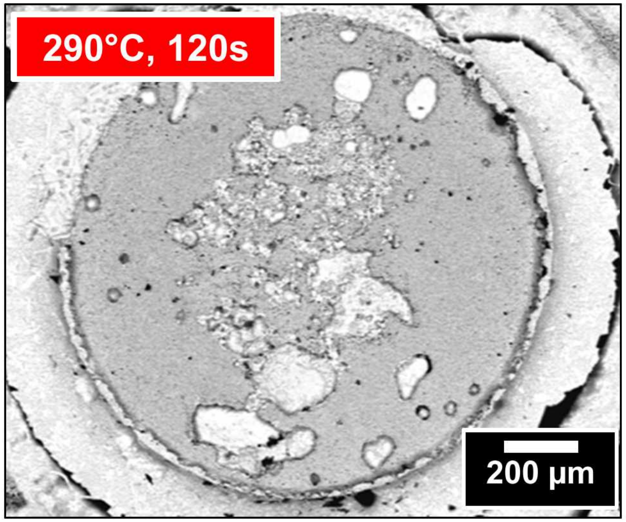
Results – Failure Mode versus Strength

- The strength decrease, albeit small, was accompanied by a change in the fracture surface morphology.
- The fracture surface, “A”, increased in extent with the “severity” of the soldering process.
  - Area “A” was separation within the $(Cu, Au)_xSn_y$ IMC layer at the Cu pin.





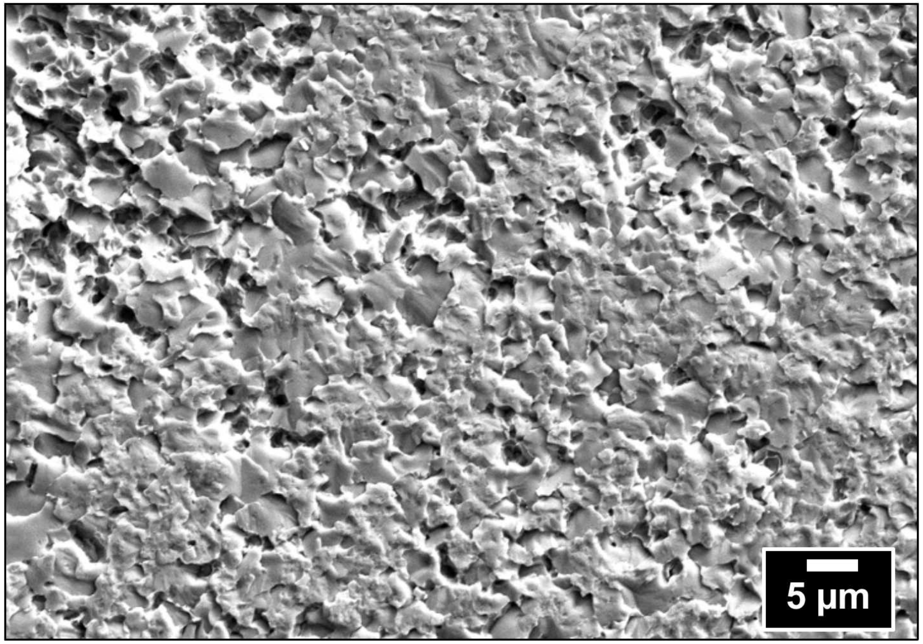




Results – Failure Mode versus Strength

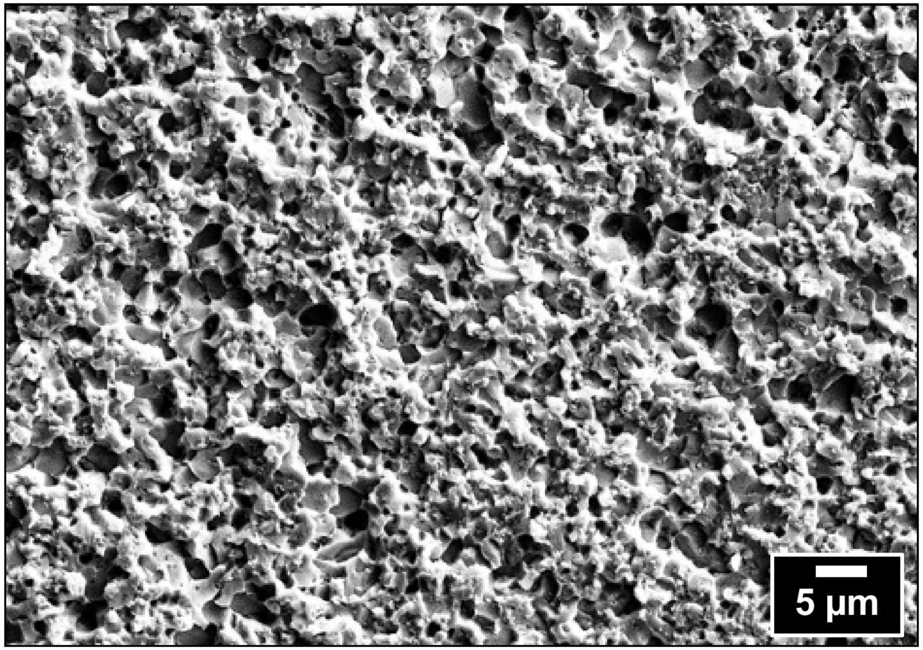
- The **"A" fracture surface** changed on the micro-scale.

215°C, 60s



7241303, As-fab 215°C; 60 s; A1

290°C, 120s



7301303, As-fab 290°C; 120 s; A1

The increased surface relief was caused by further growth of the (Cu, Au)$_x$Sn$_y$ IMC layer at the Cu pin side of the joint.

Summary

- A study was performed to evaluate the tensile strength of Sn-Pb solder joints made to 0.20Ti/W - 4.0Cu - 2.0Pt - 0.38Au (µm) thin films on low-temperature, co-fired ceramic (LTCC) substrates.
- The strength performance was evaluated as a function of soldering time and temperature process parameters.
- Pin pull strengths remained excellent, across the process conditions.
- Four failure modes were identify on the fracture surfaces.
  - Solder failure
  - Thin film delamination
  - Thin film peeling
  - LTCC divots

Summary

◆ **The latter three failure modes:**

- **Thin film delamination**
- **Thin film peeling**
- **LTCC divots**

… did not correlate with the pull strength trends.

- **The absence of any trend implied that the associated structures had *comparable, intrinsic strength levels*.**

◆ **The strength decrease correlated with the solder failure mode.**

- **The strength loss was associated with an increased presence of *fracture in the (Cu, Au)$_x$Sn$_y$ IMC layer* that developed at the Cu pin side of the Sn-Pb solder joint.**