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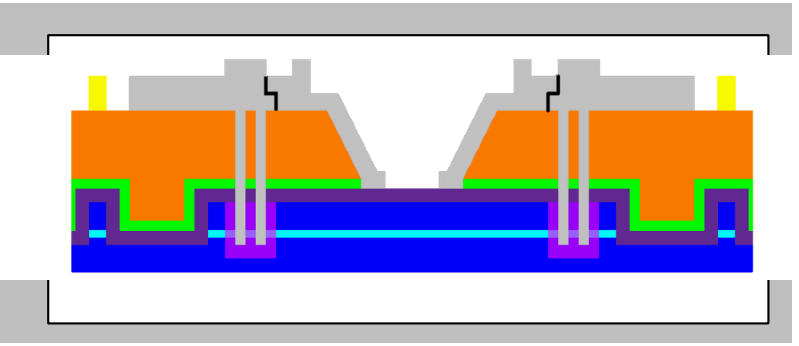
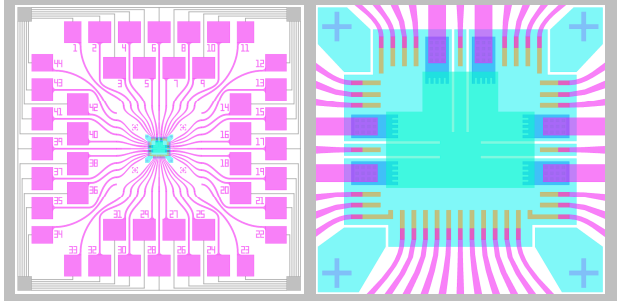




Qubits in Silicon

UW/Delft/Harvard/SNL Collaboration

Dan Ward

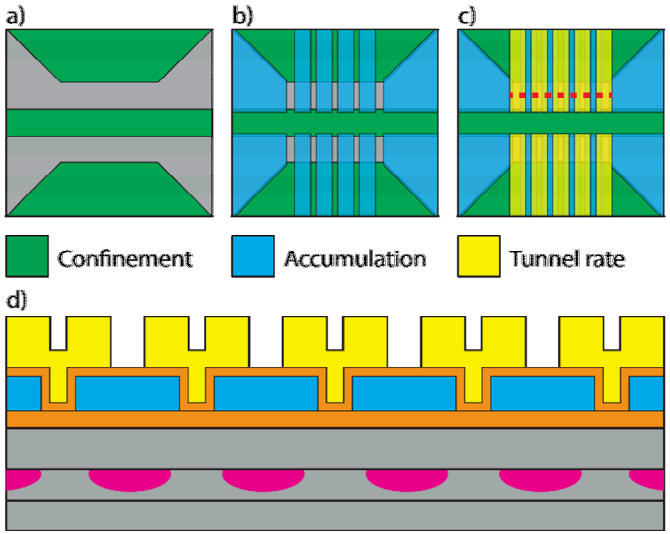
August 15th, 2017

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Overview

- Year 1 Milestone
  - Deliver 32 quadruple quantum dot devices with a yield of 50%
  - Stretch Goal – Extend to six quantum dots

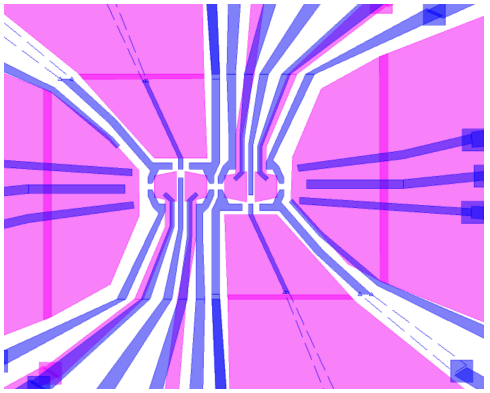
- SNL is focusing on fabrication to support all other team members
  - Wafer level fabrication of starting die
  - Nanostructure fabrication



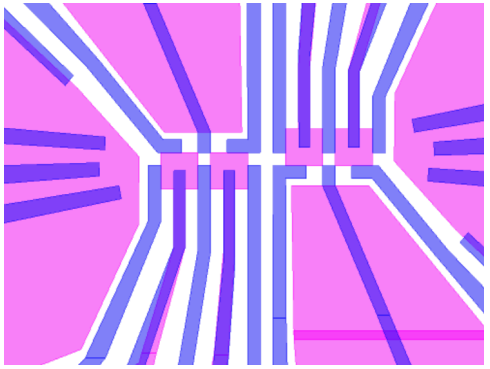
SNL Mesa Fabrication Facility

Fabrication Goals

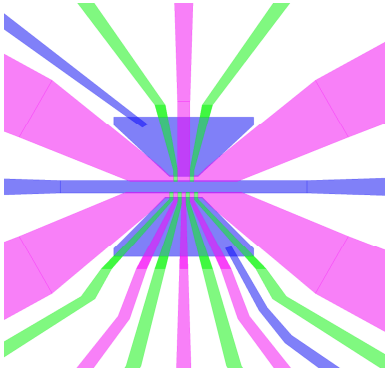
- Meeting the requirements for all team members
  - Enable different device types: “Open” and “Closed”
  - Devices must be measureable everywhere
  - Support a variety of sample mounting PCBs
    - Die size requirements
    - Layout concerns for RF
- Material optimization
  - Testers and witness samples to detect fabrication failure mechanisms and performance hits
    - Ohmic continuity
    - Gate-ohmic isolation
    - Gate-gate isolation
    - Hall mobility
    - Threshold voltage
    - RF transmission/reflection



Gate Layout - Harvard



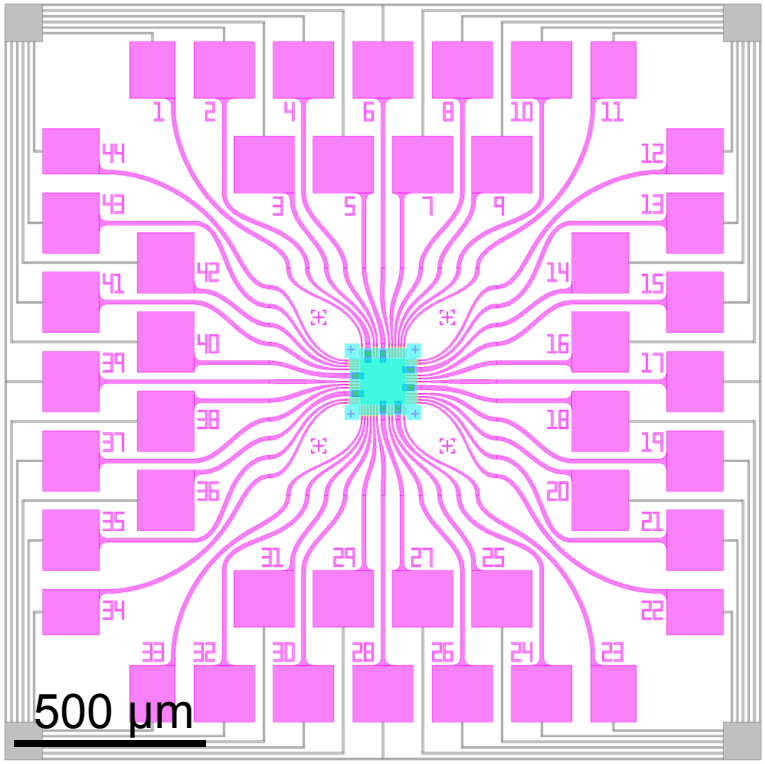
Gate Layout – UW – “Open”

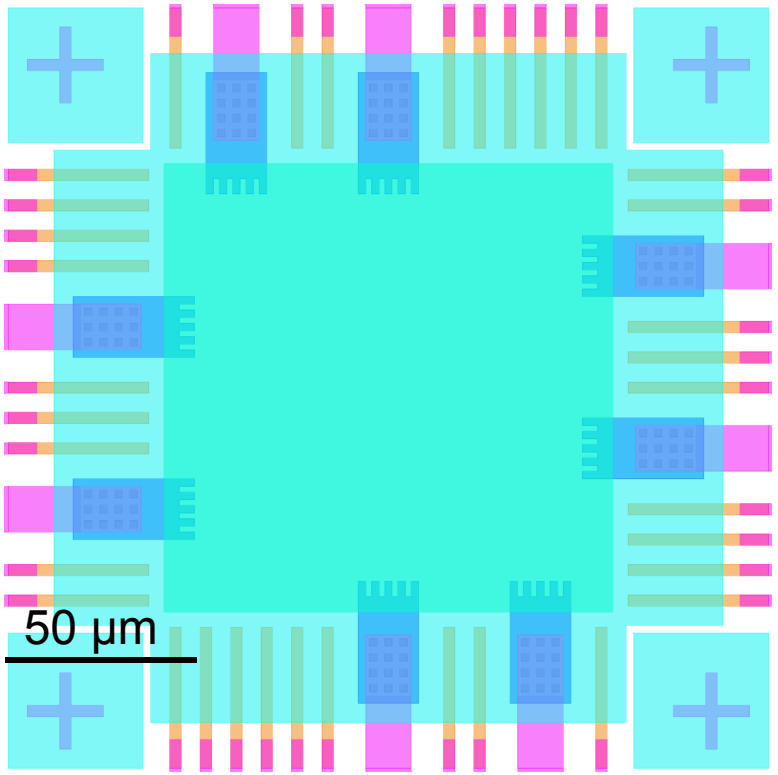


Gate Layout – UW – “Closed”

- Wafer level fabrication
  - 75 mm wafer platform
  - 96 die per wafer for 6.0 mm x 6.0 mm die
  - Multiple gate/ohmic layouts
  - Dedicated diagnostic die
  - Die-level designs should be compatible across fabrication facilities as much as possible

Nanostructure Die Design
Open Device Layouts



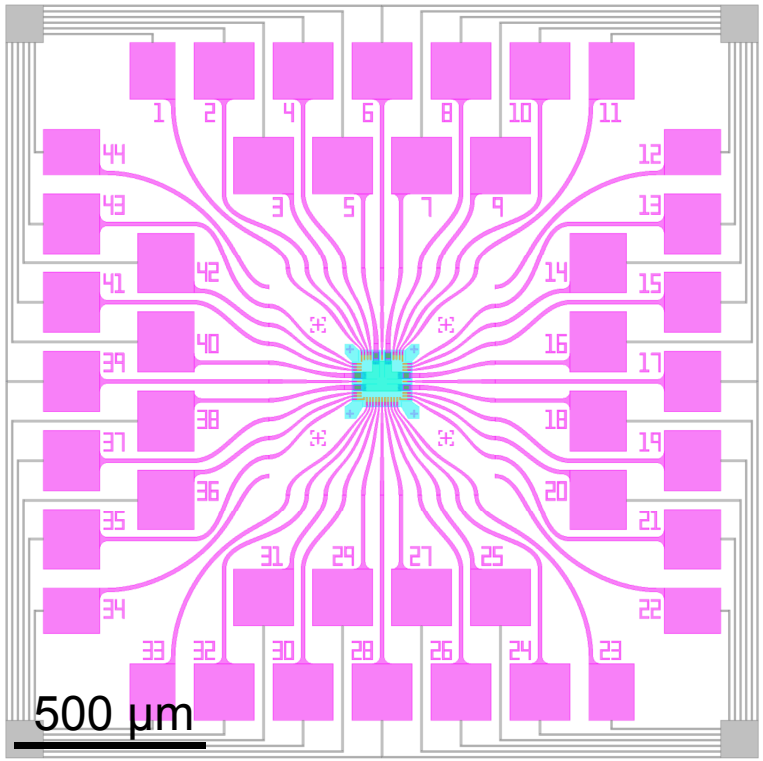


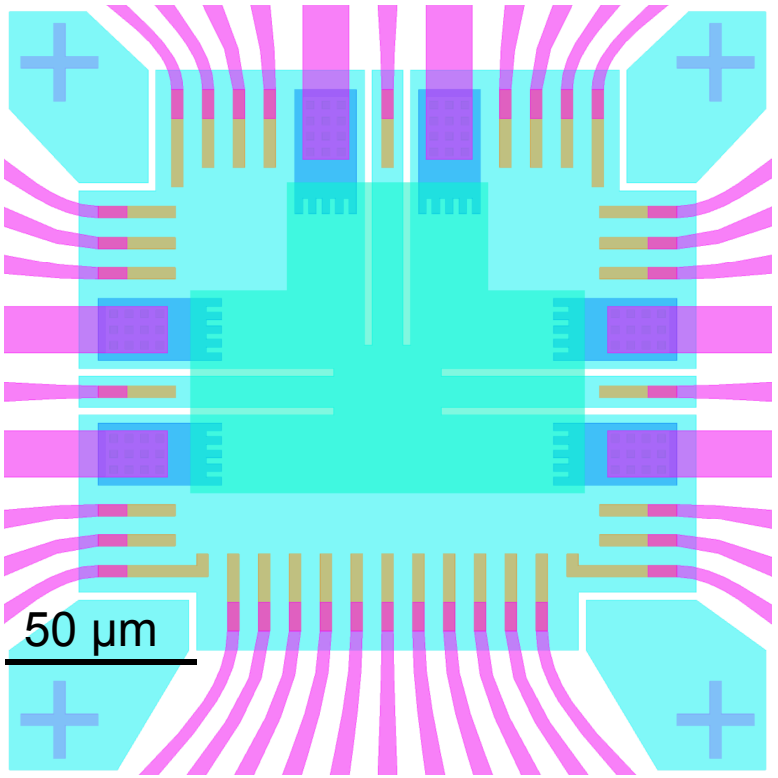
Building library of standard device elements

- Ohmics
- Alignment
- Bond Pads

Common design rules enable rapid die layout to meet team members needs.

Nanostructure Die Design
Closed Device Layouts

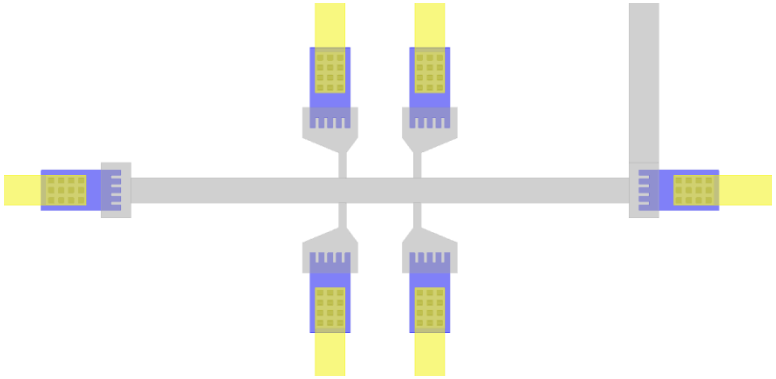




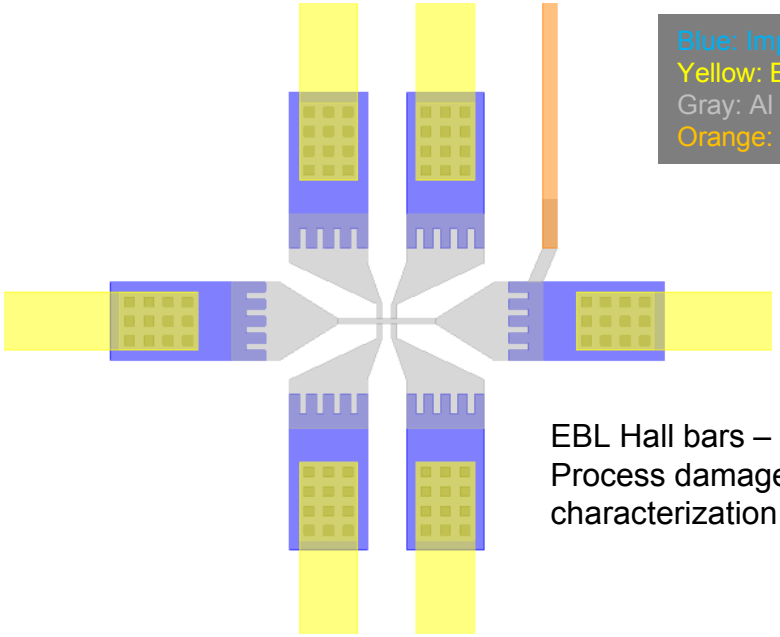
- Reuse of elements for rapid die development
- Use of known elements reduces risk in future designs – Proven designs

- Additional leads added to enable more complicated future devices
- Extra leads can be used now as diagnostics and to provide redundant functionality to improve yield

Diagnostic Die Structures



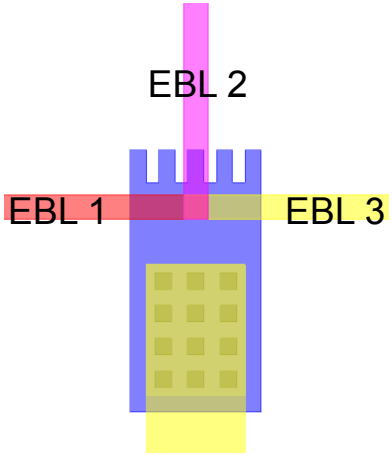
Optical litho Hall bars – Material characterization



EBL Hall bars – Process damage characterization

Ohmic tester – Electrical characterization

RF CPW tester – Materials and electrical characterization



Dielectric tester – Leakage testing between multiple EBL patterned gate layers and ohmics

Wafer Level Fabrication Process

1. **Starting Material**
2. Sacrificial Oxide Deposition (Low T CVD)
3. Si Marker Etch (CF4)
4. Ion implant (Arsenic)
5. Oxide Strip (BOE)
6. Gate Oxide Deposition (ALD, Al2O3)
7. SiN Deposition (CVD)
8. Field Oxide (Low T CVD, SiO2)
9. Alignment Marks (W)
10. Window Etch (HF)
11. Optical to EBL jumpers (W)
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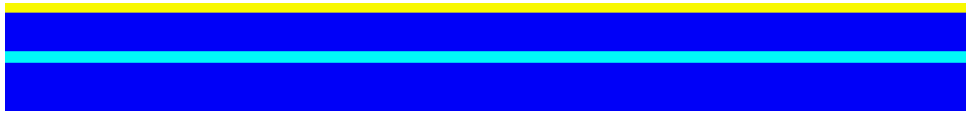

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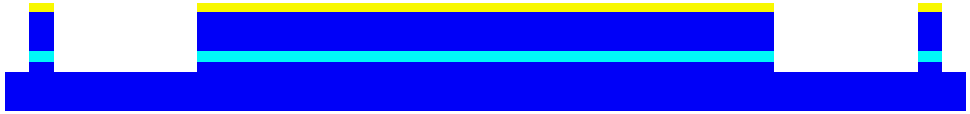

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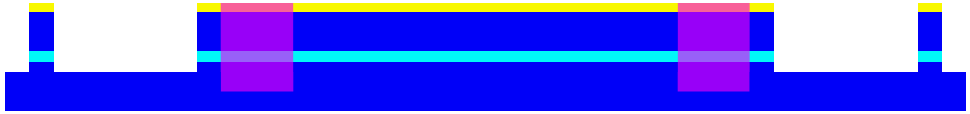

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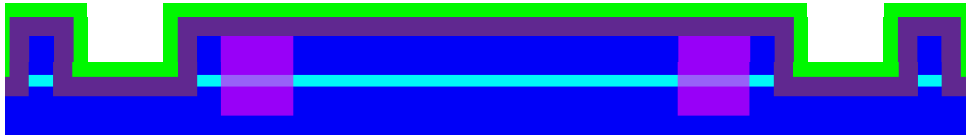

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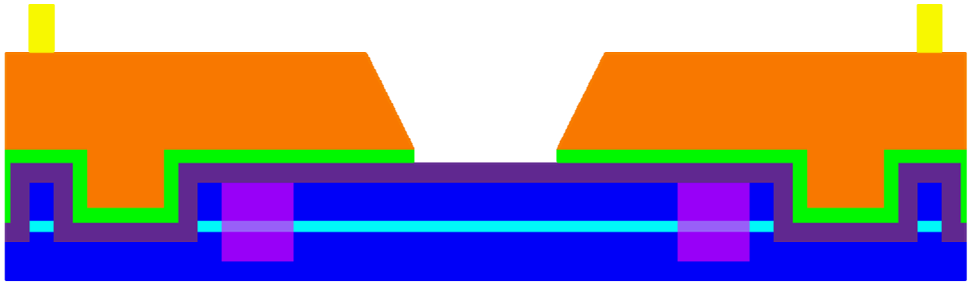

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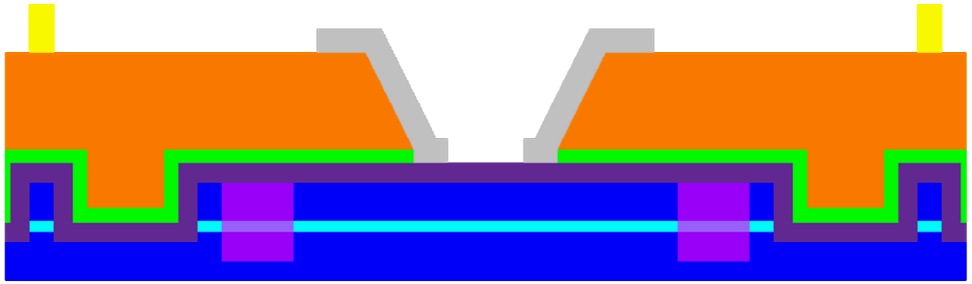

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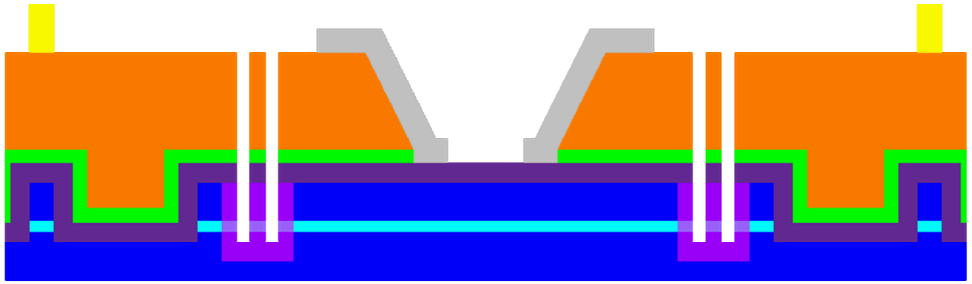

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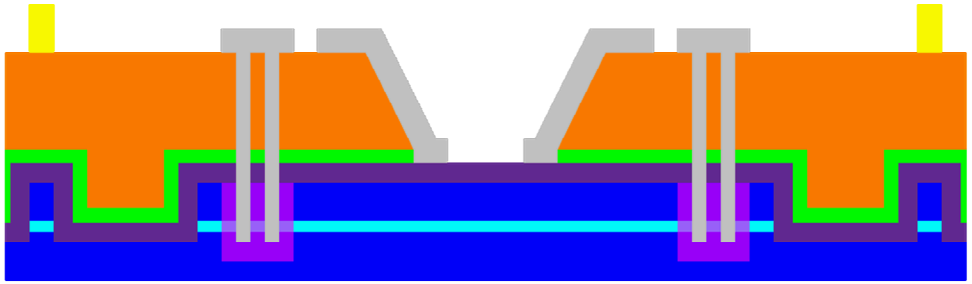

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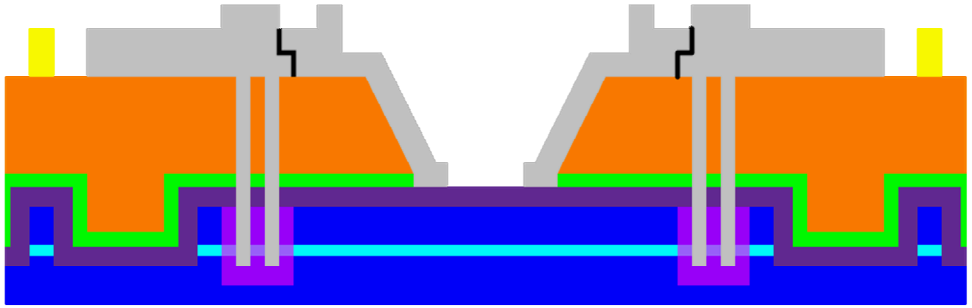
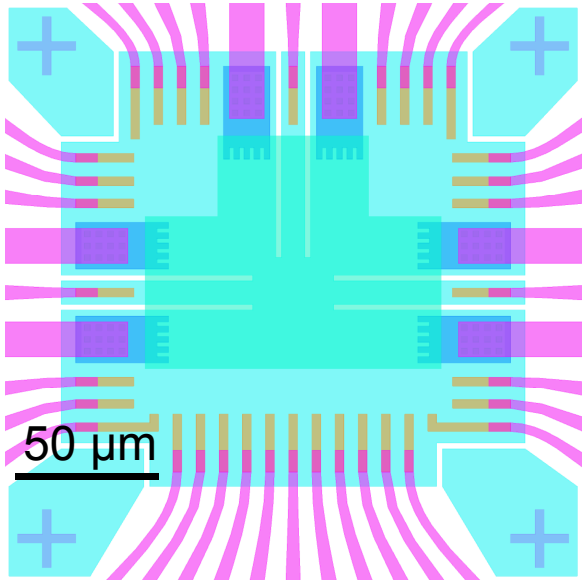


Summary

- Fabricating quadruple quantum dots for all team members
  - Stretch goal extending fabrication to 6 quantum dots
  - Designing to specific requirements of each team member
  - Material optimization
  - Wafer level fabrication of starting materials



- Timeline
  - First wafers through fabrication in October
  - First nanostructure devices deliver in November