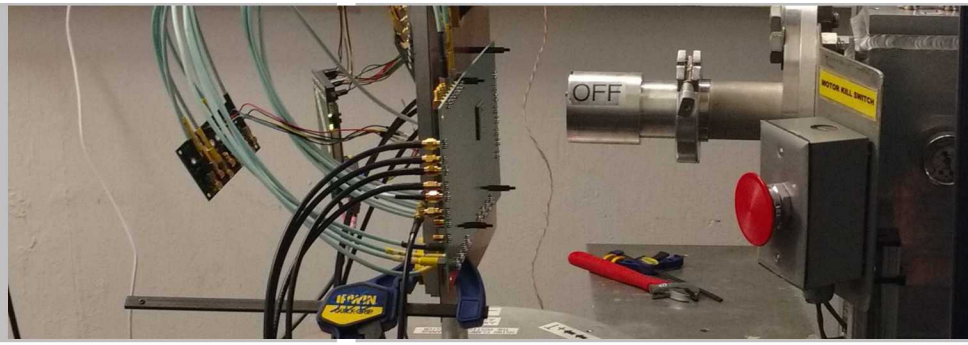
SAND2018-2901PE



Heavy-Ion Irradiation of the Xilinx Kintex UltraScale+ FPGA

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Overview

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- Device Properties
- Test Description
- Results
  - SEU
  - MCU
  - SEL
- Conclusion

Background: UltraScale+

- In early 2017, Xilinx began the first customer shipments of UltraScale+ parts
  - Highly anticipated due to 16 nm TSMC FinFET technology
  - Started with Zynq MPSoC devices; FPGA fabric-only devices followed shortly thereafter
  - Expected significant improvement in SEU response

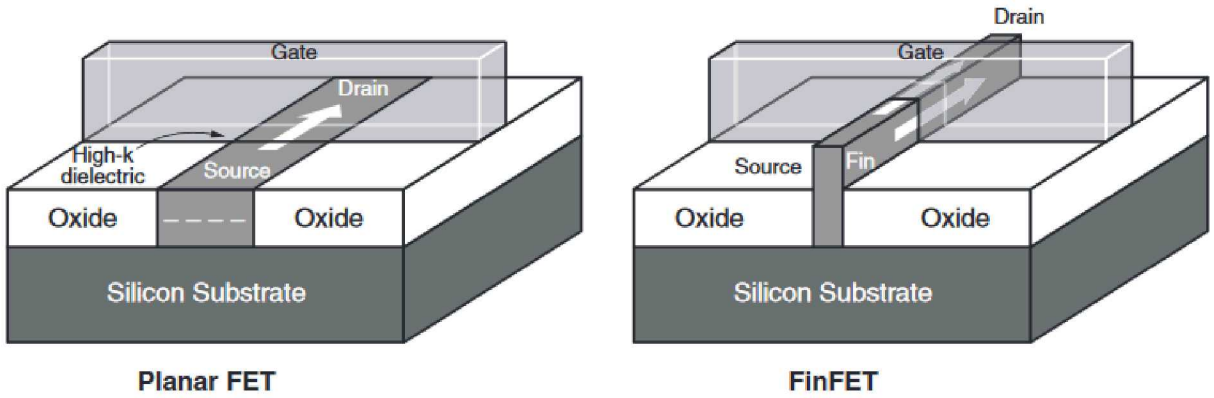


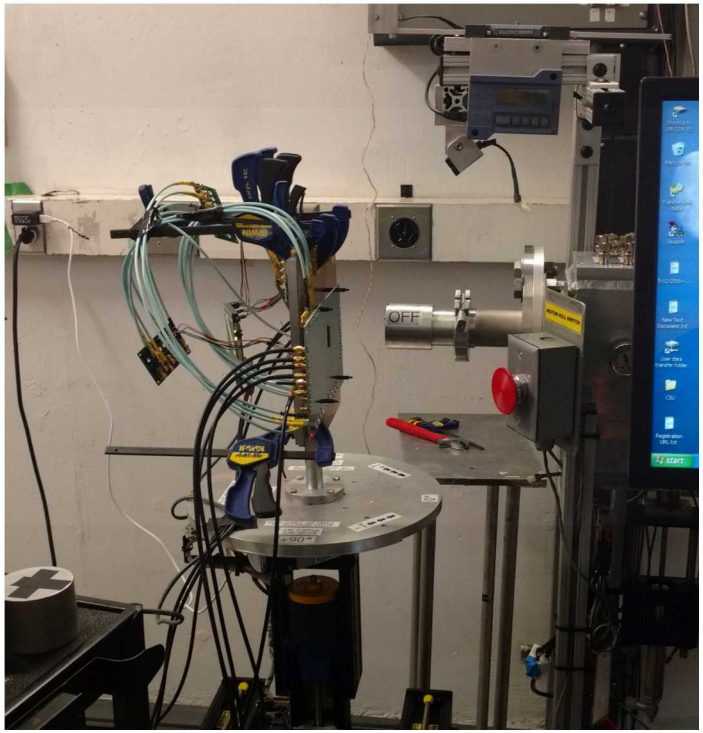
Image from Xilinx, Inc., WP472.

Device Overview

- An evaluation of the radiation response of this device family was desired to evaluate new FinFET processes
- Device-Under-Test selected was the Kintex UltraScale+ FPGA
  - FPGA Fabric-only device (no processors)
  - XCKU9P-1FFVE900E-ES2
  - 212,086,240 configuration bits
  - 548,160 Flip-flops
  - 274,080 Look-up Tables
  - 32.1 Mbit BlockRAM (912 @ 36Kb)
  - 4 CMT Tiles
  - 2,520 DSP Blocks
  - 28 GTH Transceivers

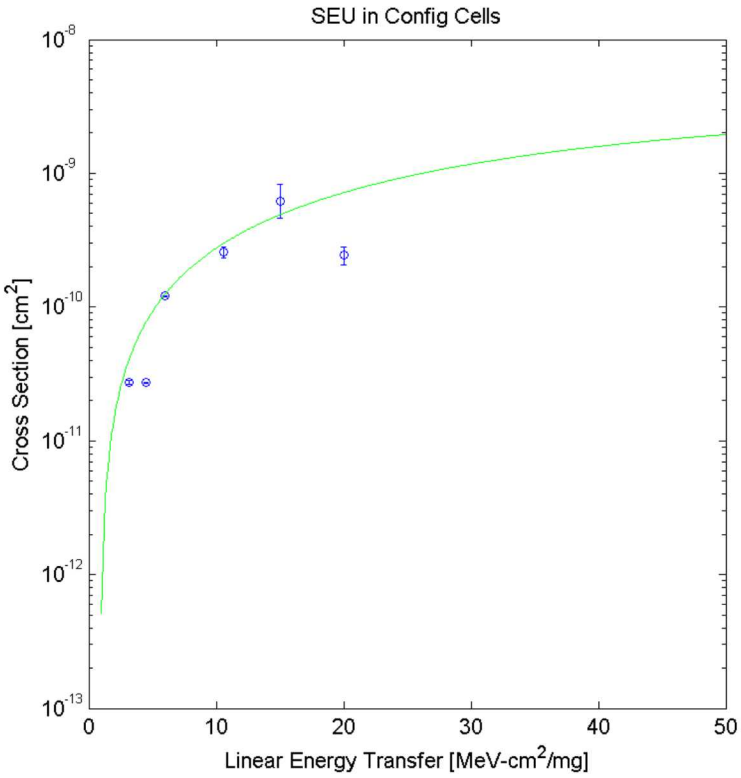
Test Description

- Testing was performed at the Texas A&M K500 Cyclotron in May of 2017
  - Irradiated with Argon and Neon, LET range of 3.2 to 20.1 MeV-cm^2/mg
  - Data shown in this presentation reflects irradiations at normal incidence only
- Device was programmed with a static design (pre-initialized flip-flop shift registers and BlockRAM, no running clock)
- Scrubbing and readback operations were performed with the BYU JCM using the JTAG interface



SEU Results

- The unmasked configuration bits were analyzed for SEU (approximately 118.6M bits)
- Bits storing “0” values tend to upset more often than bits storing “1” by a ratio of ~4:1
- Space rate for GEO orbit, solar minimum, 0.1” Al shielding:
  - 0.28 SEU/device/day (all 212M bits)



SEU Discussion

- FinFET SEU performance is excellent compared to previous generations

	Configuration Memory Rates			Weibull Parameters			
	per bit, per day	Improve-ment*	Node	Onset (MeV-cm^2/mg)	Limit (cm^2/bit)	Width (MeV-cm^2/mg)	Power
Virtex-II	3.99E-07	1	130 nm	1	4.37E-08	33	0.8
Virtex-4	2.63E-07	1.517	90 nm	0.2	1.76E-07	400	0.98
Kintex-7	1.41E-08	28.298	28 nm	1.9	1.43E-08	125	0.8
UltraScale	7.56E-09	52.778	20 nm	0.8	2.00E-09	27	0.88
UltraScale+	1.33E-09	300.000	16 nm	0.9	3.13E-09	50	1.4

** compared to Virtex-II*

Other Data sources:

[Virtex-2] R. Koga, J. George, G. Swift, C. Yui, L. Edmonds, C. Carmichael, T. Langley, P. Murray, K. Lanes, and M. Napier, "Comparison of Xilinx Virtex-II FPGA SEE sensitivities to protons and heavy ions," *Nuclear Science, IEEE Transactions on,* vol. 51, no. 5, pp. 2825-2833, 2004.

[Virtex-4] G. Allen, G. Swift, C. Carmichael, C. Tseng, and G. Miller, "Upset measurements on Mil/Aero Virtex-4 FPGAs incorporating 90 nm features and a thin epitaxial layer."

Multiple-Cell Upset

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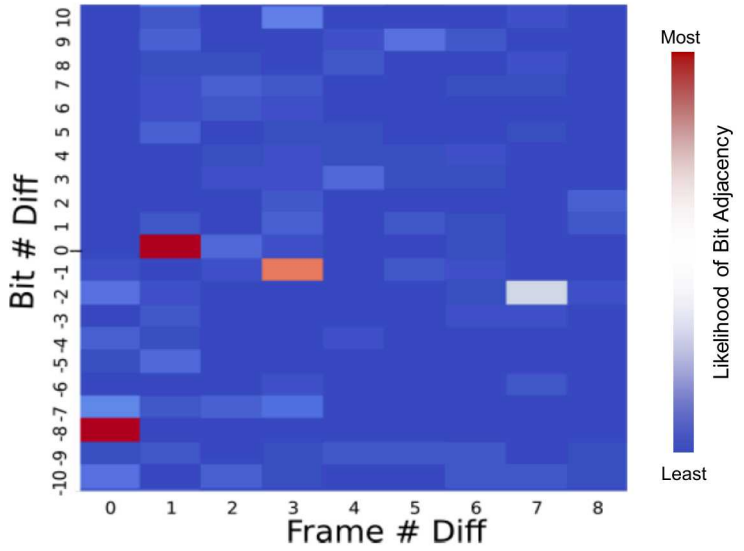
- Multiple-Cell Upsets (MCUs) are a concern in highly scaled technologies due to smaller distance between memory cells
  - MCU occurs when a single particle causes two or more physically adjacent cells to upset
  - Evaluated by technique in (1), citation below
- An Error-Correcting Code (ECC) is present in configuration memory frames
  - Configuration frames in UltraScale+ are 2,976 bits and are the smallest addressable memory unit
  - Previous families utilized single-error correct, double-error detect ECC; UltraScale+ appears to have the same scheme (?)

[1] *M. Wirthlin, D. Lee, G. Swift and H. Quinn, "A Method and Case Study on Identifying Physically Adjacent Multiple-Cell Upsets Using 28-nm, Interleaved and SECDED-Protected Arrays," in IEEE Transactions on Nuclear Science, vol. 61, no. 6, pp. 3080-3087, Dec. 2014. doi: 10.1109/TNS.2014.2366913*

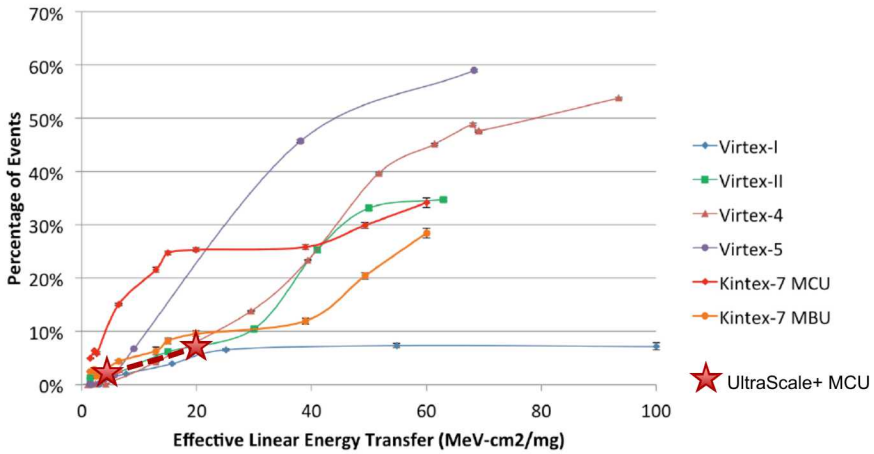
MCU Results

- Heat map on right shows which bits have a high probability of adjacency
- MCUs comprise ~7% of events at the higher LETs used in this test (table below)
- When compared to historical MCU data from previous generations, MCU response is excellent



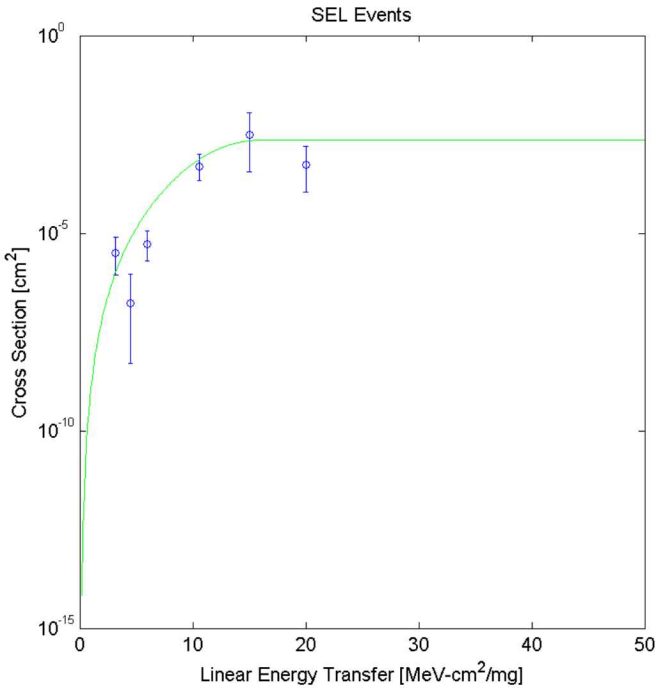
PERCENTAGES OF MCUS EXTRACTED FOR ARGON AND NEON IONS.

	MCU Shapes							
ion	(1,0)	(0,-8)	(7,-2)	(3,-1)	(0,-8),(0,-8)	(1,0),(1,0)	(1,0),(3,-1)	total upsets
Ar	4.89%	0.67%	0.57%	0.67%	0.19%	0.00%	0.10%	**1044**
Ne	0.41%	0.68%	0.06%	0.11%	0.11%	0.00%	0.00%	**70305**



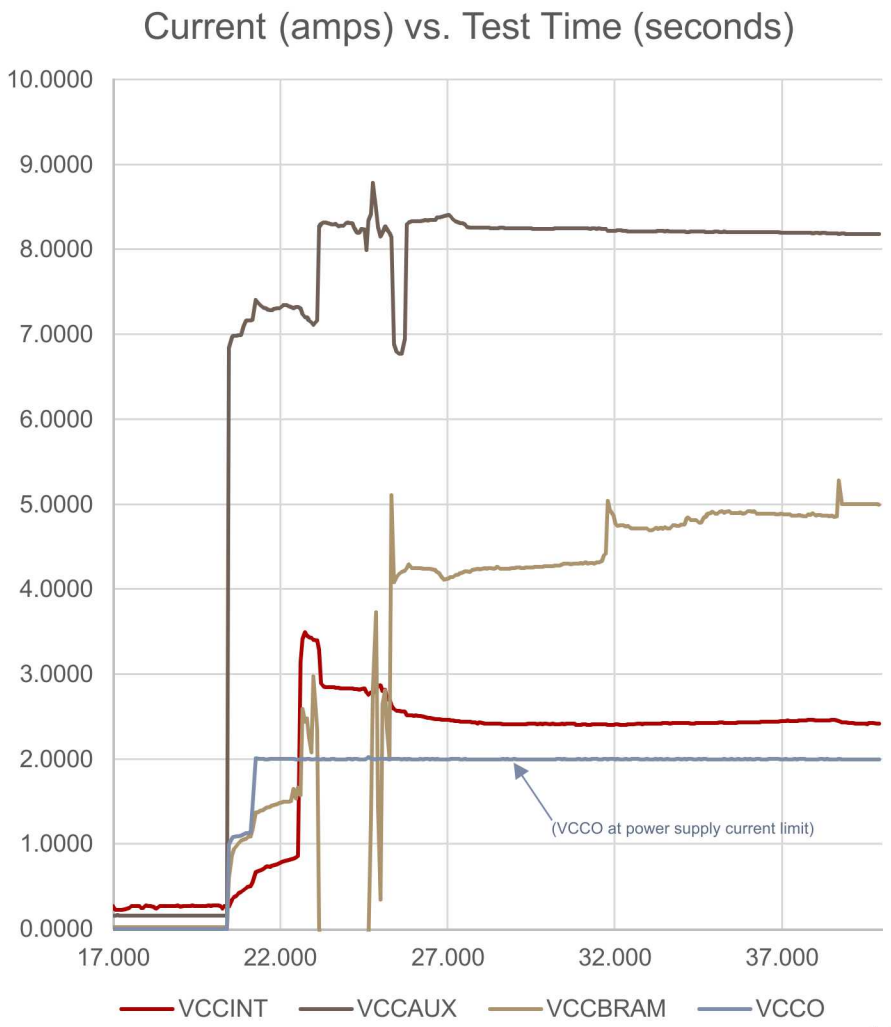
SEL Results

- Single-Event Latch-Up was observed at LET of 3.2 MeV-cm^2/mg at ambient temperature and normal voltage biases
  - LET threshold may be lower; testing was not performed below this LET
- Space rate for GEO orbit, solar minimum, 0.1” Al shielding:
  - 0.0097 SEL event per day (= 1 event approximately every 103 days)
- VCCAUX was the primary culprit
  - Latch-up-like behavior on other rails was observed, but always happened following a SEL on VCCAUX (probably due to die temperature increase)



SEL Discussion

- Current jumps observed from SEL ranged from hundreds of milliamps to several amps
- Destructive event observed occurred when multiple latch-up sites were allowed to collect in the device
  - Unlike 7-series "μSEL"
  - Graph on the right shows one example of this, where SEL sites were allowed to collect



Conclusion

- Need to complete data analysis on the existing data set:
  - Flip-flop and BlockRAM upset analysis
- Additional SEU and SEL investigations for future beam tests:
  - Angular studies (rotation and tilt)
  - Further investigation of SEL and SEL mitigation
- In summary:
  - SEU performance of this device family is excellent
  - MCU performance is very acceptable
  - Unfortunately, SEL is too significant for high-reliability missions