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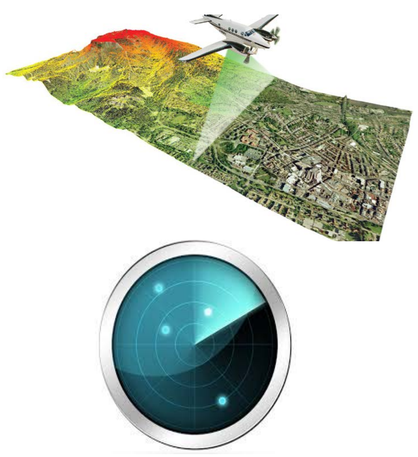
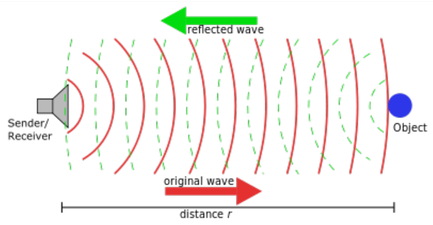
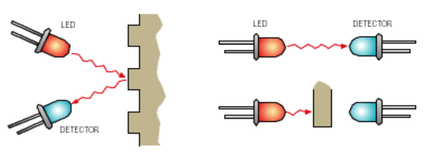
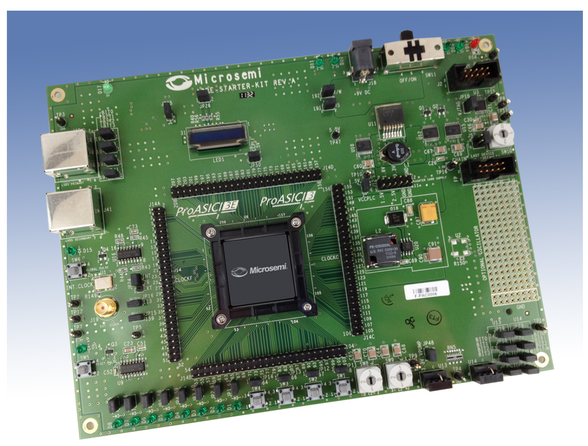








Digital femtosecond time difference circuit for CERN's timing system.

P. Moreira † and I. Darwazeh †

† University College London

Abstract: This paper presents a novel digital circuit, based on the analog Dual Mixer Time Difference circuit, developed by David W. Allan, designed to characterise oscillators frequency stability. The proposed digital circuit, named Digital Dual Mixer Time Difference (DDMTD), is capable of measuring time differences between two digital clock signals with very fine resolution (subpicosecond) using a relative low frequency counter.

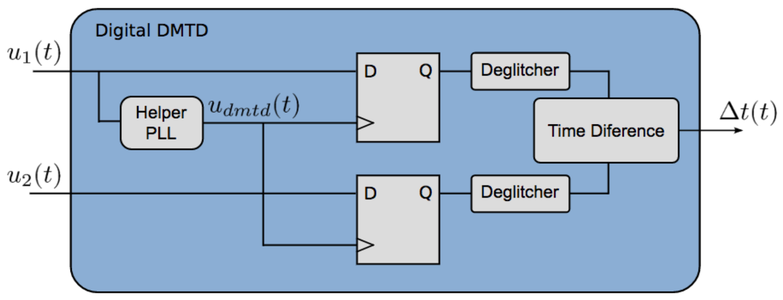
Digital Dual Mixer Time Difference Circuit

Dustin Tso, Sarina Kapai: Electrical Engineering, USC
Robert J. Mariano, Marc R. Feldman, 8736
Sandia National Laboratories, U.S. Department of Energy
7/24/2017

Introduction:

D-DMTD is a digital phase detector, capable of measuring the time difference between two digital clock signals with high resolution (sub-picosecond) using a relatively low frequency counter. Our project applies the design theorized by the white paper, *Digital femtosecond time difference circuit for CERN's timing system* by P. Moreira to a digital system, programmed onto a Microsemi ProASIC3E FPGA.

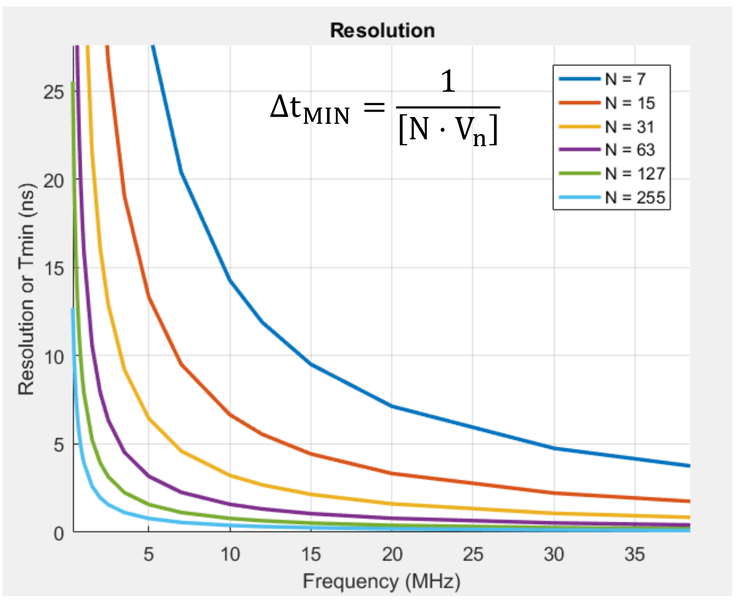
Design:



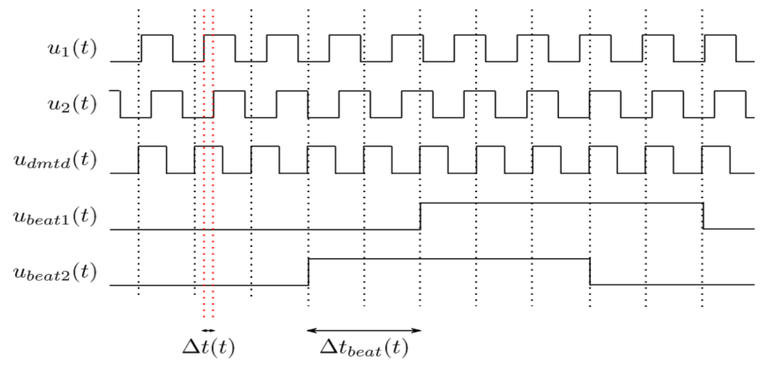
The design consists of two input digital clock signals—$u_1(t)$ and $u_2(t)$—both of which have a frequency of v_n and a relative phase difference of Δt. The Helper PLL is set by the user at a specific frequency to produce the $u_{dmtd}(t)$ clock signal. To specify v_{dmtd} use the following formula:

$$v_{dmtd} = \left[\frac{N}{N+1}\right] v_N$$

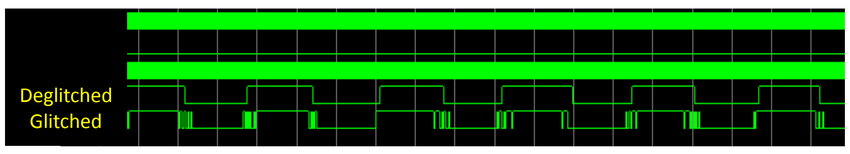
Selection of N:



Beating Two Signals:



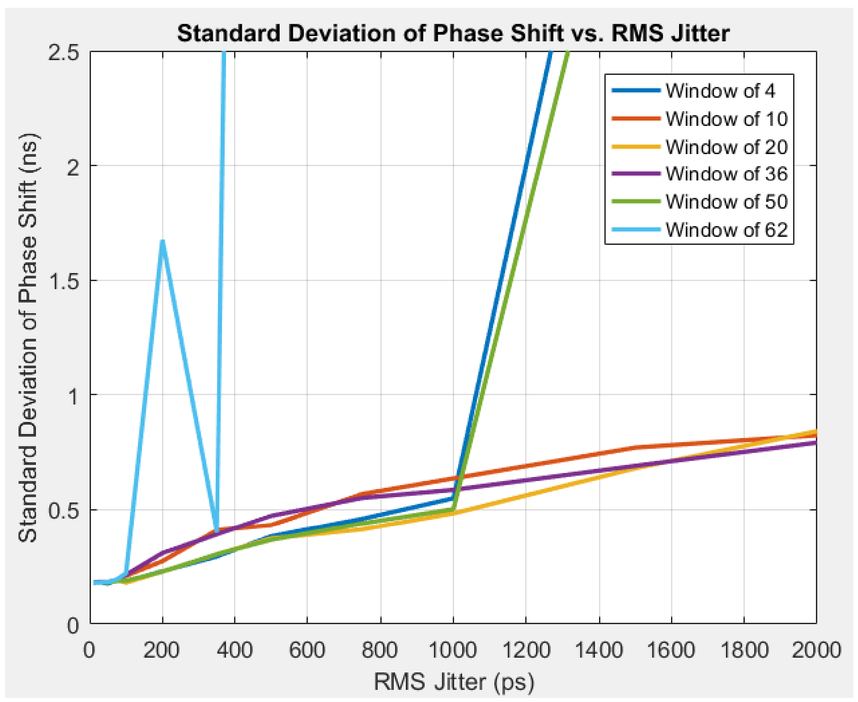
Deglitching Mechanism:



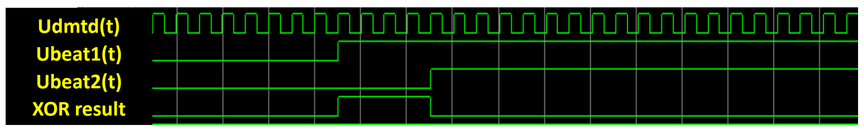
*This image was generated by ModelSim.

The deglitcher algorithm uses a shifting array that takes in a new value from $u_1(t)$ or $u_2(t)$ on every rising edge of $u_{dmtd}(t)$, continuously evaluating whether the number of ones and zeros in the array are equal. When this happens, the algorithm initiates a transition in the output signal—a one switches to a zero, or zero switches to a one. The foundation of this algorithm was briefly introduced in the white paper.

Selection of Window Size:



XORing the Beat Signals:



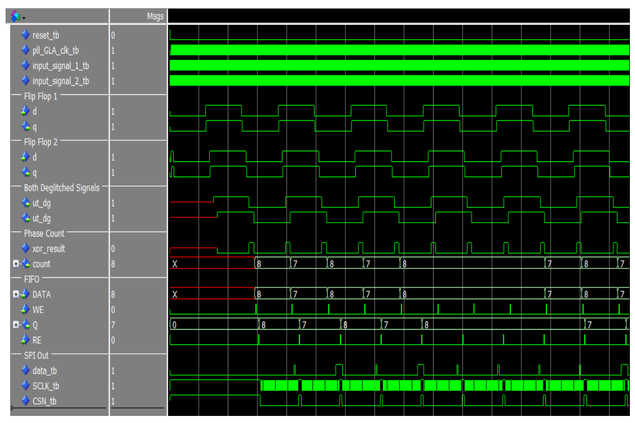
In the figure above, the XOR result is '1' for 4 clock periods of $u_{dmtd}(t)$, each of which lasts 50.394 ns (based on 20 MHz input signals). We refer to this XOR result as 'count'.

$$\Delta t = \Delta t_{beat}\left(\frac{v_{beat}}{v_n}\right) = (\Delta t_{beat})\left[1 - \left(\frac{N}{N+1}\right)\right]$$

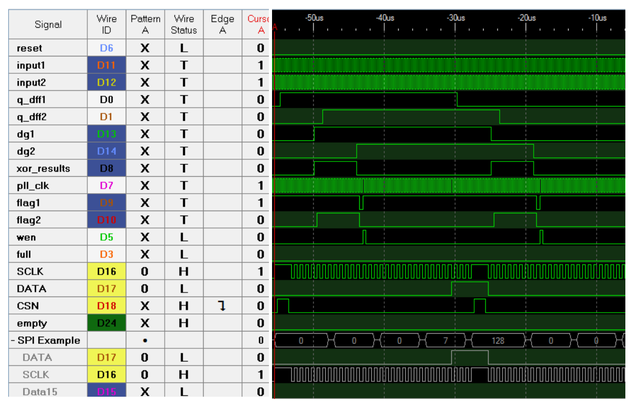
With 'count' = 4, our Δt_{beat} value is 4 * 50.394 ns = 201.576 ns. With the equation above, we get 1.5748125 ns for the phase shift between the original two signals $u_1(t)$ and $u_2(t)$. The simulations set $u_1(t)$ and $u_2(t)$ to have a relative phase shift of 1.3 ns, and so our estimation of 1.5748125 ns is slightly off.

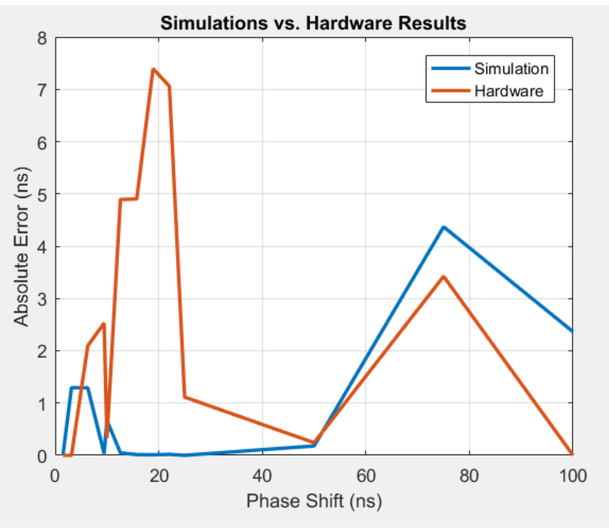
Testing:

SPI Interface:



Results and Analysis:





Variable Index

DMTD	dual mixer time difference
Δt(t) or Δt	Phase shift between two digital clock signals; represents time between two initial trigger events
ΔtMIN	The minimum phase shift we can detect between two digital clock signals; measure of resolution
N	Variable that establishes ratio between vn and vbeat
U1(t)	Input signal with frequency vn
U2(t)	Input signal with frequency vn; phase shifted relative to U1(t)
Udmtd(t)	Clock signal that samples u1(t) and u2(t); set at a slightly lower frequency to spread out two signals
U1beat(t)	Result of passing U1(t) through d-flip-flops; stretched out in time domain
U2beat(t)	Result of passing U2(t) through d-flip-flops; stretched out in time domain
Vn	Frequency of input signals: U1(t) and U2(t)
Vbeat	Frequency of beat signals: U1beat(t) and U2beat(t)
Vdmtd	Frequency of Udmtd(t); slightly less than Vn

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