SAND2017-7580C

New Methods for Rapid Time-Series Analysis

Panel Session: Advances in Accelerated Distribution System Time-Series Analysis

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Outline

Overview of a couple new methods for Rapid QSTS

1. Variable Time-Step Methods
   - Predetermined Time-Step
   - Causal Variable Time-Step: Backtrack
2. Circuit Reduction
3. Sampling Partial Year

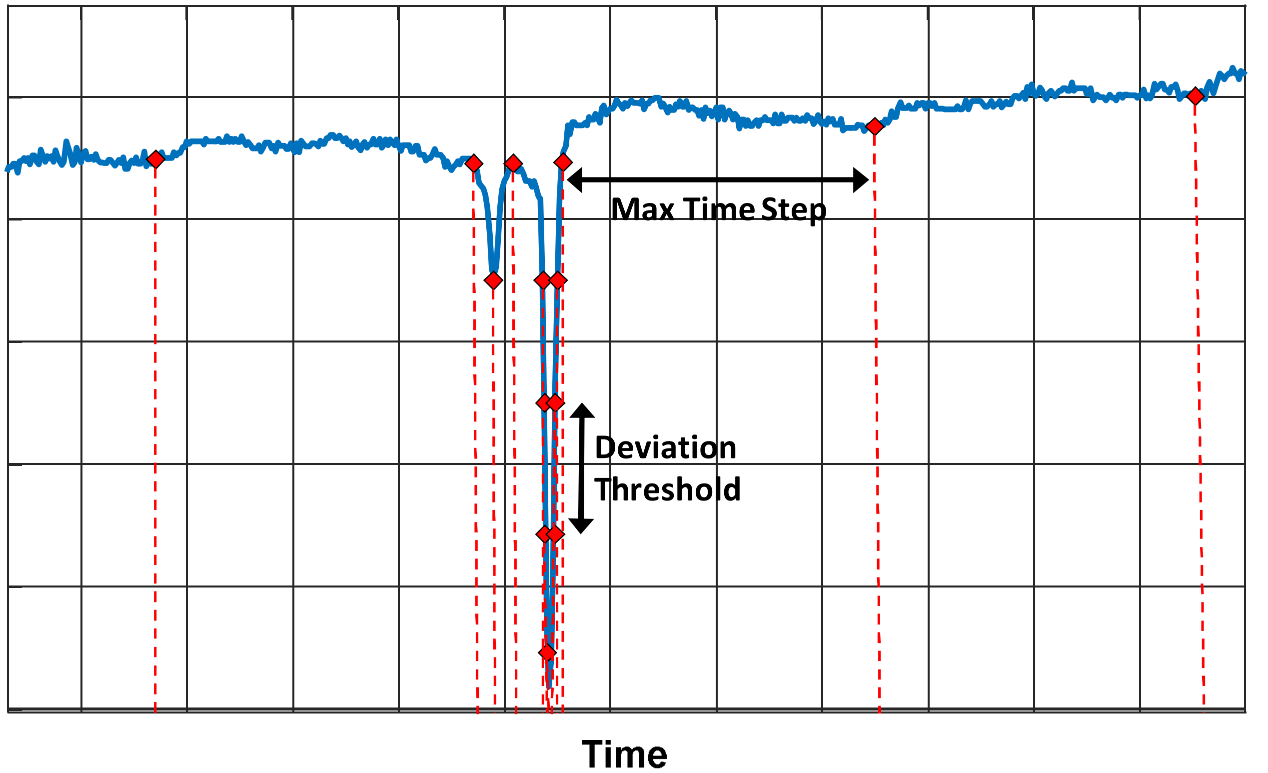
Variable Time-Step

Objective:

- Reduce the computational burden by adjusting the QSTS time-step to solve fewer load flows
- Variable time-step solver does not solve every time-step and skips forward to time points of interest, advancing through the QSTS analysis with varying time-steps
- Two different methods to calculate step-size:
  - Input Variables: preprocesses the load and generation time-series data in order to define the time-steps
  - Output Variables: Causal solver adjusts the time-step using data from previous power flow
- Possible to combine the two methods

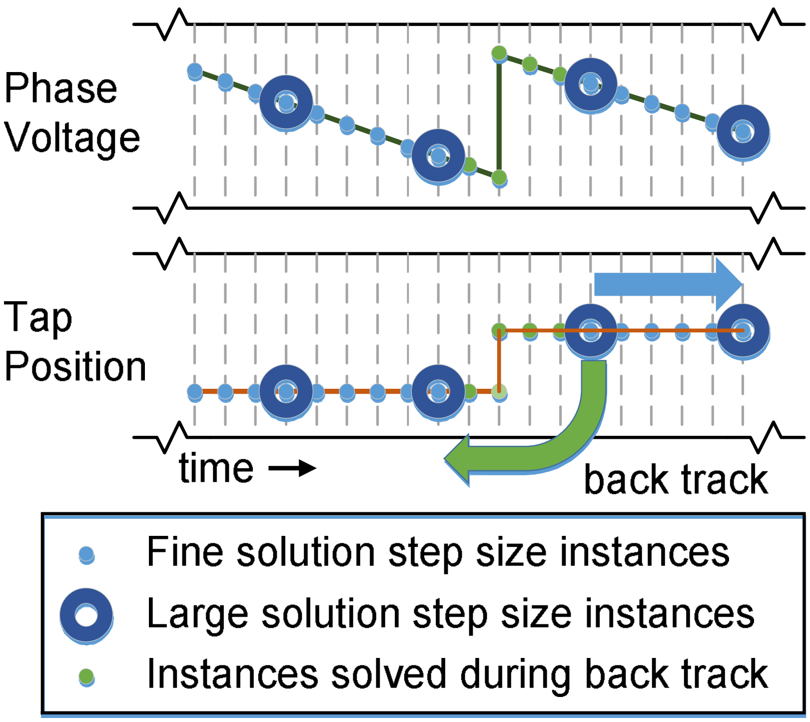
Variable Time-Step (Input Variables)

- Predetermined time-steps by preprocessing the load and generation time-series data. Only requires the input data (no interaction with the power flow solver)
- This type of variable time-step solver has two tuning parameters (max time-step and deviation threshold)



Variable Time-Step (Output Variables)

- Backtrack method employs two time-step sizes (large and small)
- Large time-steps are taken until a change in the automatic voltage regulation state is detected
- Upon detection, the solution backtracks to the last known time point with no state changes and small time-steps are taken to resolve the potential control actions



Utilizes the implemented control delay as a window to detect automatic voltage regulation device operation

Variable Time-Step (Input AND Output)

- The variable time-step using input and output variables can be combined for additional speed
  1. First determine the variable time-steps using the input variables (power deviation threshold and maximum allowed time-step)
  2. Run QSTS jumping between predetermined time-steps. If during a power flow solve an event is detected, backtrack to the previous predetermined time-step and runs the simulation at high resolution.

Deviation Threshold (kW)	Max Time Step (s)	Tap Changes Per Regulator	Capacitor Switches	Percent Reduction	Times Faster
Base Case		7048,7222,8449	2504		
100	180	-5.8%, -5.8%, -6.1%	-7.0%	97.0%	32.9x

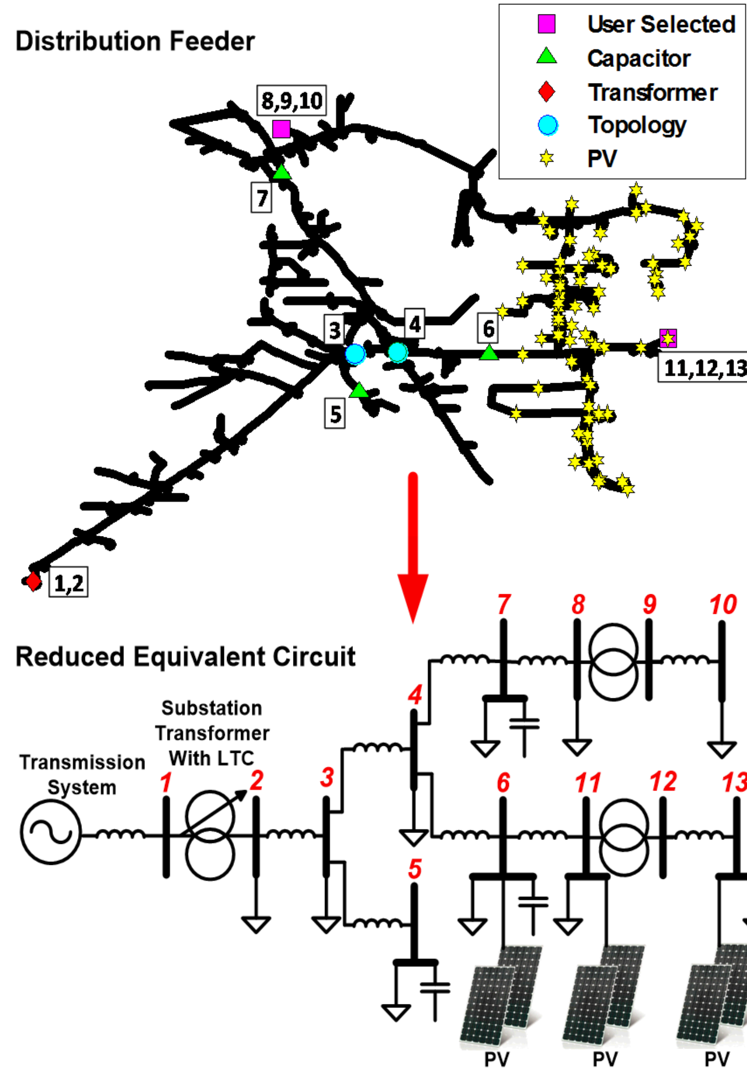
Circuit Reduction

Objective:

– Use an equivalent reduced circuit with fewer buses to decrease the power flow simulation time

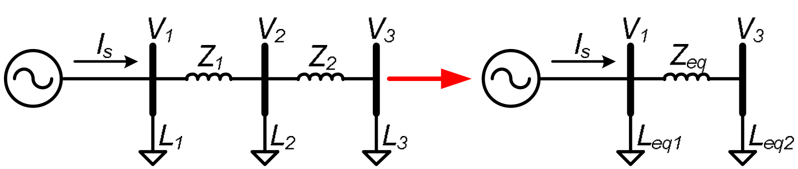
Solution:

– Many buses can be removed or aggregated into nearby buses, while keeping the results for the remaining buses equivalent

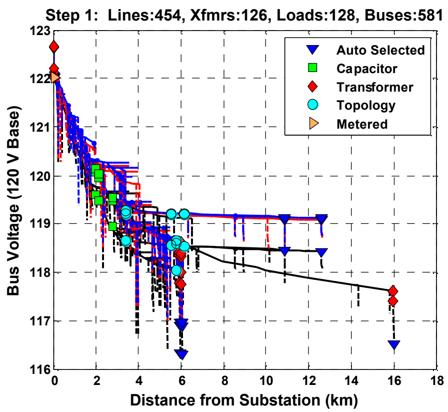
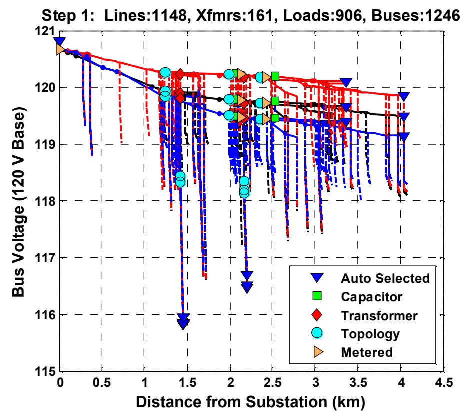
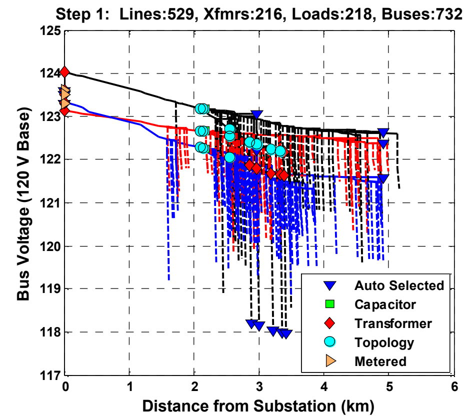
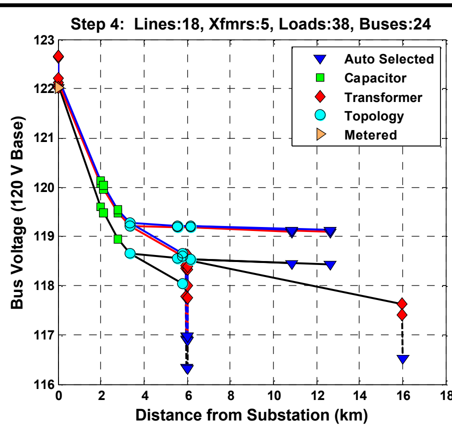
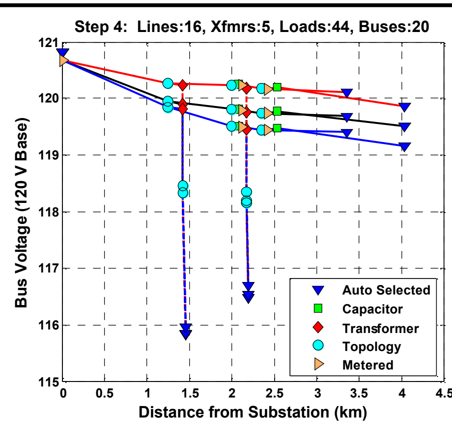
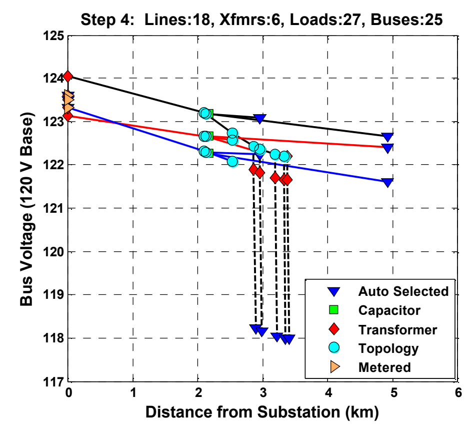


Circuit Reduction

- Reduction algorithms can handle unbalanced loads and PV, unbalanced and unsymmetrical wire impedance, mutual coupling, shunt capacitance, transformer magnetizing currents, and multiple different load profiles and PV power profiles.
- With certain assumptions, the results are exactly equivalent for the reduced circuit
- Steps:
  1) Select buses to keep
  2) Remove buses without objects (Kron reduction)
  3) Remove unnecessary laterals (Norton equivalents)
  4) Load Bus Reduction

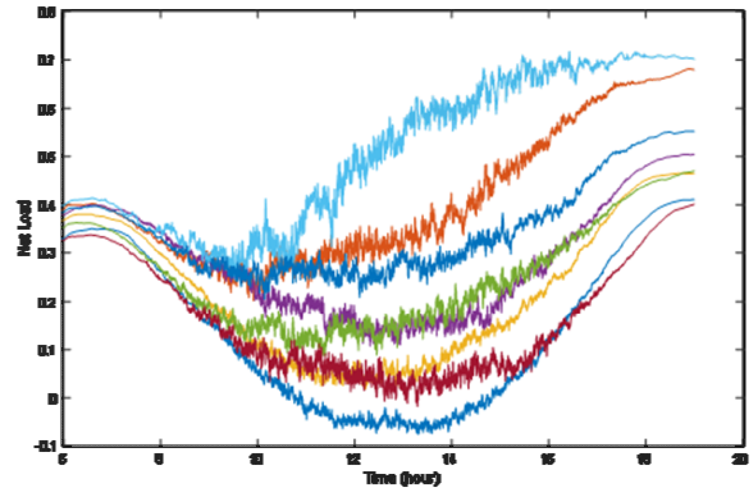


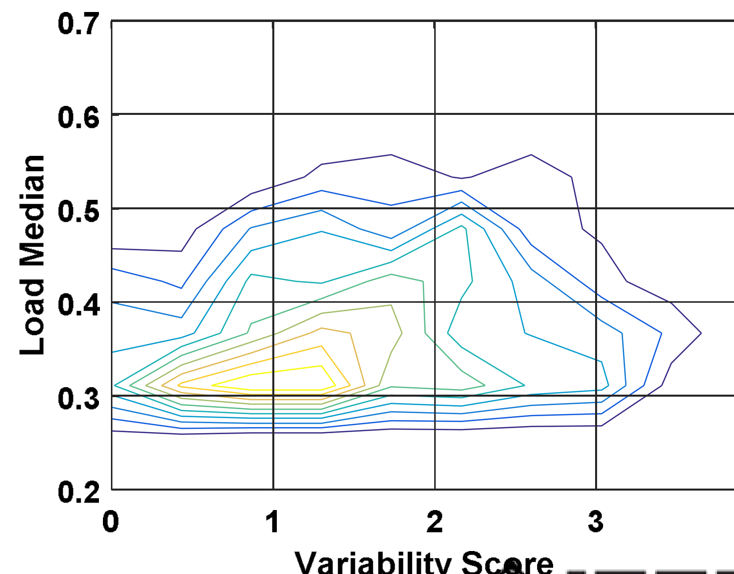
Circuit Reduction Results

	Feeder UT11 96% Reduction <0.01% Error	Feeder Ckt 7 98% Reduction <0.02% Error	Feeder UQ11 97% Reduction <0.02% Error
Full			
Reduced			

Intelligent Sample Selection

- **<u>Objective:</u>**
  - Run QSTS on most effective sample periods of the year and reconstruct the annual simulation results
- **<u>Many ways to select samples intelligently:</u>**
  - Clustering days (top figure)
  - Stratified sampling (bottom figure).
- **<u>Stratified sampling</u>** has shown good results, grouping periods based on their median load and PV variability score.



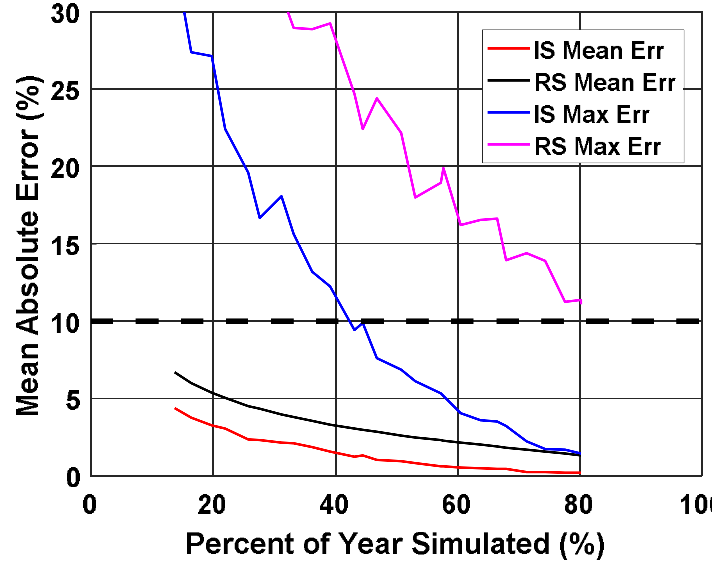


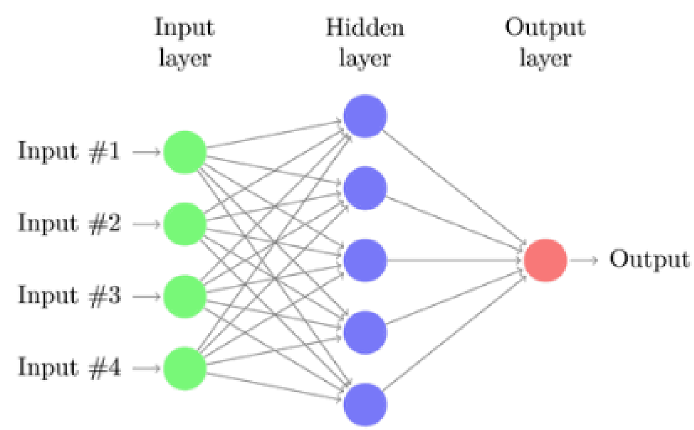
Intelligent Sample Selection

- For a Monte Carlo simulation with 100,000 iterations, the intelligent sampling (IS) is compared to random sampling (RS) in the top figure.

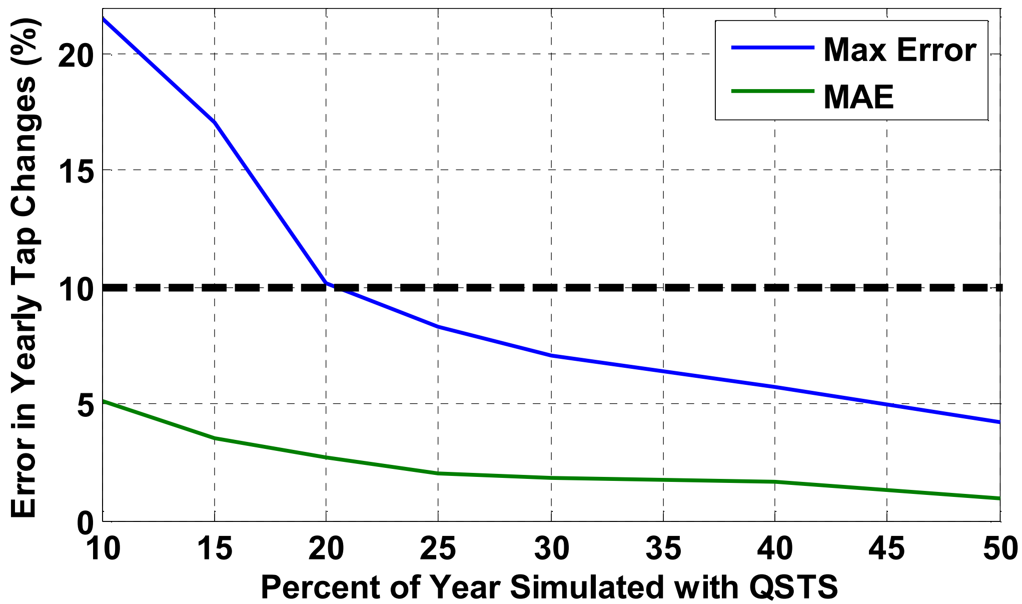
- Randomly sampling time periods from the year to perform QSTS simulations can occasionally have a significant bias because only specific types of days (e.g. only clear sky days, or only winter days) are sampled

- Additional accuracy can be achieved by using the intelligently sampled periods as training data in a neural network to learn and predict the number of tap changes for the rest of the year.





Intelligent Sampling With Machine Learning



- Statistical techniques provide a confidence interval for the metrics, so more of the year can continue to be run with QSTS until allowable error thresholds are met.
- By simulating more of the year with QSTS, the training data size and accuracy is increased, but additional computational time is required for running the longer QSTS simulation.

Conclusions

- Compared to a normal brute-force QSTS simulation at 1-second resolution for a year:
  - Variable time-step is 30x faster by skipping through time during low variability periods
  - Circuit reduction is 10-50x faster by reducing the computational time of each power flow
  - Intelligent sampling is 5x faster by selecting representative parts of the year to solve

QUESTIONS?

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