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Design and characterization of an improved, 2 ns, multi-frame imager for the Ultra-Fast X-ray Imager (UXI) program at Sandia National Laboratories

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ABSTRACT

The Icarus camera is an improvement on past imagers (Furi and Hippogriff) designed for the Ultra-Fast X-ray Imager (UXI) program to deliver ultra-fast, time-gated, multi-frame image sets for High Energy Density Physics (HEDP) experiments. Icarus is a 1024 x 512 pixel array with 25 μm spatial resolution containing 4 frames of storage per pixel. It has improved timing generation and distribution components and has achieved 2 ns time gating. Design improvements and initial characterization and performance results will be discussed.

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1. INTRODUCTION

High Energy Density Physics (HEDP) experiments evolve on an extremely fast time scale, with events of interest lasting only a few nanoseconds. This presents significant challenges to developing diagnostic sensors that are capable of operating at these speeds. Two dimensional, multi-frame imagers have the potential to provide significant insight into HEDP experiments if the challenging temporal requirements can be met.

Current diagnostics often utilize streak cameras, which have excellent temporal resolution, but are limited to a single spatial dimension. Micro Channel Plate (MCP) detectors are capable of providing two-dimensional data, but suffer from a number of limitations including limited dynamic range, gain errors, and difficulty in maintaining calibration. Additionally, MCPs are limited to a single frame of data for a given line-of-sight. CMOS imager technology designed specifically to accommodate HEDP requirements has the potential to overcome many of the limitations existing diagnostics exhibit.

Continuous operation of a nanosecond shuttered camera for a large-scale imager of would yield a prohibitive amount of data. A 1024 x 1024 pixel camera operated at 1 billion frames-per-second produces 1.3 Petabytes of data per second, requiring a read-off bandwidth that is unattainable with current camera technology. To avoid these readout speed limitations, burst-mode imagers capture multiple frames of image data on a fast time scale using MOSFET switches as electronic shutters, store these frames in-situ on in-pixel storage elements, and then read the image data off on a slower timescale. This type of camera can deliver the speeds required for ultra-fast timescale experiments for a limited number of frames, typically dictated by how many memory elements can be fit into a given pixel spatial resolution.

The Ultra-fast X-ray Imager (UXI) program at Sandia National Laboratories has pursued burst mode, hybrid CMOS imager development to augment existing HEDP diagnostics. Hybrid imagers incur additional cost and complexity versus monolithic CMOS cameras; however, hybrid cameras enable independent development of the Read-Out Integrated Circuit (ROIC) and photodiode array (PD). This facilitates the design of diagnostic-specific PD arrays that can be mated to previously characterized ROICs.

Two previous imagers developed by the UXI program, Furi [1] and Hippogriff [2], have demonstrated time gates of around two nanoseconds for two frames of native pixel storage [3] and up to eight frames in a spatial-temporal interlacing mode [2]. These cameras have yielded positive results at both the Sandia National Laboratories' Z-machine as well as the National Ignition Facility at Lawrence Livermore National Laboratories [4, 5]. The Icarus camera presented here is a follow-on design focused on improving performance over the previous Furi and Hippogriff cameras. These cameras are the fastest CMOS X-ray imagers demonstrated to date [6].

2. ICARUS ARCHITECTURE

Conceptually, the Icarus architecture is similar to the proven Furi and Hippogriff cameras, but Icarus incorporates numerous minor circuit modifications and significant improvements to the physical design intended to mitigate issues discovered in prior cameras.

As with prior cameras, upon receiving an external asynchronous trigger, Icarus will generate four pre-programmed high speed shutter pulses, distribute these shutter pulses to the pixel array, and capture four independent images that are stored in-situ and then read out on a slower timescale.

Icarus has a slightly larger pixel array, increasing the number of columns from 448 to 512 for a final array size of 1024 x 512 pixels while maintaining the same 25 μm pitch as past cameras. The pixel storage has been increased from two frames used in previous designs to four frames at the expense of reducing pixel full well from 1.5 million e^- to 500 thousand e^-. The minimum integration time of approximately two nanoseconds was maintained. Figure 1 is a block diagram of the Icarus architecture.

Additional architectural changes from prior designs include independently timed hemispheres. This allows the user to project images onto each hemisphere and obtain 8 frames of temporal data while maintaining the full 25 μm spatial resolution on one half the image plane (1024 x 256) or, alternatively, utilize the entire image plane (1024 x 512) for four frames of data. Hemisphere tuning enables mitigation of fixed pattern timing offsets that have been observed in past cameras due to non-idealities associated with ROIC fabrication. The number of analog readout channels has been increased to 32 to maintain approximately the same readout time of 131 ms for 2.1 million pixel frames. Top level physical layout implementation was also improved. This resulted in a die size reduction of 20% for Icarus compared to past cameras while increasing the size of the image plane to 25.6 x 12.8 μm (a 13% detector active area increase).

Finally, the photodiode configuration was changed from common anode (n-on-p type) to common cathode (p-on-n type). Common cathode detectors improve the detector quantum efficiency for low energy X-rays (less than 2 keV), energetic electrons, and shorter wavelength visible light (less than 500 nm) at the expense of reduced transient response due to collecting holes rather than electrons. This improved QE will improve the performance of Icarus when sensing lower energy spectra.

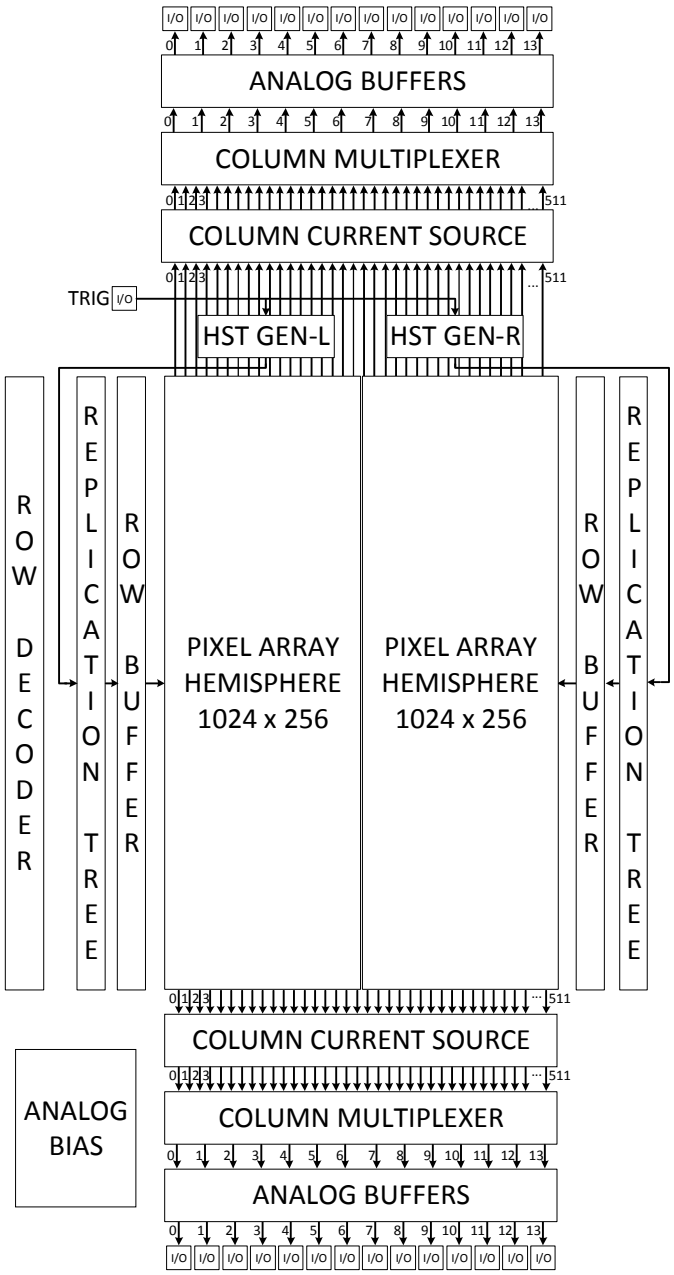

Figure 1. Block diagram of the Icarus ROIC.

2.1 High Speed Timing Generator (HSTGen) modifications

The high-speed timing generation block, responsible for generating configurable and independent shutters to be distributed to the pixel array, has been modified to incorporate independent hemisphere timing, hemisphere tuning, and additional programmability to accommodate the four shutters required for this iteration of camera.

2.1.1 Oscillator

Icarus incorporates two additional oscillators for evaluation. In addition to the previously characterized relaxation oscillator, [1] two, seven-stage ring oscillators, one with frequency reduction capacitors integrated in between each

stage, and one without, were designed. One of the three oscillators is selected via a two-bit digital multiplexer with an external test clock input available as the fourth bit. Figure 2 indicates frequency ranges available with the various clocking options

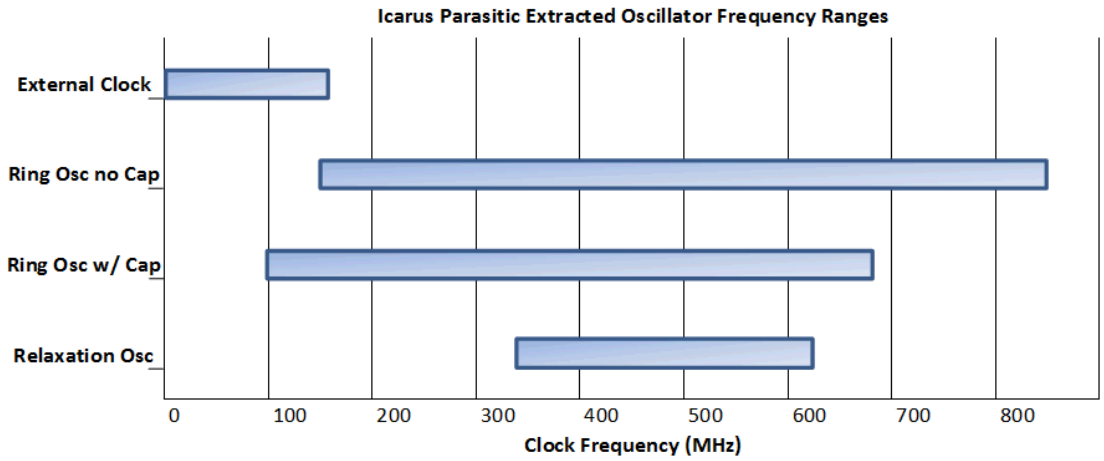

Figure 2. Plot of simulated oscillator frequency coverage.

2.1.2 Pattern generator/Deserializer

Two independent pattern generators have been integrated on Icarus, one generating shutters for the left hemisphere and a complement for the right hemisphere. Each register has a 40-bit depth and is synchronously clocked by one of the oscillators described in 2.1.1 to drive each independent hemisphere [Figure 3].

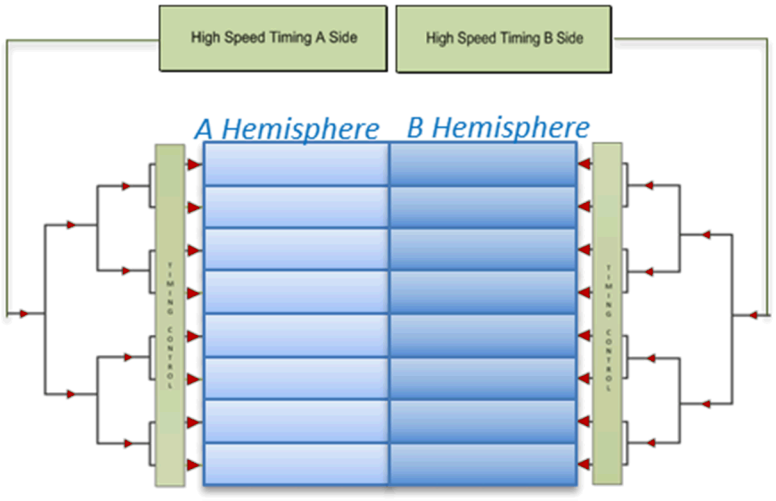

Figure 3. Shutter timing distribution concept.

2.1.3 Hemisphere tuning cell

Past imagers have displayed significant left/right hemisphere timing offset [1-3]. Driving both hemispheres from either side requires mirroring the physical layout of the die, which is necessary to reduce to overall row capacitive

load to enable nanosecond scale shutter pulses to be propagated. As a result, an offset in transistor source/drain drive, due to photolithographic mask shift occurs and is manifested as a timing offset. This offset can be minimized through careful design; however, it cannot be eliminated. Icarus integrates an analog delay cell, inserted in between the high-speed timing oscillator and the adjustable timing shutter shift register, capable of tuning the left and right hemispheres with respect to each other. This delay cell, in the form of a current starved inverter adjusted by off-chip bias voltages [Figure 4] is capable of sub nanosecond tuning.

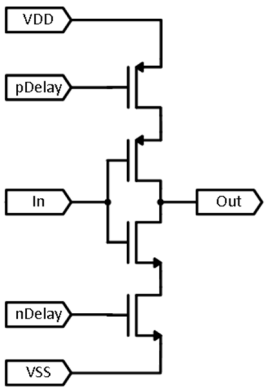

Figure 4. diagram of analog tuning cell.

2.2 High Speed Timing Distribution

Modifications were also made to the high-speed timing distribution circuitry to improve timing distribution fidelity.

On the Furi and Hippogriff cameras, the binary replication tree that distributes the shutter and reset pulses demonstrated minor, but visible vertical patterns due to the binary nature of the replication tree fanout. Icarus sought to mitigate this effect by shorting the outputs of stages six, eight, and ten to rebalance any offsets introduced by this replication circuitry [7] (Figure 5). There are some impacts to total dynamic current consumption with this method due to driving the additional parasitic capacitance of these output stage shorting interconnects, but is inconsequential when compared to transient photocurrent demands on the power supplies.

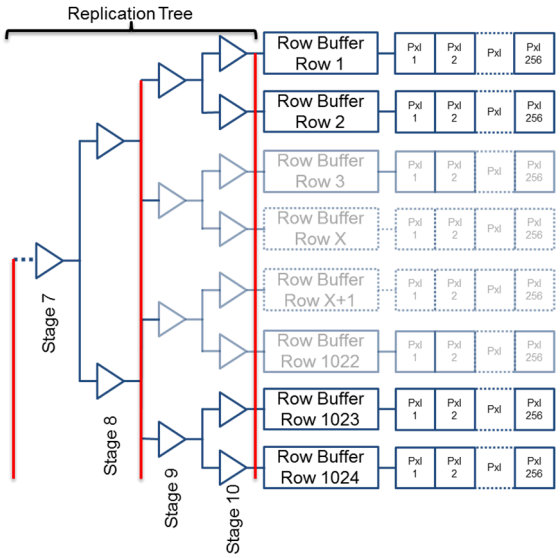

Figure 5. Block diagram showing the 3 stages where the replication tree is shorted.

2.3-Multi-Frame Pixel (Pixel)

Significant changes were made to the unit pixel cell for Icarus. Switching detector type from common anode to common cathode was advantageous to the ROIC pixel design. Photocurrent flowing into the pixel dictates referencing the pixel to VSS rather than VDD [Figure 6] as in past designs. The pixel uses a single, optimized nFET transistor for the shutter switch rather than a complementary pair as in Furi and Hippogriff. This affected the total voltage swing possible in the pixel but improved leakage and reduced shutter signal routing complexity by eliminating the need for complementary signal pairs. Common cathode design also requires only distributing a single VSS type reference plane. This allowed more robust ground plane physical implementation and reduced transient photocurrent IR drop.

Reference planes for the pixel were split into two. VSS provides return the path for MIM capacitor current and read-off source followers, and VRST provides the reference voltage for pixel reset. VRST can be adjusted off-chip, which allows the pixel array to be globally modulated to electrically test pixel functionality and readout. A tunable anti-bloom transistor has been integrated to mitigate large input signals that may occur during an experiment. Lastly, the physical layout of the pixel was reexamined and successfully minimized intra-pixel (frame-to-frame) and inter-pixel (pixel-to-pixel) coupling.

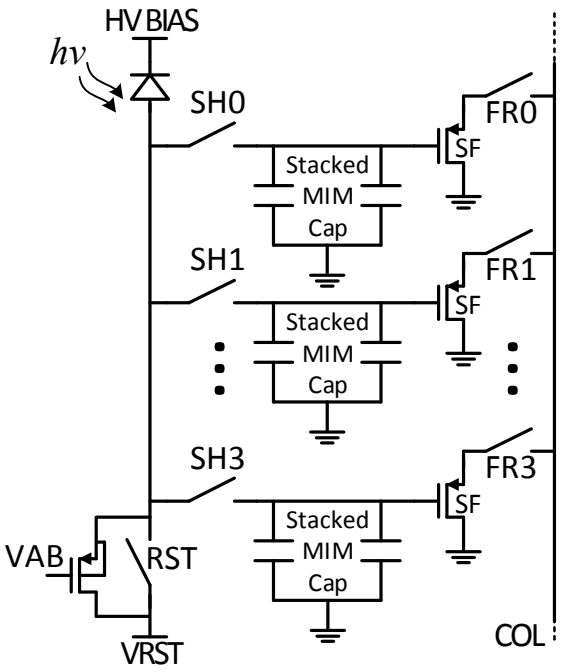

Figure 6. Icarus unit pixel.

2.4 Analog Readout

Parallel analog readout has been maintained as in previous imagers; however, the number of analog channels has been increased to 32, with the array readout being split from top to bottom to maintain the same overall readout time of 131 ms. This mitigates concerns over potential leakage of smaller storage capacitors than have been utilized on past cameras.

3. ROIC TEST RESULTS

Below is a brief summary of test and characterization of the Icarus camera. For a detailed examination of Icarus performance, see [8].

Note that an issue with pixel layout rendered two of the four frames of data inaccessible. This reduces the number of possible frames of data from four to two for this version of the camera. A re-spin of the ROIC eliminated this issue and is currently undergoing hybridization.

Table1 is a comparison of insertion delay of Icarus compared to past imagers.

Camera	Trigger-to-shutter latency	Timing propagation latency	Trigger-to-pixel latency
Furi	34 ns	48.13 ns	82.13 ns
Hippogriff	54 ns	26.6 ns	80.5 ns
Icarus	**32 ns**	**4.7 ns**	**36.7 ns**

Table 1 is a summary of insertion delay for the successive generations of UXI cameras. Icarus has more than halved insertion delay. This has been achieved by optimizing each individual stage in the binary replication tree. This has minimized the number of repeater inverters.

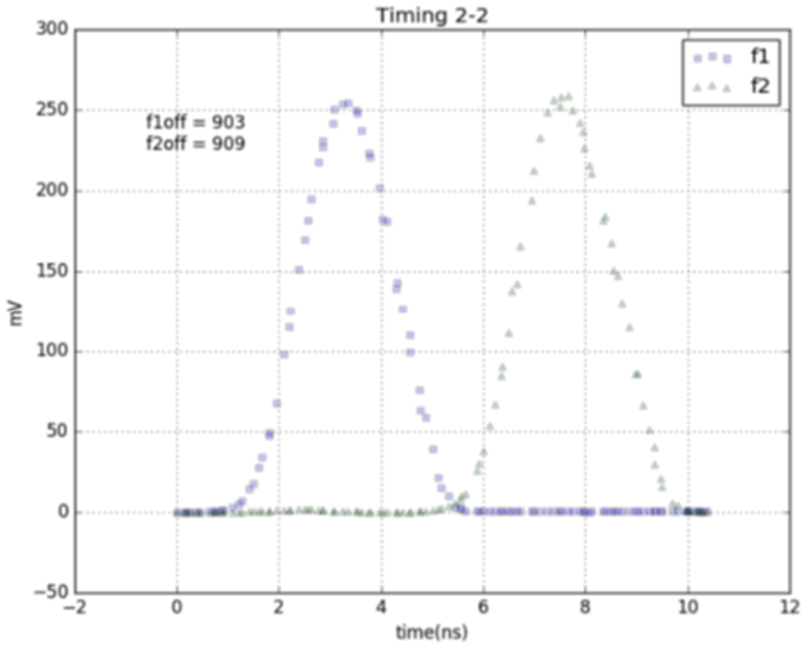

Figure 7. Two nanosecond shutter profile

Figure 7 is a high temporal resolution shutter profile for two frames, obtained by stepping an optical impulse in 20 ps increments. Shutter-to-shutter uniformity is greatly improved over past cameras.

Table 2. Left/Right hemisphere skew between Icarus and past sensors.

Camera	Native Left/Right Hemisphere timing skew
Furi	700-800 ps
Hippogriff	400-500 ps
Icarus	200-400 ps
Icarus Tuned	**70 ps**

Table 2 is a summary comparing past imagers hemisphere skew to Icarus and results of tuning the Icarus left/right skew via the analog tuning delay cells. One can observe significant generational improvements to timing skew, while the on-chip tuning capability allows one to reduce hemisphere timing skew to less than 3.5% of minimum integration time.

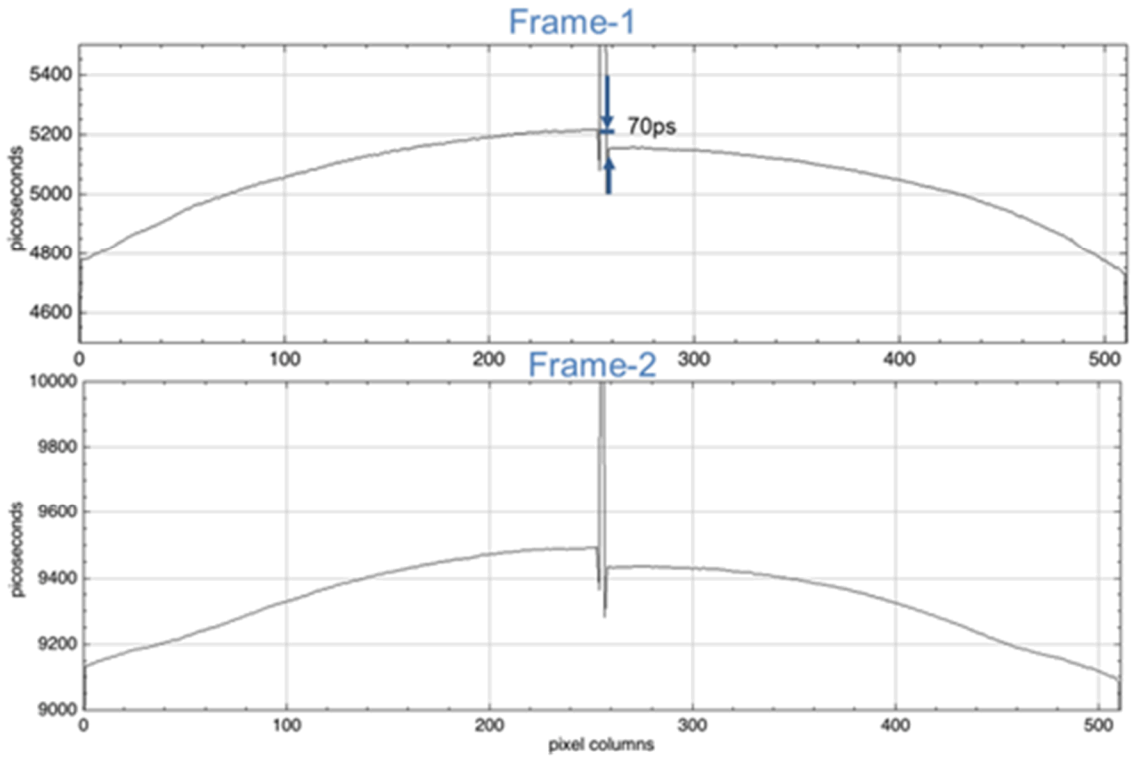

Figure 8. Row wise line out

Figure 8 is a row-wise line out showing row timing skew for frames 1 and 2. This skew is approximately 400 ps from the outer most column to inner most column. One can also observe the tuned hemisphere timing skew on the order of 70 ps. The spike in the middle of the line out data is due to two dead columns in the exact center of the pixel array.

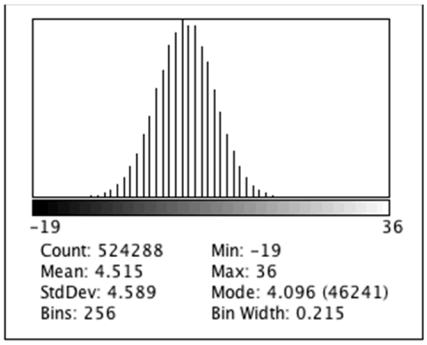

Figure 9. Dark pixel readout histogram.

Noise floor, combined with maximum full well dictates dynamic range. Lower noise floor allows the sensor to obtain relevant data in lower fluence applications. Read noise was targeted for improvement on the Icarus design with a goal of 500 e^-. Figure 9 is a histogram of pixel data for a dark image readout which provides a measurement of total read noise. ADC LSB is 76 µV for this measurement. 4.6 LSB's standard deviation translates to an RMS read noise of 164 e^-.

Table 3. Pixel leakage test results for 4 separate ROIC parts.

ROIC	ΔV at 500 ms	Time to 10% voltage droop
I14E1	13.8 mV	8.19 s
I14E8	8.0 mV	12.8 s
I14E5	8.3 mV	14.6 s
I14E6	8.0 mV	11.23 s
Average	**9.5 mV**	**11.7 s**

Capacitor leakage results are compiled in table 2 for four individual pixels across four separate ROICs. Pixel capacitor leakage measurements were performed by manually forcing 1.3 V onto a pixel. All shutter switches were disabled and leakage was recorded for two data points, ΔV at 500 ms and time to 10% signal droop. Leakage was linear with time (Figure 10). The primary leakage mechanism is the nFET shutter transistor channel leakage. From this data, it was determined that 2.5 mV leakage would be encountered by the final pixels read out at the end of 131 ms.

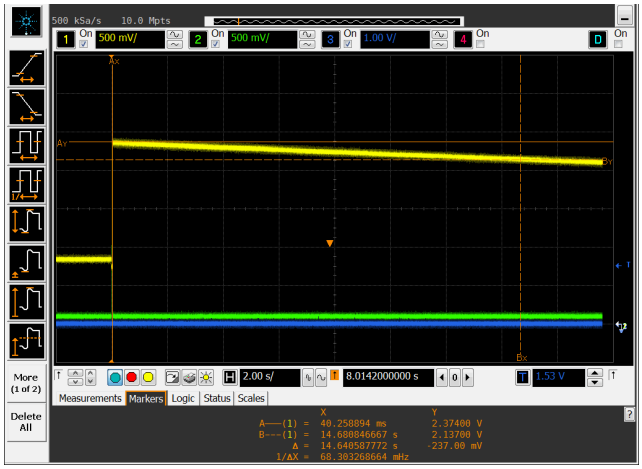

Figure 10. Pixel leakage over 10 s.

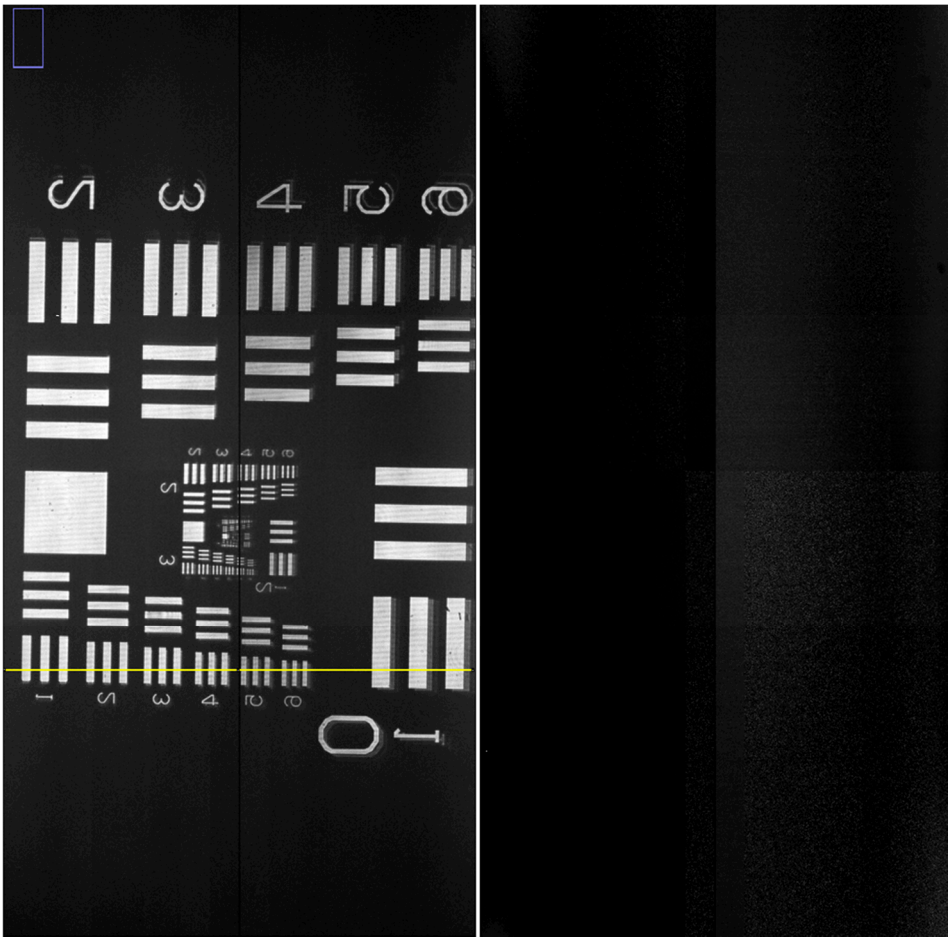

Figure 11. Frame 1 Air Force Test Pattern Image with Frame 1 on the left and unexposed Frame 2 on the right.

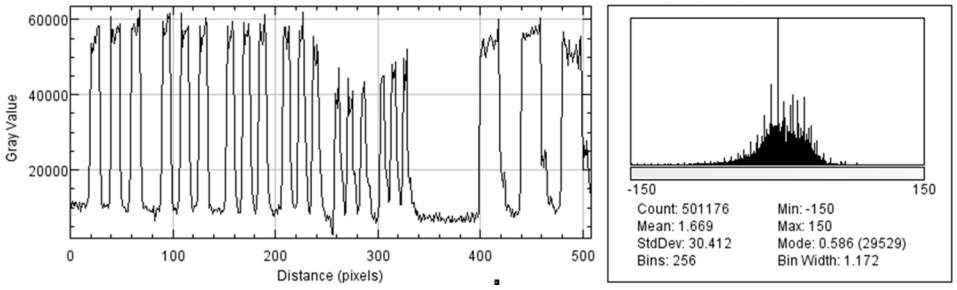

Figure 12. Lineout for frame 1 on the left, histogram of dark pixels for Frame 2on the right.

Figure 11 is a two-nanosecond time gated image sequence taken with an Air Force Test Pattern (AFTP) with a pulsed laser illumination timed for the first frame. The second frame is unexposed and demonstrates good isolation between frames. One LSB count = 76 µV. Fixed pattern offsets from the 32 analog output drivers are visible in the dark frame 2. Figure 12, left side plot is a line out of the AFTP demonstrating good Modulation Transfer Function while the right-side plot is a histogram of Frame 2 which is intentionally unexposed due to laser timing. Note that this histogram standard deviation is slightly larger than that of the dark calculations above, indicating approximately 26 LSB's

coupling frame-to-frame which translates to 1.6 mV or 750 e^-. Some reflections between the sensor and target can also be observed in Figure 11 which translates to a broadening of the lineout data in Figure 12. This is an artifact of the test setup and not camera performance

4. CONCLUSION

A 1024 x 512 pixel, 25 μm spatial resolution, four frame per-pixel imager has been built and characterized. Significant improvements in performance have been demonstrated over prior camera designs. Shutter profile quality has been improved, Noise floor reduced, and insertion delay more than halved. This imager has demonstrated exciting potential for utilizing hybrid-CMOS burst mode imagers in HEDP research, and work is ongoing to integrate the Icarus cameras into every national Inertial Confinement Fusion (ICF) facility as well as other world class research institutions.

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