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Rapid QSTS Simulations for High-Resolution Comprehensive Assessment of Distributed PV

Panel Session: New Operation and Planning Tools/Models for High PV Penetration Grids

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Quasi-Static Time-Series (QSTS)

What is QSTS?

Quasi-static time series (QSTS) analysis captures time-dependent aspects of power flow, including the interaction between the daily changes in load and PV output and control actions by feeder devices and advanced inverters.

What is the problem with today's tools?

Snapshot analyses and other methods that only investigate specific and limited time periods can be overly pessimistic about PV impacts. They do not include the geographic and temporal diversity in PV production and load and the interaction with control systems may not be adequately analyzed.

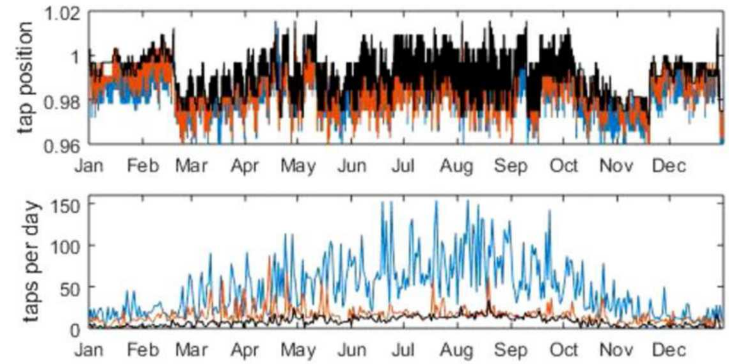
Why do we need QSTS?

QSTS simulations are needed today to understand:

- Rapid fluctuations due to high variable PV
- Impact to voltage regulators and switch capacitors
- Temporary extreme conditions before controls react

The need will continue to increase in the future:

- Study interactions between advanced inverters with volt-var
- Simulate fast operating FACTS devices



Yearlong QSTS for Regulator Tap Position

"You can't manage what you can't measure"

-P. Drucker

Progression of Impact Study Methods and Tools

	Extreme Voltages	Thermal Loading	Regulators Tap Changes	Capacitor Switching	Time outside ANSI	Losses	Computation Time[1]
Snapshot	Good	Good	-	-	-	-	<1 sec
Hourly Timeseries	Great	Great	-	-	Good	Great	5 sec
1 day QSTS	Poor	Poor	Decent	Decent	Poor	Poor	5 minutes
1 year QSTS	Great	Great	Great	Great	Great	Great	36 hours
New Rapid QSTS Algorithms	Great	Great	Great	Great	Great	Great	30 sec

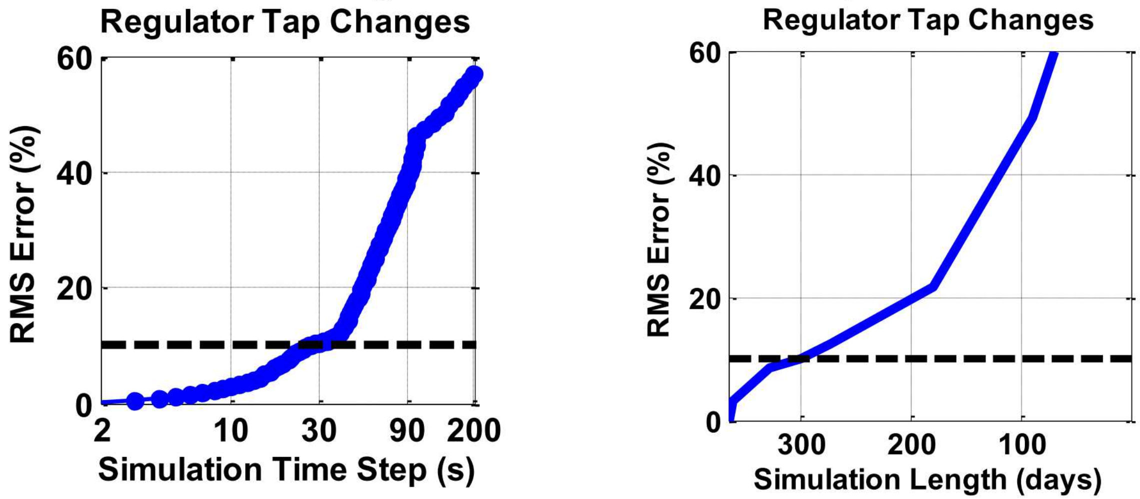
Our new rapid QSTS algorithms maintain the accuracy of high-resolution yearlong QSTS simulations

…..while solving in a fraction of the time

Quasi-Static Time Series (QSTS) Requirements

- QSTS simulations need to be:
  - High resolution simulation to capture solar variability (time step less than 10 seconds)
  - Extended-term simulations (year-long)

Error for Time-Step and Simulation Length Compared to Yearlong 1-second Resolution QSTS



M. J. Reno, J. Deboever, and B. Mather, "Motivation and Requirements for Quasi-Static Time Series (QSTS) for Distribution System Analysis," IEEE PES General Meeting, 2017.

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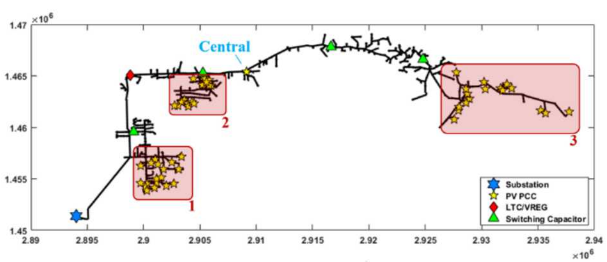
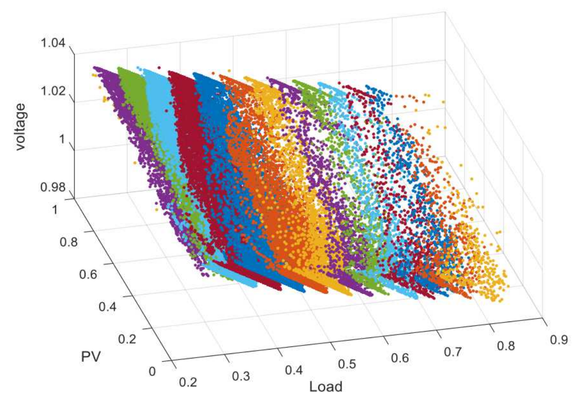
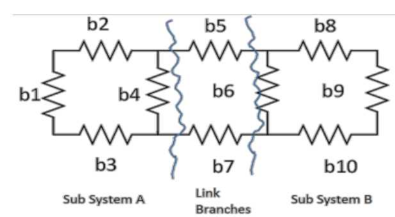
Computational Time of QSTS

- **Objective**: Reduce the computational time (10-120 hours) and complexity of QSTS analysis to achieve year-long time-series solutions that can be run in less than 5 minutes
- There are several ways to improve the speed of QSTS
  1) Fast Time-Series Approximations
  2) Improved Power Flow Solution Algorithms
  3) Circuit Reduction
  4) Parallelization of QSTS (Temporally or Spatially)

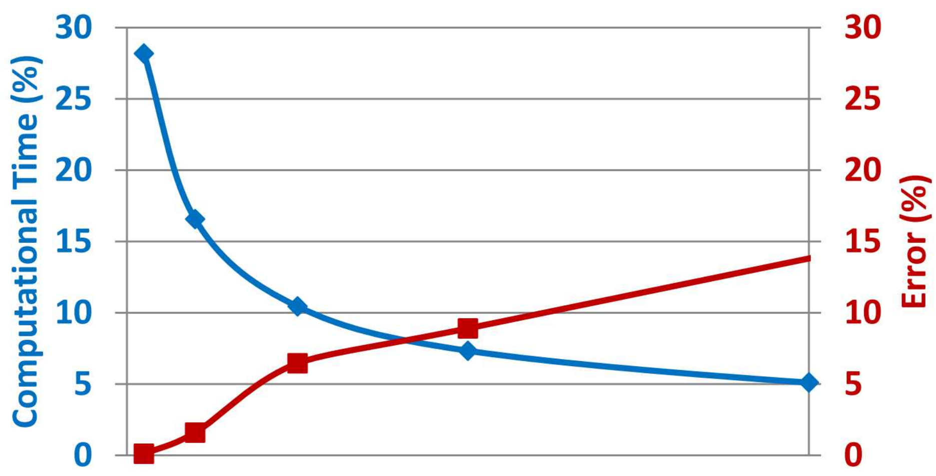






Evaluating Speed and Accuracy

- Speed improvements may come at the expense of accuracy



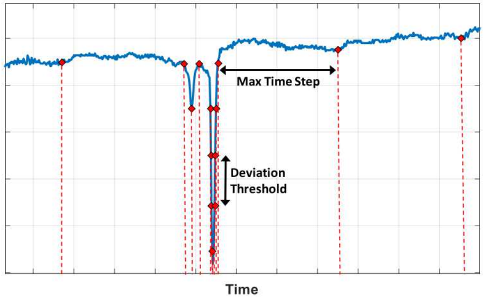
- All new algorithms are tested extensively and validated against yearlong 1-second resolution QSTS results
  - Regulator tap changes, capacitor switching operations
  - Bus voltages, hours per year with ANSI violations
  - Thermal loading (worst overloads and time overloaded)
  - Yearly line losses

1) Fast Time Series Approximations

- Objective: Dramatically speed up the computational process using innovative methods to progress through the timeseries simulation

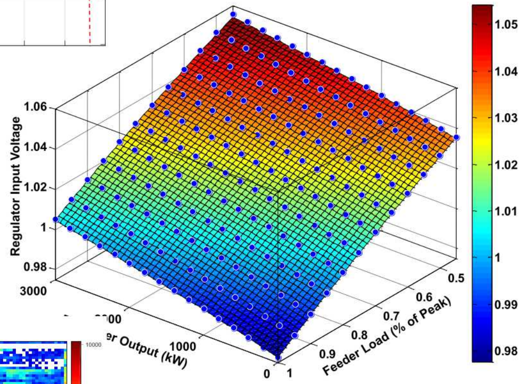
▣ Variable Time-Step

– Reduce the computational burden by adjusting the QSTS time-step to solve fewer load flows, skipping forward to time points of interest



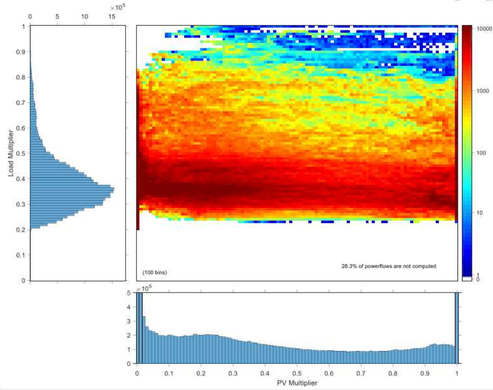
▣ Event-Based Simulation

– Detect discrete system events using voltage sensitivities and jump from event to the next



▣ Vector Quantization

– Take advantage of repeated power flow computations using a quantized lookup table to bypass the power flow solver

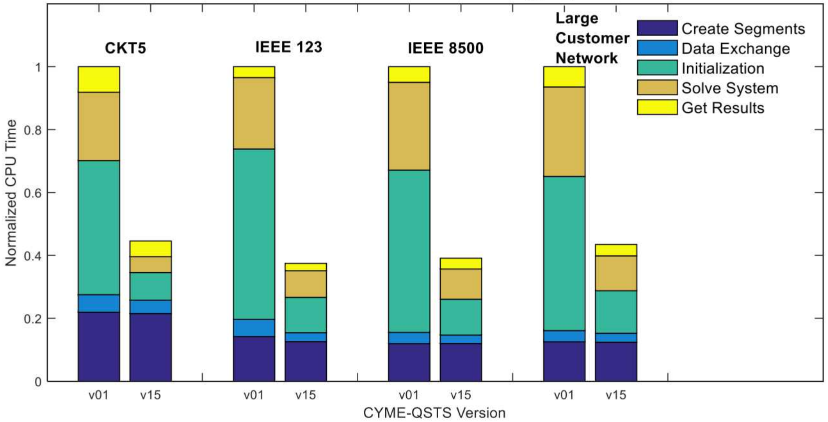


2) Improved Power Flow Algorithms

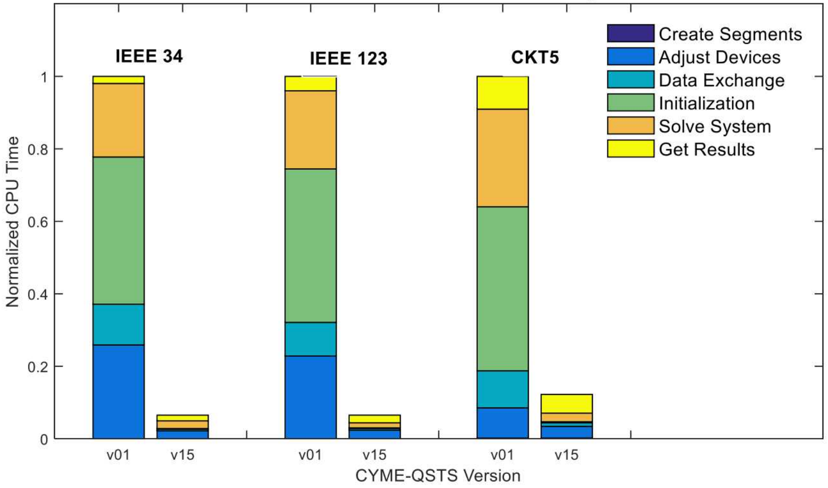
Objective: Speed up single power flow solutions through improved algorithms, data handling, and memory management

Solutions:
- Initialization using previous solution
- Focused data recording and offloading
- Improve memory management
- Investigate different power flow algorithms
- Decrease controller convergence time

Reduction in CPU time for a **single** power flow



Reduction in CPU time for **1440 series** power flows

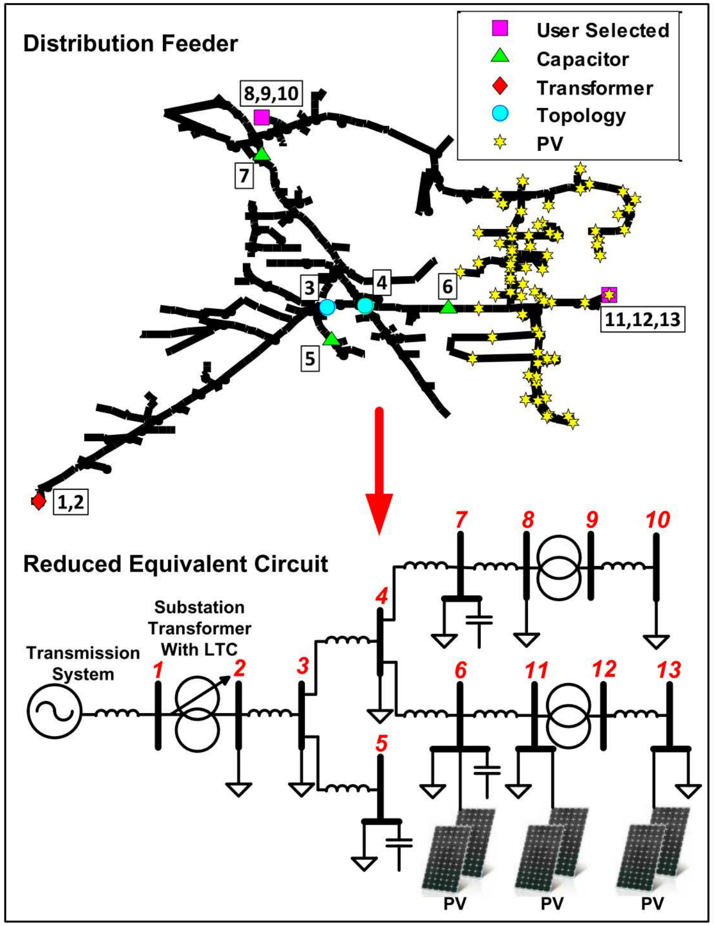


3) Circuit Reduction

Objective: Use an equivalent reduced circuit with fewer buses to decrease the power flow simulation time.

Solutions:

- Many buses can be removed or aggregated into nearby buses, while keeping the results for the remaining buses equivalent
- Reduction algorithms can handle unbalanced loads and PV, unbalanced and unsymmetrical wire impedance, mutual coupling, shunt capacitance, transformer magnetizing currents, and multiple different load profiles and PV power profiles.



4) Parallelization of QSTS

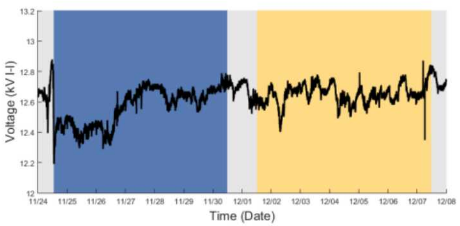
Objective: Solving QSTS is inherently sequential (single-core), but the speed can be improved with more computational power

Solutions:

- Intelligently divide the solution to allow for parallelization (multi-core)
- Many personal computers have multiple cores
- Small clusters or servers can be used for processing (CYME Server)

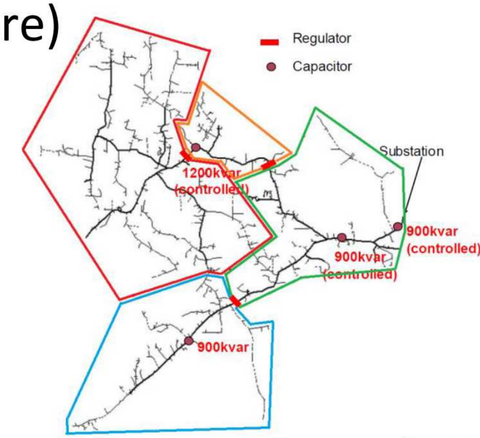
Temporal Decomposition

- Yearlong QSTS is split into individual solutions and computed via multiple cores
- Solutions are "stitched" together after processing



Diakoptics

- Circuit is intelligently divided and power flows for division calculated (multi-core)



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Results of the QSTS Project for PY 1 & PY 2

- We have developed a portfolio of rapid QSTS algorithms, each demonstrating significant speed improvements
- Algorithms can be combined for additional speed
  - For example: a reduced circuit can be simulated with a variable time-step separated onto several parallel cores
- The project was targeting 1400x speed improvement:

$$\frac{\textbf{120 hours}}{\underset{\text{Fast Timeseries}}{10} \times \underset{\text{Improved Power Flow Solution}}{2} \times \underset{\text{Circuit Reduction}}{10} \times \underset{\text{Parallelization}}{7}} = \textbf{5 minutes}$$

- Project has been extremely successful and in research settings we may be able to achieve even faster speeds reaching greater than **100,000x faster**

$$\underset{\text{Fast Timeseries}}{200} \times \underset{\text{Improved Power Flow Solution}}{5} \times \underset{\text{Circuit Reduction}}{20} \times \underset{\text{Parallelization}}{7}$$

Conclusions

- Timeseries analysis is important for distribution system planning with high penetrations of DER, and high-resolution QSTS is needed to model the impacts to voltage regulators and controls
- Compared to a normal brute-force QSTS simulation at 1-second resolution for a year, rapid QSTS algorithms dramatically reduce the computational time
- Several rapid QSTS algorithms have been implemented into software - CYME improved QSTS speeds up to 10x faster
- Ongoing and future work
  - Combining rapid QSTS algorithms to demonstrate full potential
  - Implementing rapid QSTS into analysis software packages for researchers and industry to use

QUESTIONS?

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