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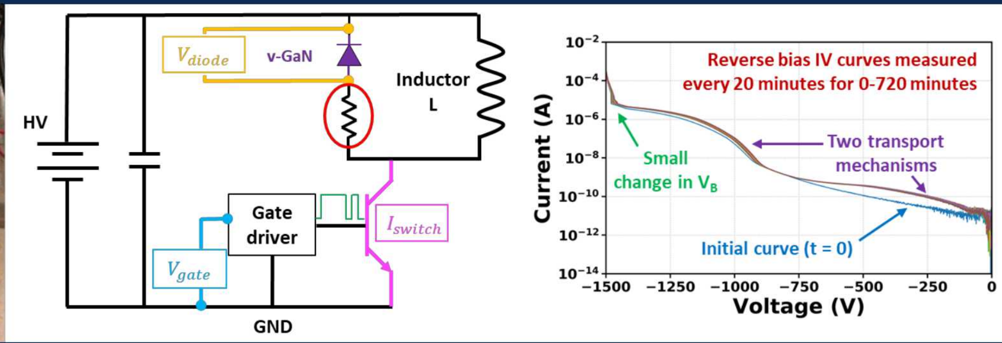

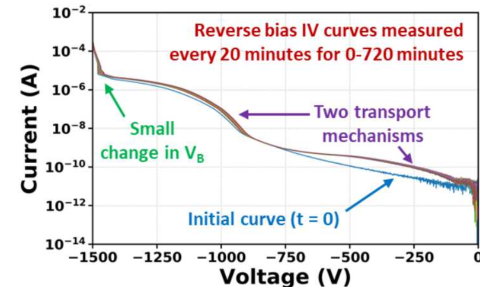

MRS SPRING MEETING & EXHIBIT

Phoenix, AZ
April 4, 2018

Hard-Switching Reliability Studies of 1200 V Vertical GaN PiN Diodes

R. Kaplar[1], O. Slobodyan[1], J. Flicker[1], S. Sandoval[2], C. Matthews[2], M. van Heukelom[1], T. Smith[1], S. Atcitty[1], S. Khalil[3], and S. Bahl[4]

1 – Sandia National Laboratories, Albuquerque, NM

2 – Sandia National Laboratories, Albuquerque, NM and University of Arkansas, Fayetteville, AR

3 – Infineon, El Segundo, CA

4 – Texas Instruments, Santa Clara, CA

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U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

III-Nitride Semiconductors Are Outstanding Materials for Power Devices

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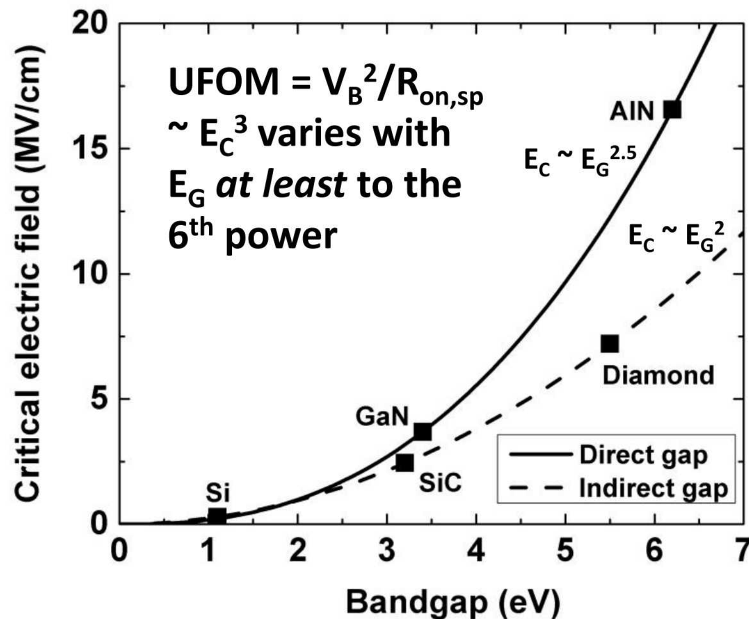
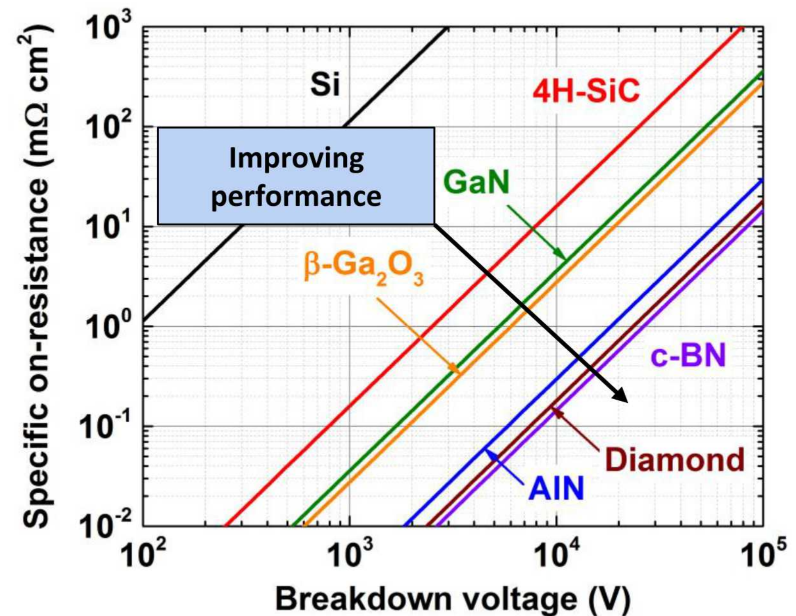
Fundamental Materials Capabilities

	Conventional		WBG		UWBG
Property	**Si**	**GaAs**	**4H-SiC**	**GaN**	**AlN**
Bandgap (eV)	1.1	1.4	3.3	3.4	6.0
Critical Electric Field (MV/cm)	0.3	0.4	2.0	4.9	13.0

III-N





Hudgins et al., *IEEE Trans. Pwr. Elec.* 18, 907 (2003)
J. Y. Tsao et al., *Adv. Elec. Mat.* 4, 1600501 (2018)

Unipolar FOM = $V_B^2/R_{on,sp} = \varepsilon\mu_n E_C^3/4$

Critical Electric Field
Is Not a Constant

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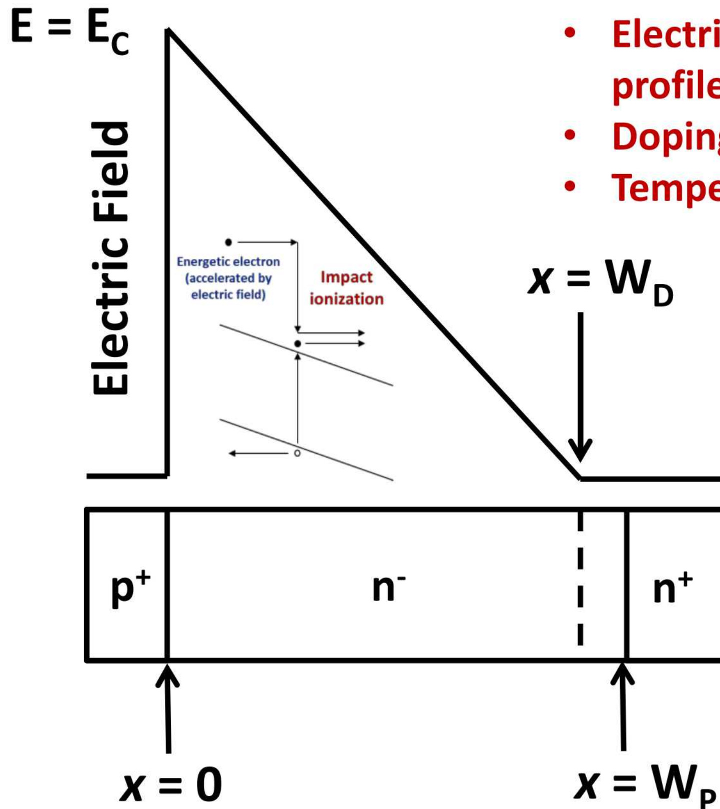
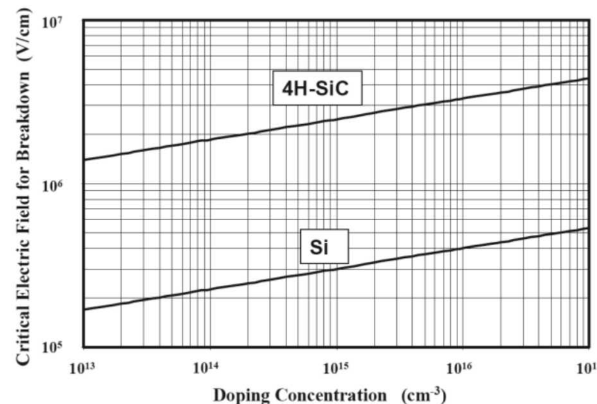
Critical electric field depends on:

- **Electric field profile (E_C is formally defined for triangular field profile in non-punch-through drift region)**
- **Doping (impurity scattering competes with impact ionization)**
- **Temperature (phonon scattering competes with impact ionization)**



$$M(x) = \frac{exp[\int_0^x (\alpha_p - \alpha_n) dx']}{1 - \int_0^{W(E_C)} \alpha_n exp[\int_0^x (\alpha_p - \alpha_n) dx'] dx}$$

Avalanche occurs when denominator approaches zero



Impact ionization and critical electric field are not well characterized for GaN or other III-N semiconductors!

The critical electric field is defined as the peak electric field that leads to avalanche breakdown in a 1D model

B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer (2008)

Impact of WBG Devices on Power Conversion Systems

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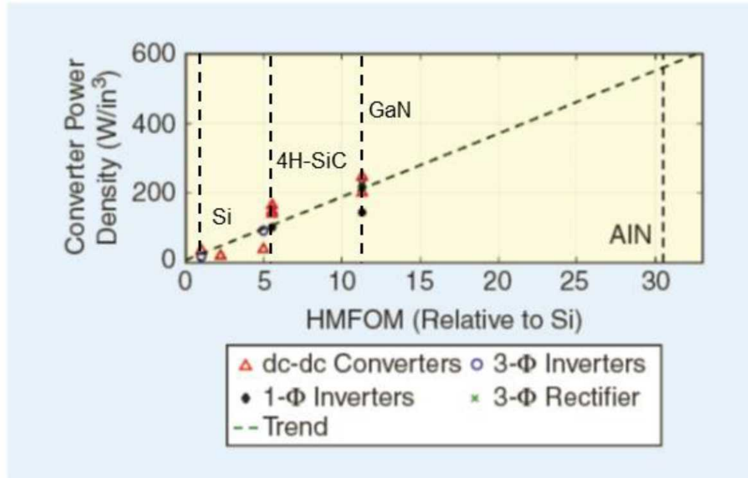
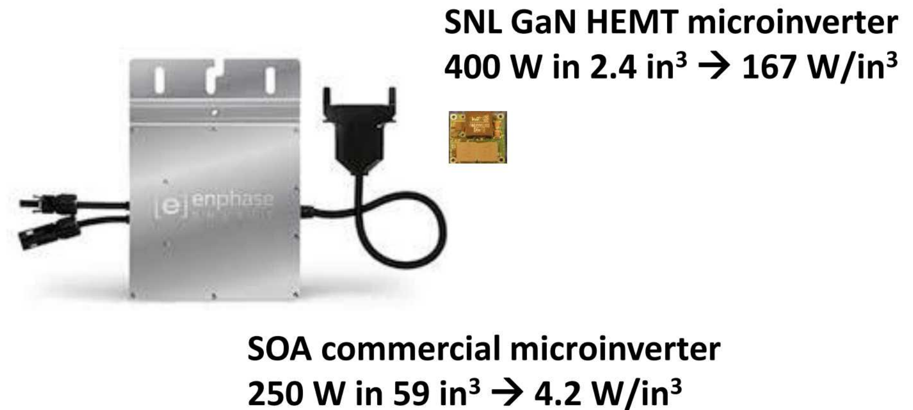
Huang Material FOM = $E_C \mu_n^{1/2}$



Considers conduction and switching losses



SNL GaN HEMT microinverter
400 W in 2.4 in^3 → 167 W/in^3

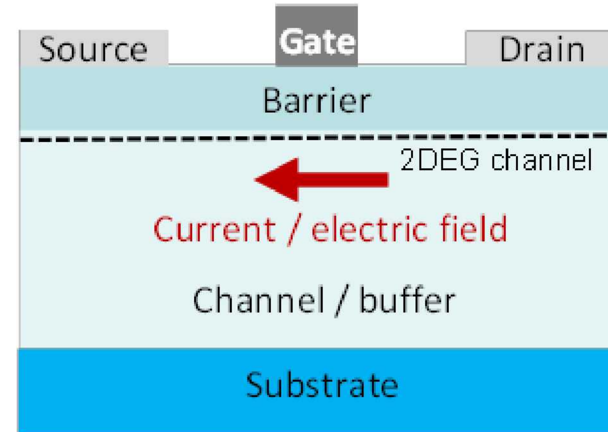
SOA commercial microinverter
250 W in 59 in^3 → 4.2 W/in^3

- **WBG semiconductor devices can have a strong impact on system size and weight due to reduced size of passive components and reduced thermal management requirements**
- ***But their reliability is less well characterized than traditional Si devices, especially for GaN and for realistic switching conditions***

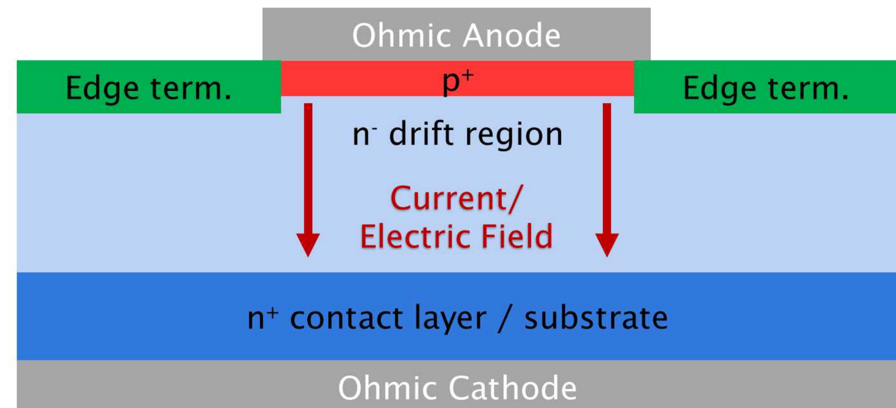
R. J. Kaplar et al., *IEEE Power Elec. Mag.* 4(1), 36 (2017)

Vertical GaN Power Devices

- **Historically, GaN power devices have lateral architecture**
  - **Limits voltage hold-off to ≈<650 V due to electric field management**
  - **High frequency, but no avalanche**



- **Vertical GaN (v-GaN) devices are now becoming available**
  - **Better potential for high-voltage operation (≈>1200 V)**
  - **Avalanche capability**
  - **Reliability and switching performance are largely *uncharacterized* in literature**



Area Advantage of Vertical GaN

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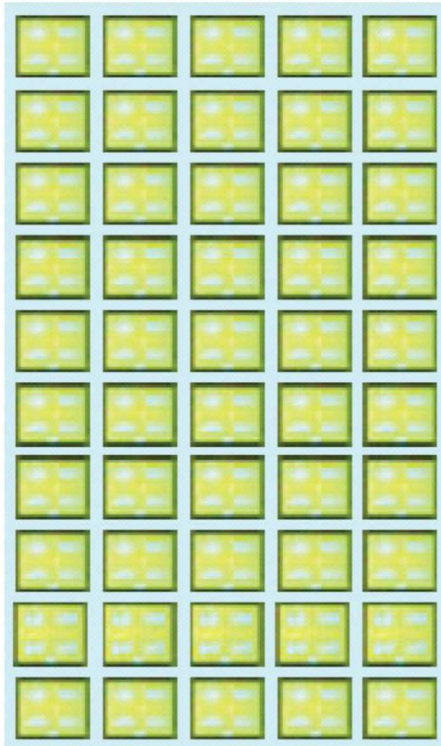
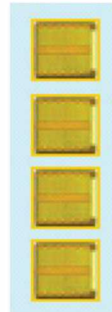
For a given on-resistance (R_{on}) of 10mΩ:

- **Tested Avogy vertical GaN PiN diodes**
  - 0.72 mm^2 area
  - 1200 V, 15 A peak forward current



500mΩ, 50 chips

Si-MOSFET

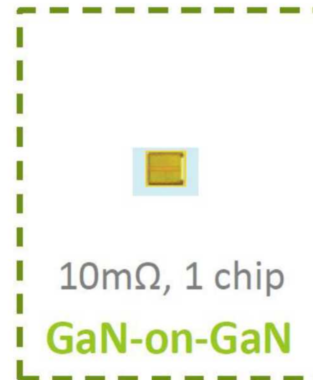


40mΩ, 4 chips

GaN-on-Si

SiC

GaN-on-GaN lowers die cost while improving $R_{on} \times C_{off}$ switching characteristic



10mΩ, 1 chip

GaN-on-GaN

The devices tested were obtained from I. Kizilyalli and O. Aktas at Avogy, and were fabricated under the ARPA-E SWITCHES program managed by Dr. Tim Heidel

I. C. Kizilyalli et al., *Microelec. Rel.* 55, 1654 (2015)

Current-Voltage Characteristics of v-GaN PiN Diodes

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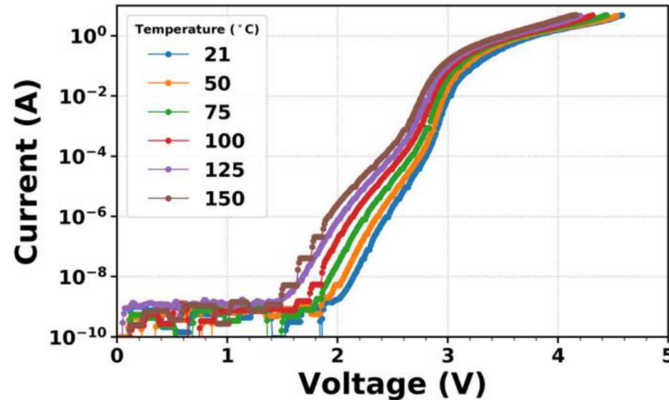
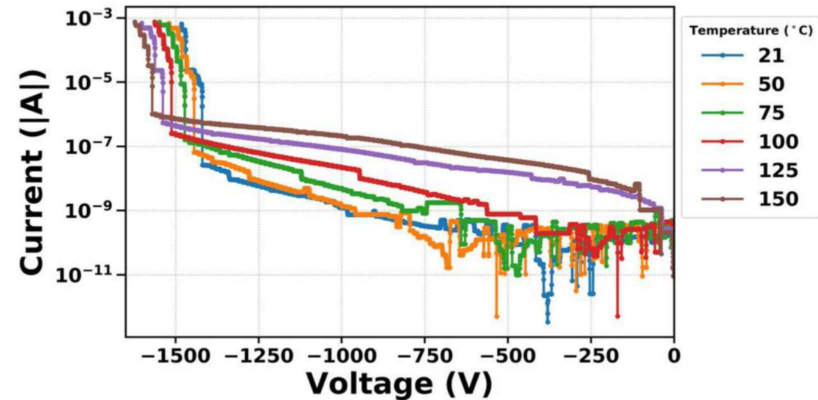
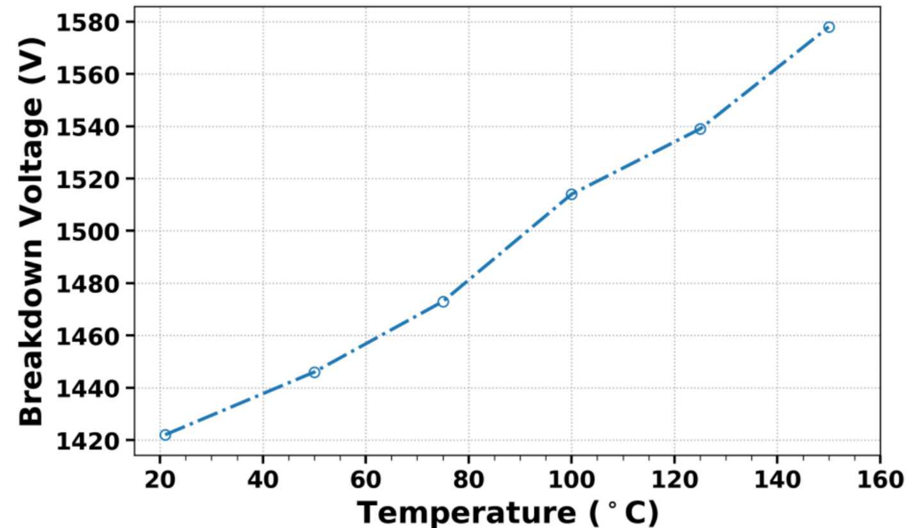




- Forward and reverse I-V curves measured
  - Room T to 150℃, 25℃ steps
- Confirmed datasheets
- Avalanche breakdown
  - Positive temperature coefficient
  - Repeatable and non-destructive



Vertical GaN PiN Diodes Show *Avalanche Ruggedness*

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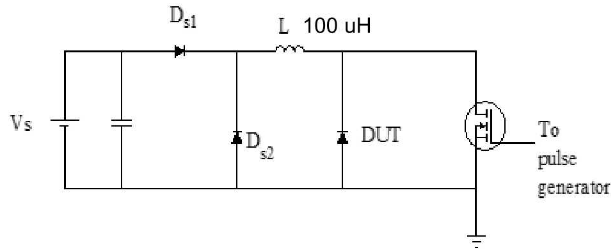

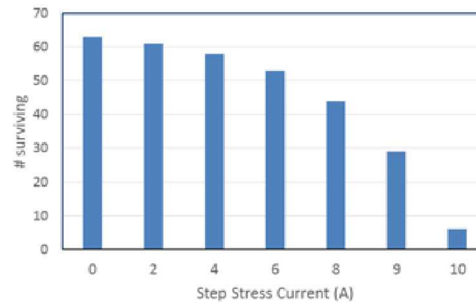

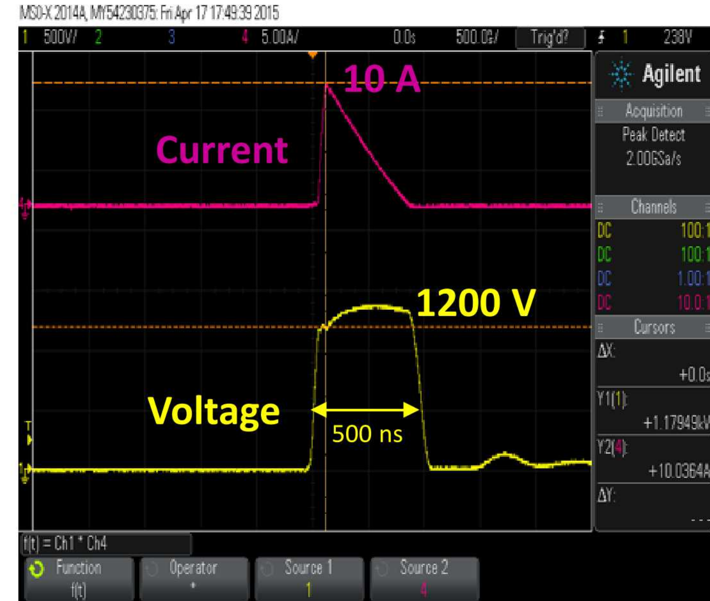

GaN vertical p-n diodes (A=0.36 mm²) can withstand 10^5 / 5kHz pulses at 10A and 1200V for 10's of ns

- **1200 V GaN PiN diode, 0.36 mm², packaged in TO220**
- **Avalanche peak power 12 kW → Energy per pulse 3 mJ**
- **Avalanche current increased after each 10^5 pulse cycle**
- **Number of surviving parts recorded; no parametric degradation for survivors**

O. Aktas and I. C. Kizilyalli, *IEEE EDL* 36(9), 890 (2015); I. Kizilyalli et al., *Microelec. Rel.* 55, 1654 (2015)

Double-Pulse Test Circuit

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- **DPTC is usually used to characterize switching of inductively-loaded power transistors**
  - **But for this work, we use a known good switch and characterize the diode**
- **Two modes of operation**
  - **Transient (double-pulse): Traditional use, characterizes switching behavior**
  - **Steady-state (continuous): New use for reliability testing**
- ***Realistic evaluation of reliability in a switching power circuit***

Circuit Diagram

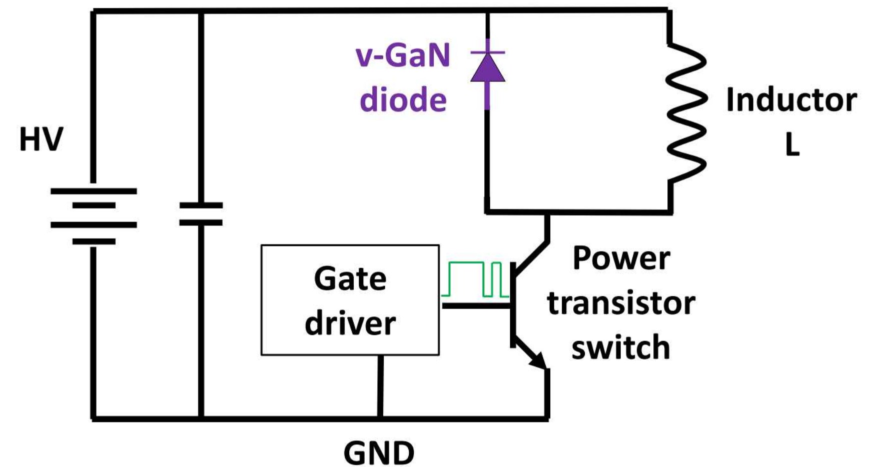

Photo of test circuit

Operation of DPTC

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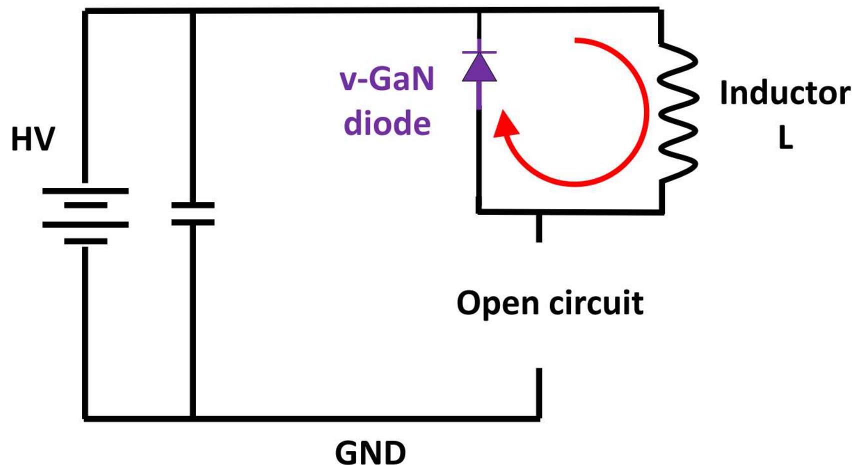
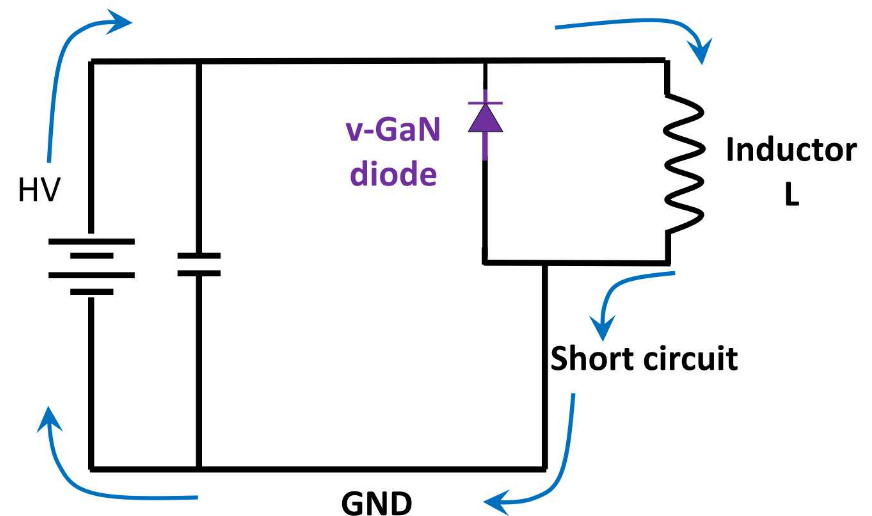
The circuit has two configurations, depending on whether the switch is open (off-state) or closed (on-state)

Switch open (off-state)



- **Supply voltage dropped across open circuit**
- **Diode is forward biased (few volts) so small voltage across inductor**
- **Inductor current is therefore constant and circulates around diode-inductor loop**

Switch closed (on-state)



- **Supply voltage dropped across reverse-biased diode, leakage current only**
- **Large voltage across inductor equal to diode reverse bias voltage**
- **Inductor current ramps up linearly and flows around circuit**

Switching Characterization Using DPTC

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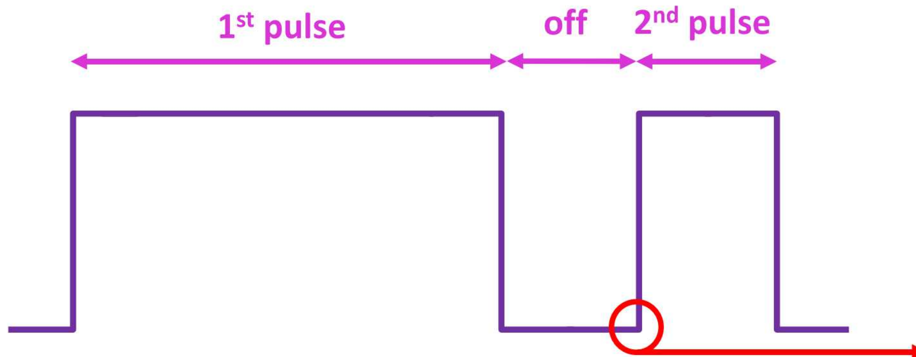
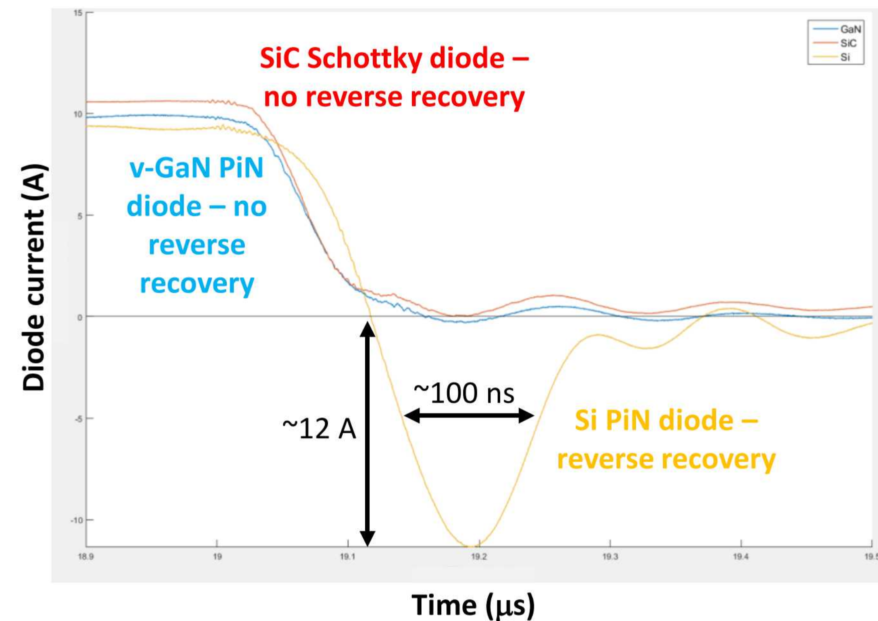
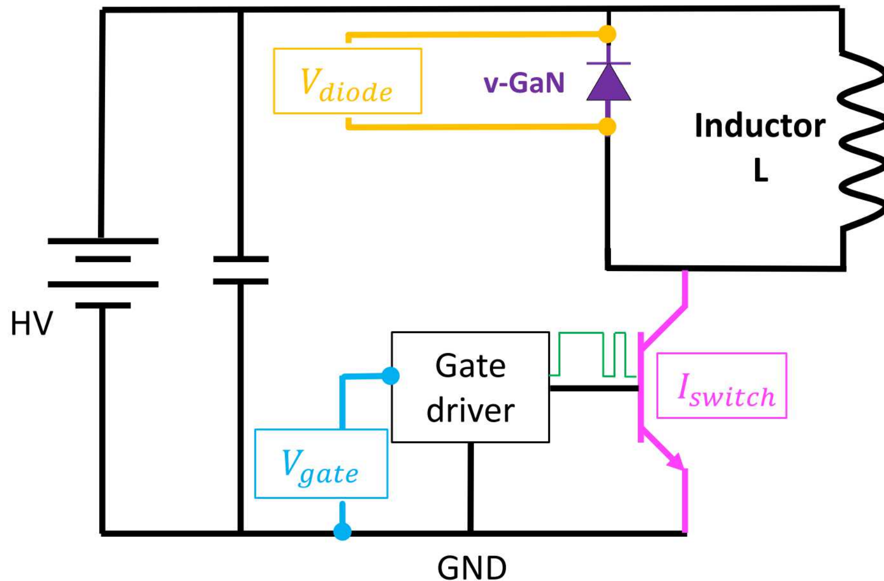


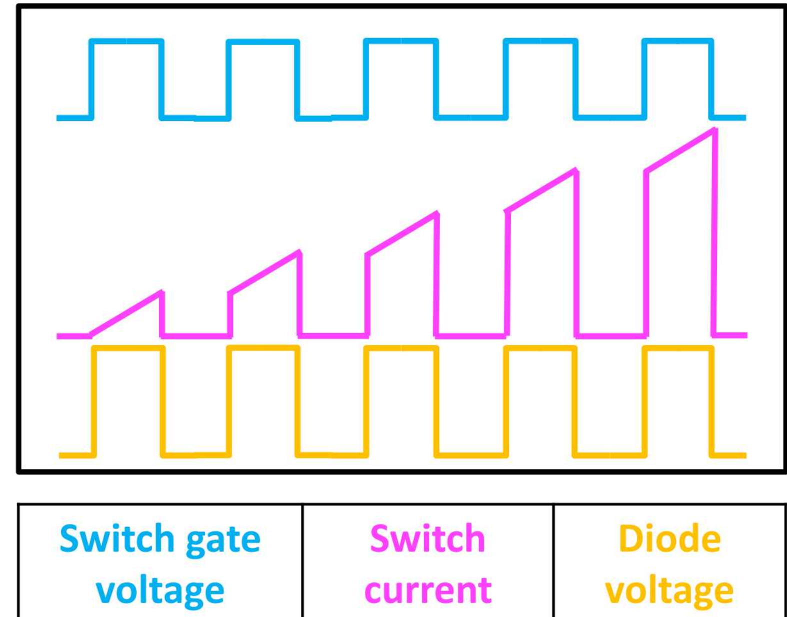
- 1st gate pulse: Increase stored energy in inductor – "charge up" to quasi-steady-state
- Gate off: Current circulates through diode/inductor loop
- 2nd gate pulse: Characterize switching transients



C. Matthews et al., *Proc. WiPDA* 4, 135 (2016)

Continuous Waveforms in Ideal DPTC





- **Idealized analysis of the double-pulse circuit**
  - All elements are lossless
  - Inductor causes current to increase indefinitely
  - Not realistic!

Continuous Waveforms in Realistic DPTC

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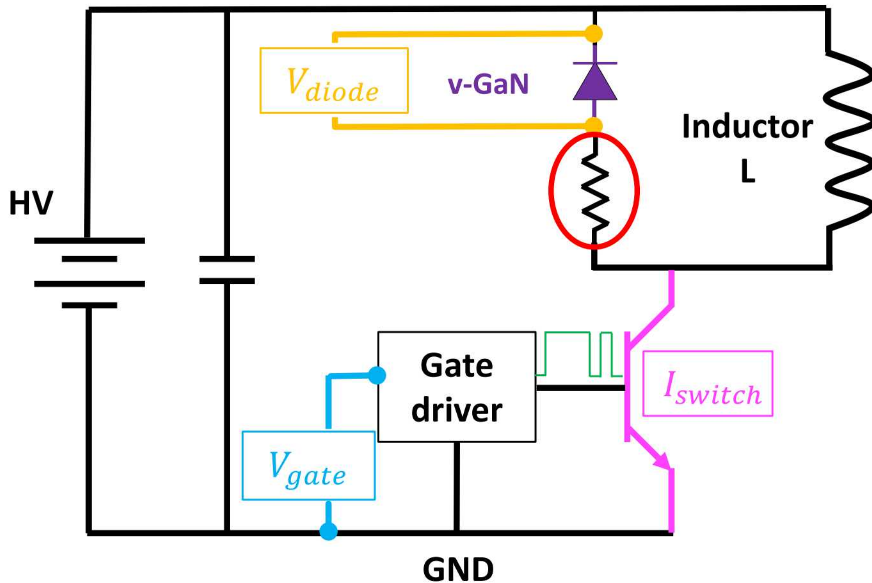
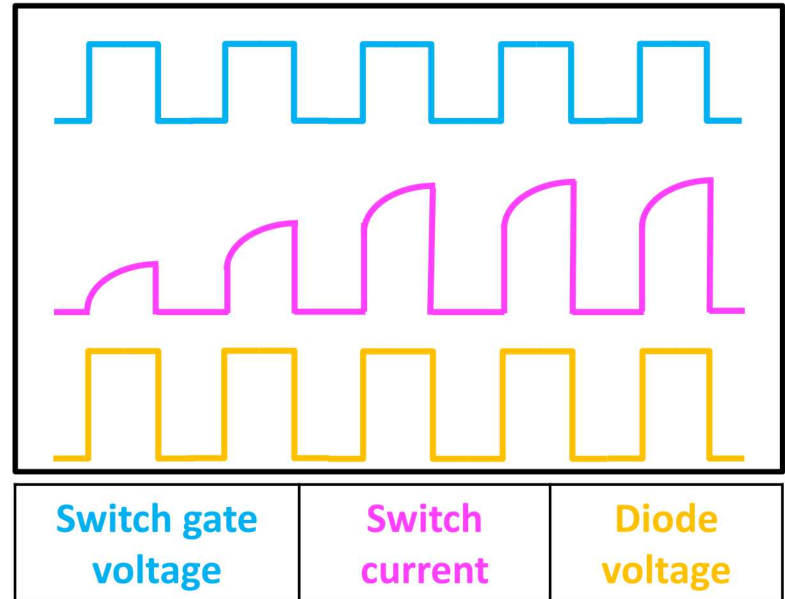
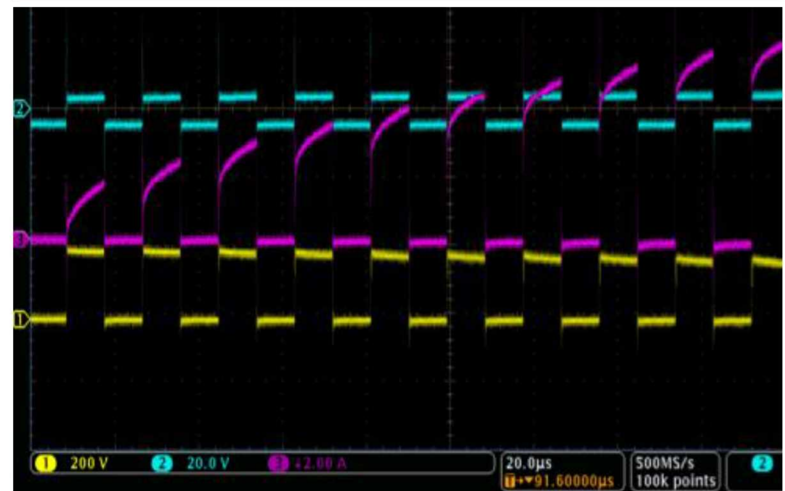
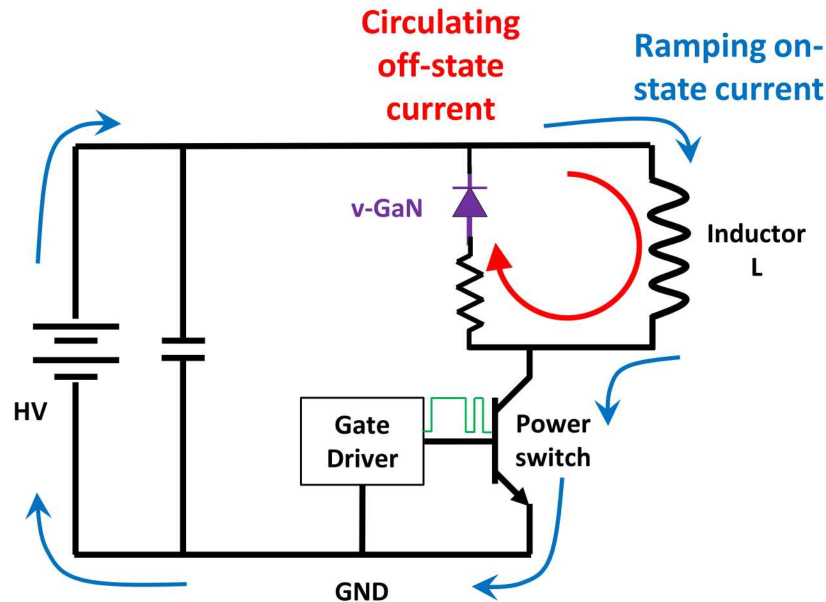






- **Real circuit has lossy elements**
  - Represented by lumped resistance in free-wheeling loop
  - Causes switch and diode current to saturate
  - Realistic DPTC is useful for continuous reliability testing!

Parameters for Steady-State Stress Operation of DPTC



- On-state current ramp:
  - $t_{on} = \frac{\Delta I_L \cdot L}{V_{in}}$
- Off-state current in loop:
  - $I_L(t) = I_{max} \cdot e^{-\frac{R}{L}t}$
- Decay time:
  - $t_{off} = -\frac{L}{R} \ln\left(1 - \frac{t_{on} \cdot V_{in}}{L \cdot I_{max}}\right)$

- Switching stress applied for 720 minutes at each of the following supply voltages:
  - 500, 750, 1000, 1170 V
- Gate drive conditions
  - Switching frequency = 1 kHz, t_{on} = 2 μs (duty = 0.2%)
  - R ≈ 1 Ω (parasitic)

500 V Pulsed Stress Measurements

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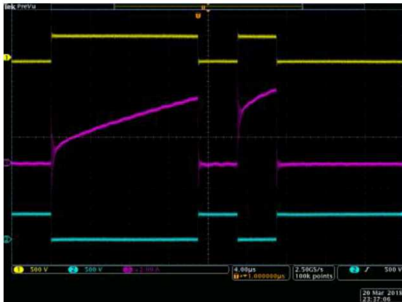
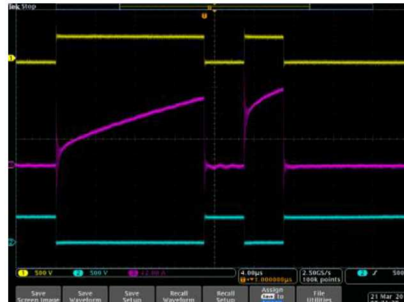
Double Pulse Pre-Stress



Double Pulse Post-Stress

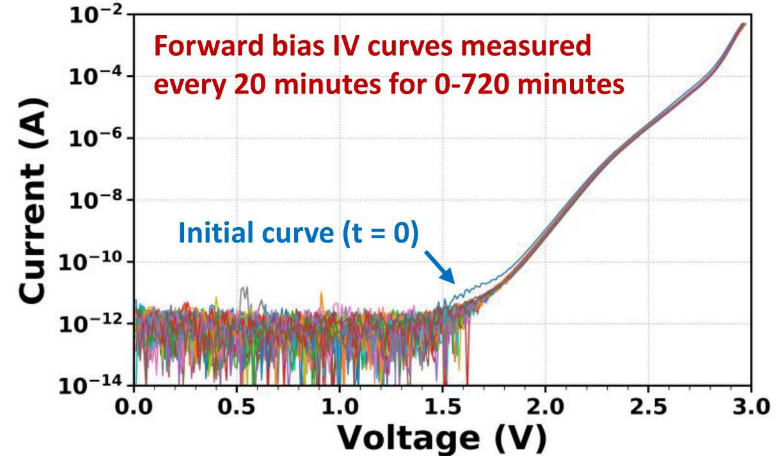


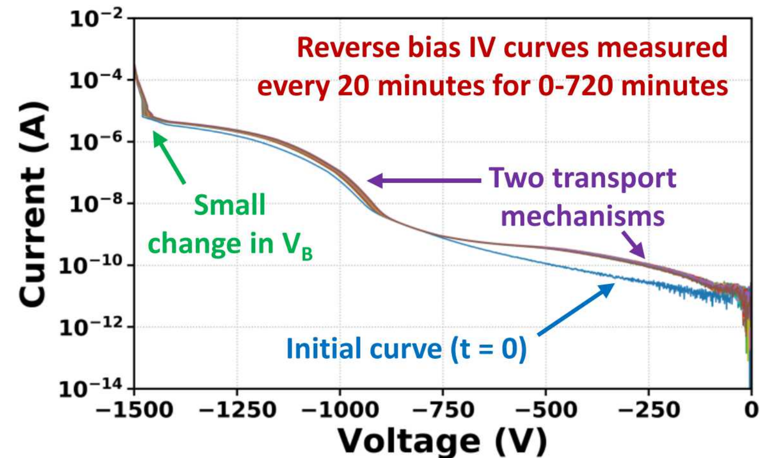
Diode voltage

Switch current

Switch D-S voltage

Stress Pulse





Small initial change in leakage current at lower V_R, followed by very stable operation

Parametric Drift During 500 V Pulsed Stress

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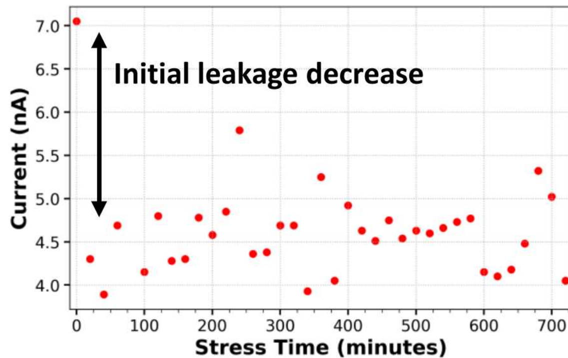
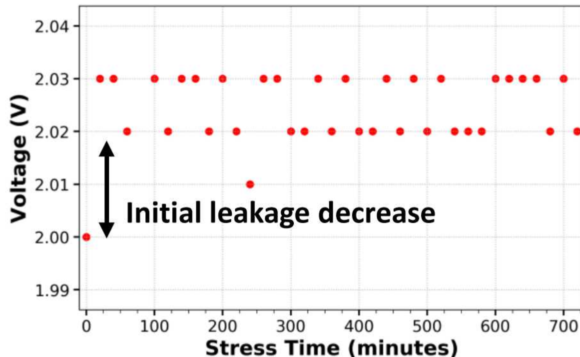
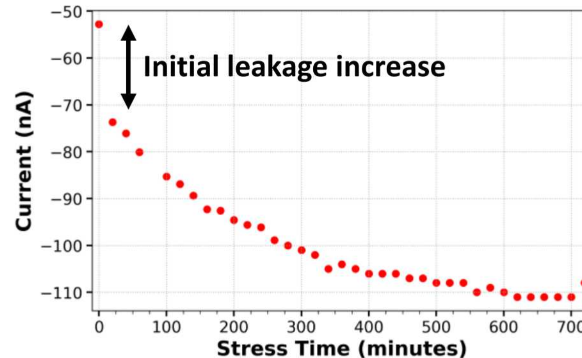
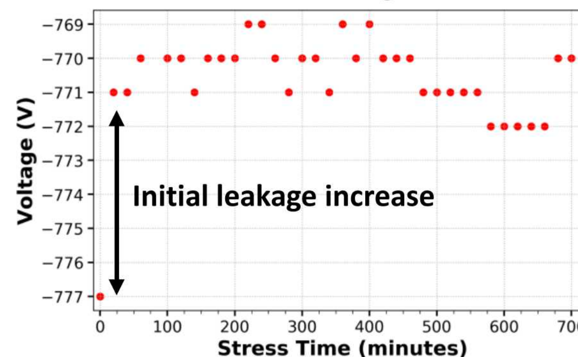
Forward Bias



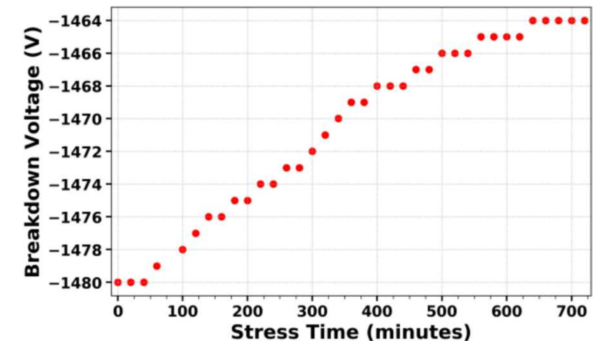


Reverse Bias





Breakdown Voltage



Small, monotonic decrease in breakdown voltage with stress time

Small initial change in leakage current, followed by very stable operation

750 V Pulsed Stress Measurements

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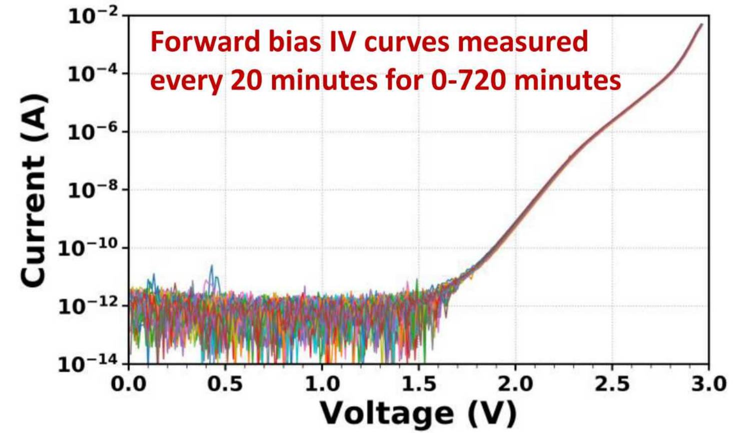
Double Pulse Pre-Stress

Double Pulse Post-Stress

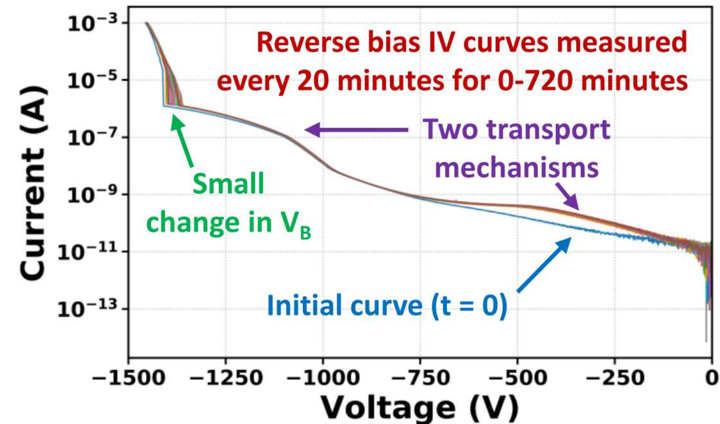


Diode voltage

Switch current

Switch D-S voltage

Stress Pulse



- Initial change in leakage similar to 500 V stress
- Small reduction in V_B with stress time

Parametric Drift During 750 V Pulsed Stress

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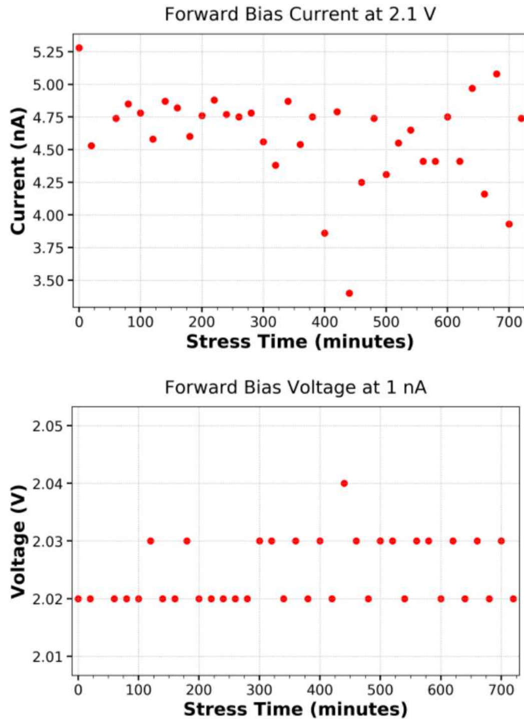
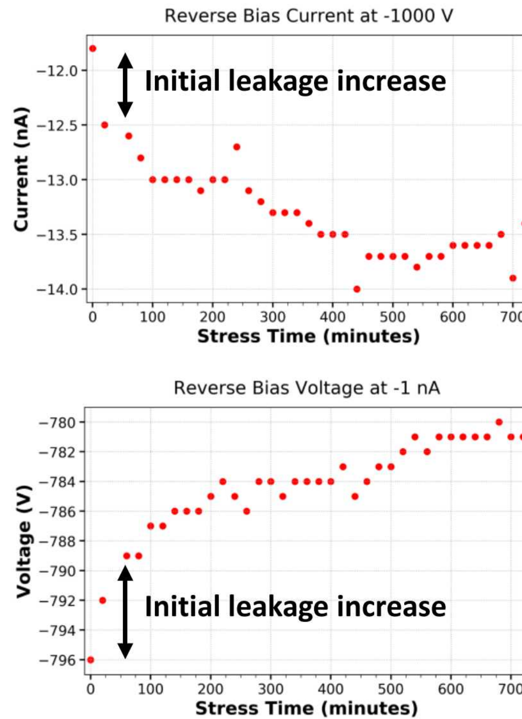
Forward Bias

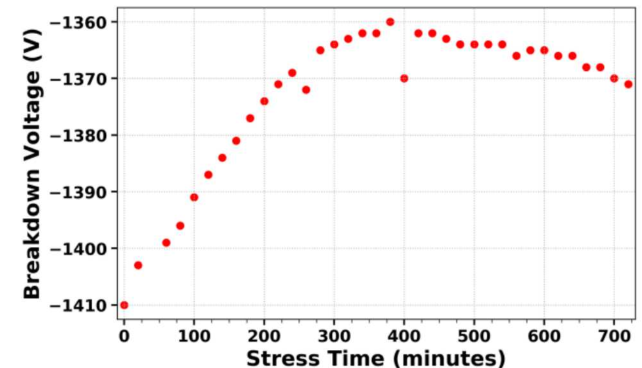


Reverse Bias



Small initial change in reverse leakage current, followed by stable operation

Breakdown Voltage



- Initial decrease in breakdown voltage
- Saturates and reverses midway through stress

1000 V Pulsed Stress Measurements

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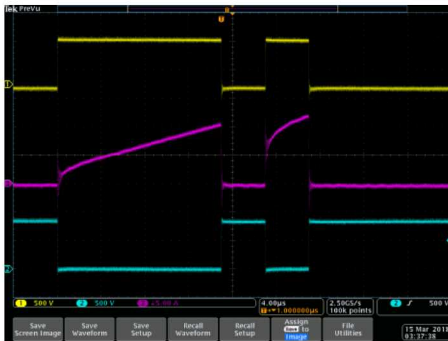
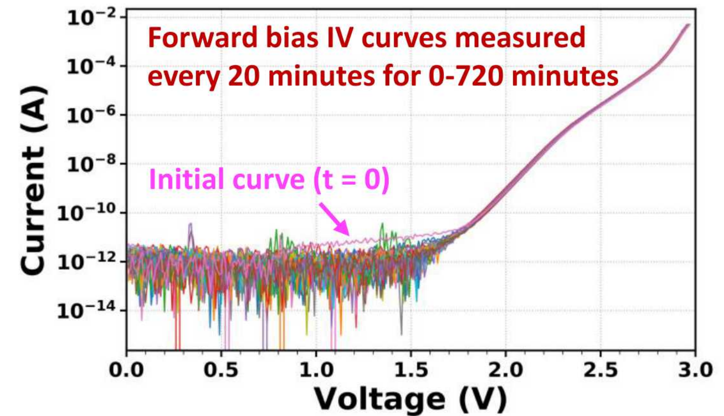
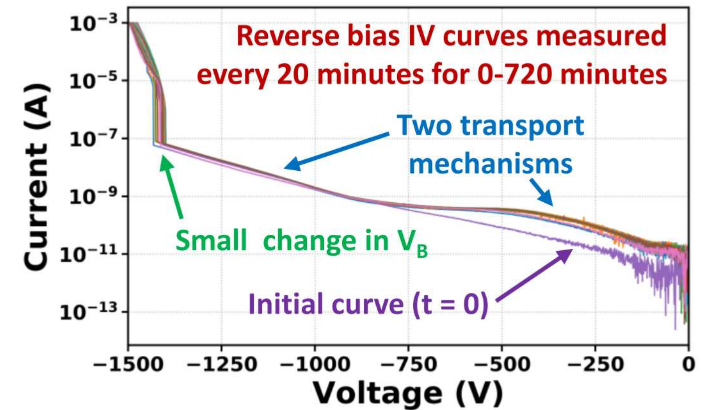
Double Pulse Pre-Stress



Double Pulse Post-Stress





Diode voltage

Switch current

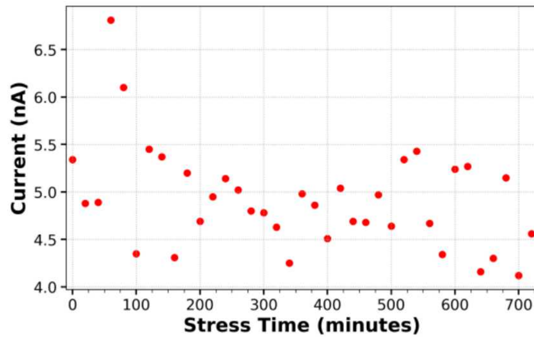
Switch D-S voltage

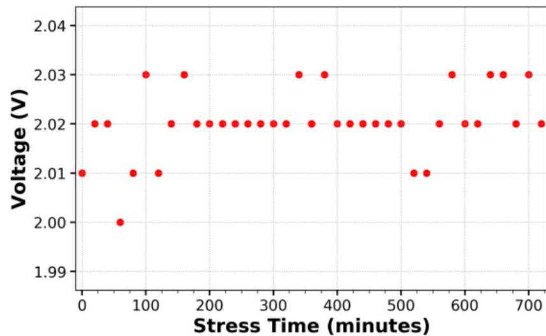
Stress Pulse

Results are similar to 750 V stress case

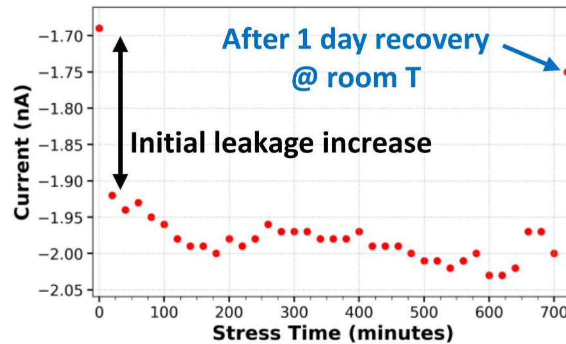
Parametric Drift During 1000 V Pulsed Stress

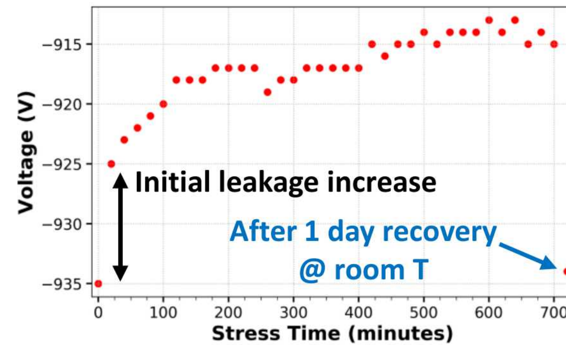
Forward Bias



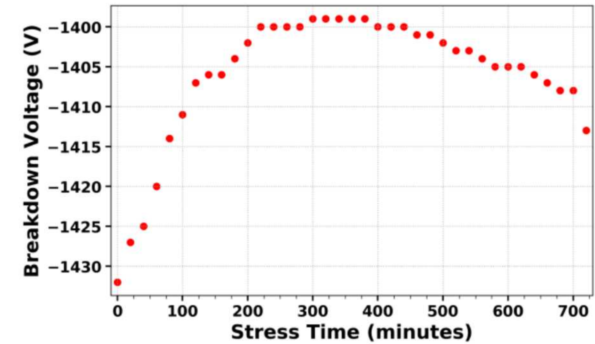


Reverse Bias





Breakdown Voltage



Breakdown behavior is similar to 750 V case

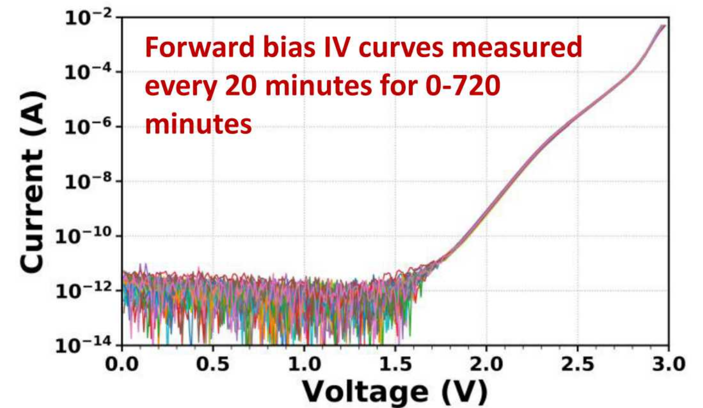
- **Behavior is similar to 750 V stress case**
- **Thermal recovery suggests that degradation mechanism involves carrier trapping**

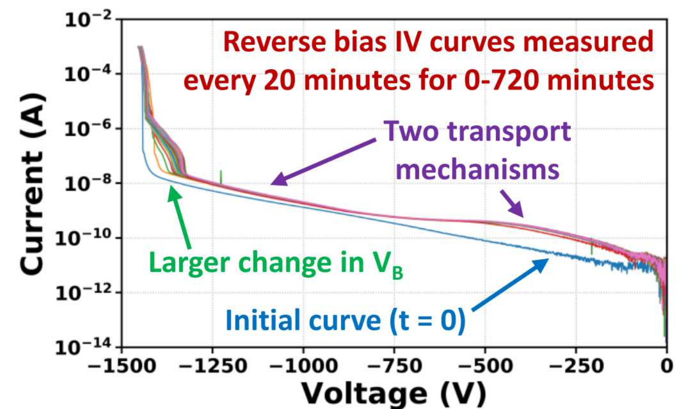
1170 V Pulsed Stress Measurements

Sandia National Laboratories

Double Pulse Pre-Stress

Double Pulse Post-Stress

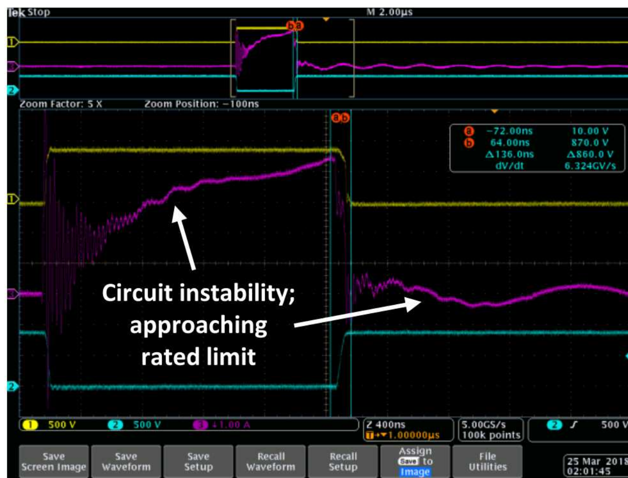




Diode voltage

Switch current

Switch D-S voltage



Stress Pulse

- Leakage results similar to lower V stress cases
- Change in V_B is larger and more complex

Parametric Drift During 1170 V Pulsed Stress

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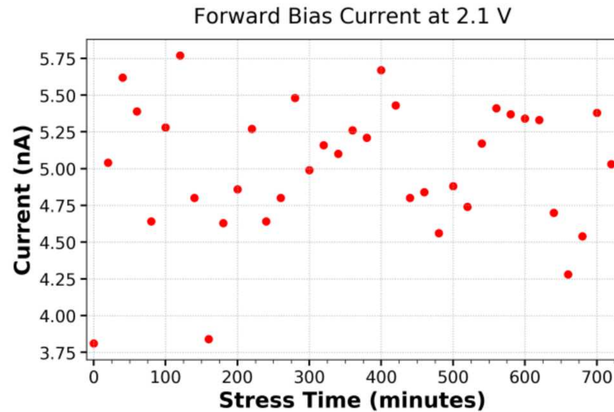
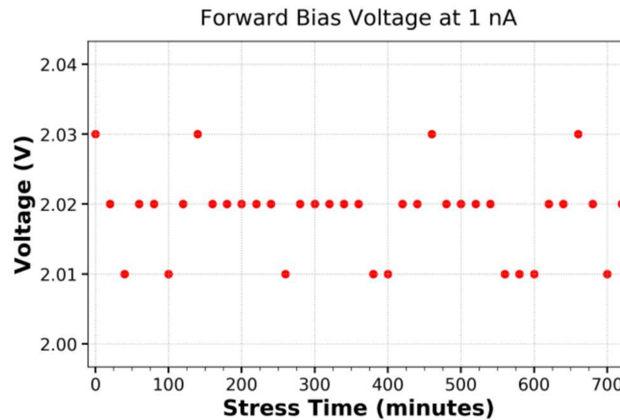
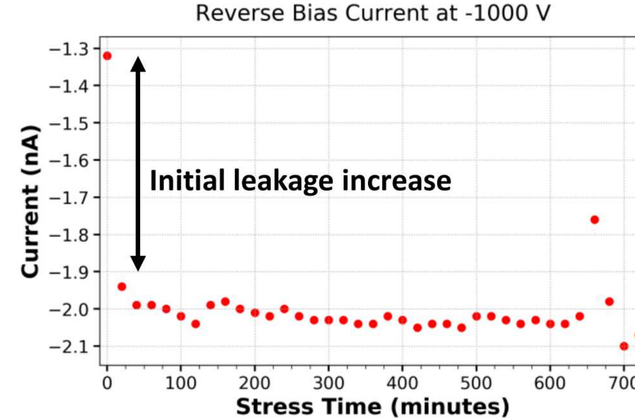
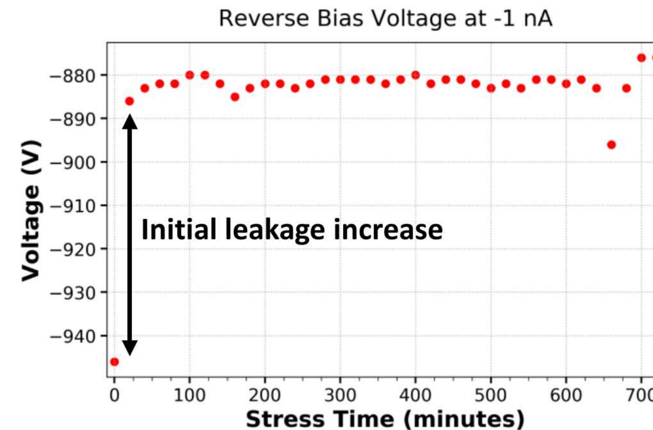
Forward Bias





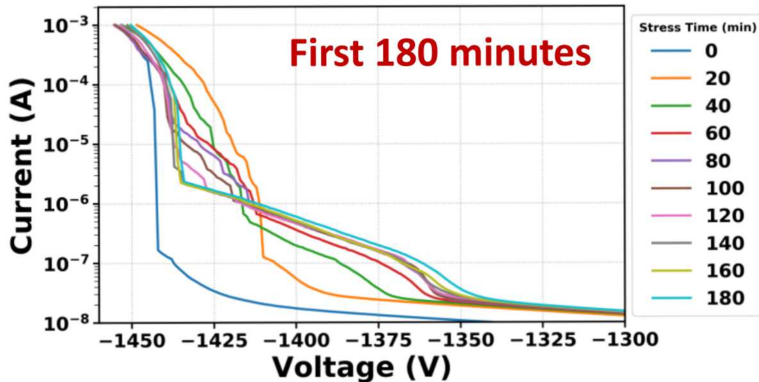
Reverse Bias

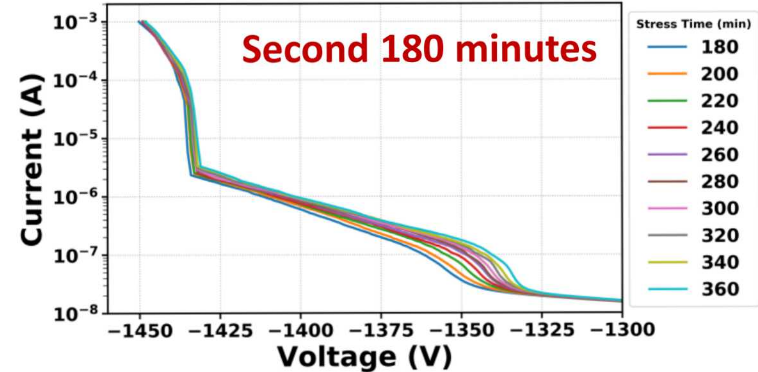


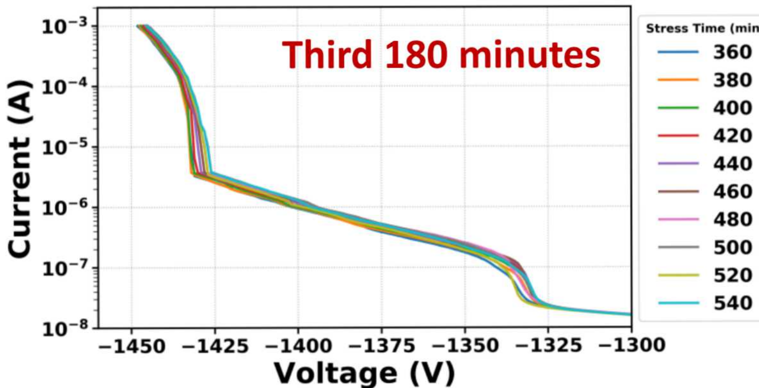


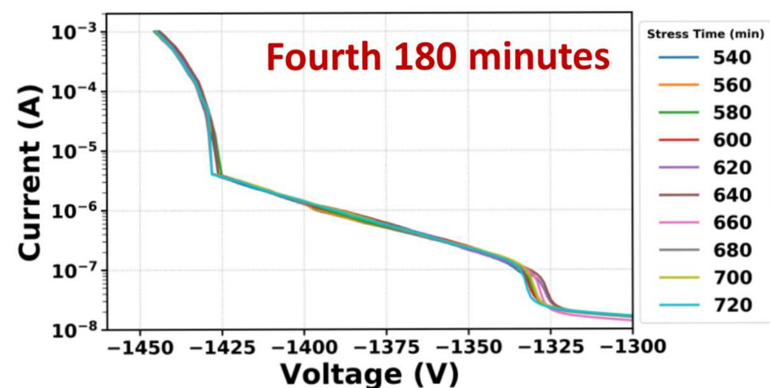
Again, small initial change in reverse leakage current, followed by stable operation

Evolution of Breakdown Voltage During 1170 V Pulsed Stress









- Looks like “soft” and “hard” breakdown mechanisms evolve with stress time
- Most change occurs within first 180 minutes

Related Topic: Hard-Switching Reliability of Power GaN HEMTs

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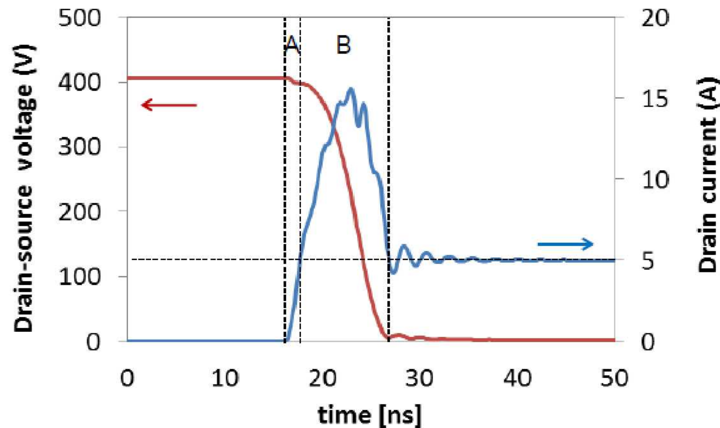
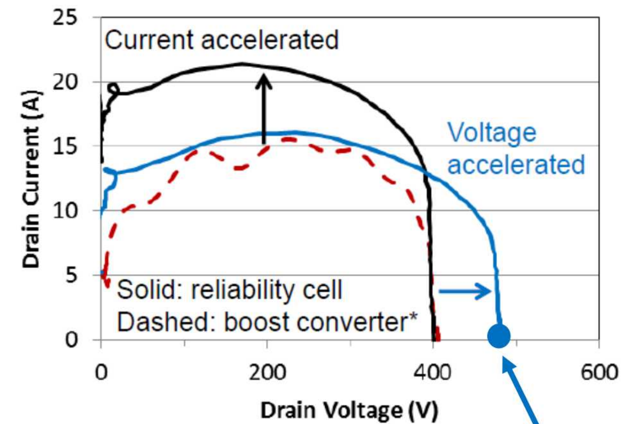
Hard-switching waveforms – current overshoot, and overlap of high current and high voltage



Switching locus – many voltage/current combinations experienced during switching



Traditional HTRB static test point

- **Completely inadequate to test for the range of conditions experienced by the device during hard switching!**

HEMTs subjected to many forms of stress during hard-switching:

- **Hot-carrier effects**
- **Time-dependent dielectric breakdown**
- **Over-current due to fast dV/dt**
- **High power dissipation**

S. Bahl et al., "Product-Level Reliability of GaN Devices," Proc. IRPS 4A-3 (2016)

New JEDEC Guidelines Will Incorporate Hard-Switching Reliability Testing

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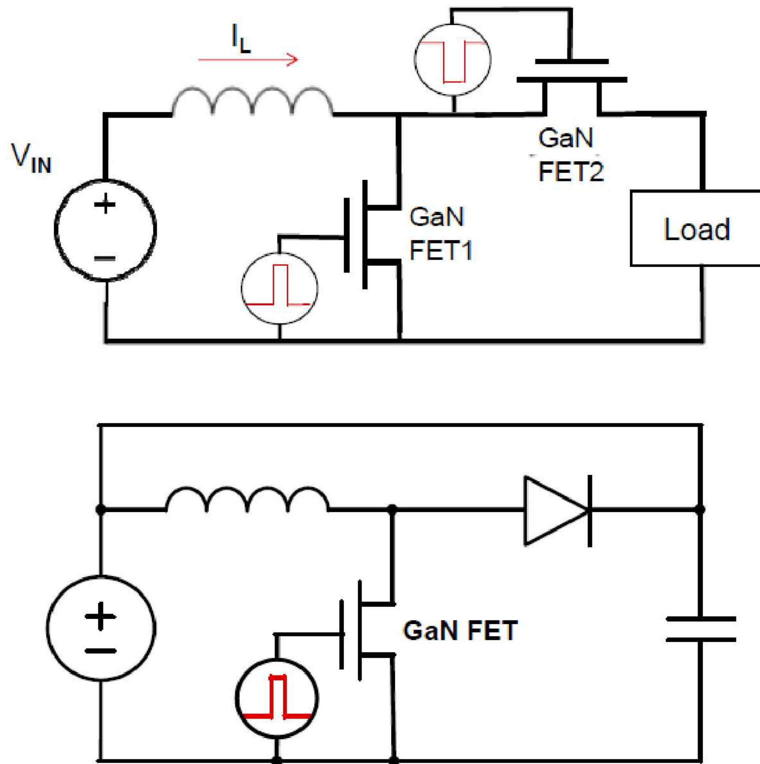
Another way to look at the DPTC – a boost converter with the input and output tied together



Newly-formed JEDEC committee JC70.1 is creating guidelines towards standardization of reliability evaluation for GaN power devices

- **Several important topics identified, one of which is hard switching reliability**
- **New tests will compliment traditional tests such as HTRB**
- **Will evaluate the entire switching locus and will thus encompass effects such as hot-carrier degradation and TDDB**
- **DPTC circuit proposed as standard test vehicle**
- **Broad international input from industry, academia, and national labs**

S. Bahl et al., "Product-Level Reliability of GaN Devices," Proc. IRPS 4A-3 (2016)

Summary

Sandia National Laboratories

- Vertical GaN may offer advantages compared to SiC and lateral GaN
  - Higher critical electric field
  - Avalanche breakdown
  - Early research stage, many outstanding questions including reliability
- Utilized double-pulse test circuit to evaluate switching reliability of 1200 V Avogy vertical GaN PiN diodes
  - Tested at 500, 750, 1000, and 1170 V in continuous-pulse mode
  - Reverse leakage at low bias increases after short stress time and saturates
  - Recovers after sitting for a day – suggests trapping mechanism is responsible
  - Breakdown voltage decreases slightly with stress time, and may recover or show "soft" and "hard" behavior depending on stress voltage
  - *Overall, the devices are robust over the range of conditions tested*
- The same circuit may be used for reliability testing of GaN HEMTs
  - JEDEC is examining this for standardization – JC70.1

We thank the DOE Office of Electricity Energy Storage Program, managed by Dr. Imre Gyuk, for funding the work at Sandia National Labs