An Image Sensor Capable of Detecting Nano-Ampere Transient Signals with Strong Background Illumination

Dahlon D. Chu
Custom Microcircuits & NV Memories
MS1074, Sandia National Laboratories
Albuquerque, NM 87185-1074
Fax: (505) 844-8480, Tel: 844-0173
email: ddchu@sandia.gov

Dean A. Dixon
Sensors and Electronics
MS0972, Sandia National Laboratories
Albuquerque, NM 87185-0972
Fax: (505) 845-0793, Tel: 845-8910
email: dadixon@sandia.gov

Donald C. Thelen Jr.
Microelectronics Research Center
2650 Yale SE,University of New Mexico
Albuquerque, NM 87106
Fax: (505) 277-9719, Tel: 277-9717
email: dthelen@mrc.unm.edu

ABSTRACT

A readout detector integrated circuit (IC) has been developed which is capable of detecting nano-ampere photo-current signals of interest in a high (micro-ampere) background illumination or DC noise level (SNR=92dB). The readout detector sensor IC processes transient signals of interest from a separate photodiode array chip. Low noise signal conditioning, filtering, and signal thresholding implement smart sensor detection of only "active pixels." This detector circuit can also be used to perform signal conditioning for other sensor applications that require detection of very small signals in a high background noise environment.

INTRODUCTION

Most imaging systems use focal plane arrays (FPA) consisting of charge coupled devices (CCD). These imagers sample the charge produced at each pixel at a specified frame rate (e.g., 30 frames/sec). The CCD's readout circuitry measures the total charge at each pixel and generates serial data streams of raw signal data. Because of the serial format of pixel data from CCD imagers, very high pixel data frame rates (100Khz) are difficult to achieve. The entire focal plane must be scanned in a sequential fashion and the serial data stream is processed off chip. Hence, imaging systems using CCDs result in a large amount of raw pixel data that must be signal conditioned, digitized, and processed off chip. Moreover, all of the FPA data is read out without thresholding in a serialized fashion requiring an enormous amount of CPU data processing and high power consumption. We have chosen to take a different approach in

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our image sensor system that will only process selected "active" pixels. Active pixels are photodiode pixels which produce photo-current signals within a frequency band of interest and exceed a threshold current level. In our application, we are not interested in most of the information in a whole image, but primarily in observing transient signals such as lightening or astronomical events. These signals require very high image sampling rates compared with video image processing frame rates.

Our sensor interface chip processes analog signals from each pixel in parallel. Only the relevant pixel data information is sent downstream for digitization and processing by a CPU. This results in a dramatic reduction in the amount of data processed by the CPU, and reduced power consumption compared with conventional CCD imaging techniques. Instead of reading out every pixel serially at a high frame rate and digitizing all the data from the sensor, only those pixels that fall within a 100Hz to 30KHz bandwidth, and exceed a nano-ampere threshold are digitized. As a result of the bandpass filtering, the dynamic range requirements for the A/D converter (ADC) are relaxed because the large background image intensity (micro-ampere) is removed from the small transient signal of interest. High frequency noise is also removed before the digital conversion which avoids aliasing. The bandpass filter is changed to a low pass filter when the threshold is exceeded, and the previous background signal level (image) is stored while the transient signal data is collected. By processing data from those pixels which are within the bandpass frequencies and which exceed a threshold current, only relevant pixel data is sent to the ADC and the digital processor. Moreover, because each pixel in the FPA has its own dedicated front-end sensing module, all the pixels are sensed in parallel at a high bandwidth, and with nearly a 100 percent duty cycle.

Innovative circuits were used to create a three pixel version of the readout detector chip. This prototype was designed to meet the power and area constraints of a future higher density pixel array. Evaluation of

this chip demonstrates that the design meets the signal processing requirements of the remote sensing system. In addition, it is capable of functioning in a satellite radiation environment of 100Krads.

CIRCUIT DESCRIPTION

The readout detector will monitor transient signals that are much smaller than the total background illumination level. Only frequency band limited signals above an adjustable threshold level are digitized and sent to the signal processor. This preprocessing in the parallel front end electronics greatly reduces the amount of data transmitted to and processed by the local CPU. The reduction in the amount of digital data also enhances the low noise environment and reduces the power required by the output drivers. The system requirements of the satellite based sensor resulted in several technical challenges for the implementation of the readout detector electronics.

1) Input referred noise less than or equal to the photodiode shot noise.

2) On-chip 100Hz to 30KHz band pass filtering of photodiode signal.

3) Ability to adjust and disable the low frequency (100Hz, 200Hz, 300Hz, etc.) high pass pole.

4) Hold the DC background signal (static background image) subtraction for several seconds.

Figure 1 shows a block diagram of a single pixel readout detector circuit. A transimpedance amplifier converts the current from the photodiode to voltage which then goes through a gain stage that also serves as a 30KHz low-pass filter. Next, DC and low frequency (< 100Hz) noise components of the signal are removed by a switched-capacitor integrator feeding back to the input of the transimpedance amplifier. Finally, an autozeroed comparator with an adjustable trigger level detects signals of interest. It causes the background subtract circuit to freeze, and permits an ADC downstream to digitize data from this active pixel and to be processed by an external CPU. The switched capacitor integrator is clocked at 1KHz, which causes some of the noise generated by the transimpedance amplifier to be aliased. The

1KHz clock was necessary to keep the capacitor ratios small (16:1). The clock is skewed to a 99 percent duty cycle to maximize the time that the circuit looks for signals of interest.

The present version of the readout detector circuit has a transimpedance amplifier implemented using a high gain low noise opamp with feedback resistors. An improved version of the transimpedance amplifier circuit has been designed as shown in Figure 2. Based upon simulation results, this circuit offers even better noise performance and consumes much less power than the existing transimpedance amplifier. It uses a low noise current buffer scheme with large resistors to develop the voltage output signal. This transimpedance amplifier has been fabricated and is awaiting performance evaluation.

In order to obtain low signal sensitivity (nano-ampere), special circuit design techniques were used such as: low noise input stages, high-gain fully differential CMOS amplifiers, switched capacitor integrators, and autozeroed circuitry. Differential circuits were important to improve power supply rejection, and cross talk rejection. Differential switched capacitor circuits also improve the signal to noise ratio by a factor of the square root of two compared with single ended circuits of the same area. The ability to hold the background level for several seconds was made possible with a differential integrator. Leakage on the switches between the sampling capacitor and the opamp will be seen as a common mode signal, and rejected by the common mode feedback circuit. Close attention was also paid to the cell and chip layout using matched and common-centroid layout techniques in order to reduce input offsets and to optimize the design. Special care was also taken to keep voltage drops from power supply currents off of the substrate. A separate power supply connected only to the substrate helps to isolate adjacent channels from one another, and keeps digital noise off the sensitive analog circuits. We used p-well resistors in the transimpedance amplifier. These resistors are known to have several problems including a non-linear voltage to current relationship, distributed parasitic capacitance, large process variation, and large temperature coefficient. Using differential circuits cancels the odd order non-linearities of the p-well

resistors. Simulations show that the distributed capacitance does not cause sufficient phase shift to cause instability. The gain variation caused by the large resistor process variation and temperature coefficient were compensated for by setting the comparator reference with an external current source and a matched p-well resistor. This chip shown in Figure 3 was fabricated using Orbit Semiconductor's 2μm p-well process.

Figure 4 shows the frequency response of the readout detector measured using a HP 3589A spectrum/network analyzer. A bandpass filter response is shown with -3dB high and low pass corner frequencies at 150Hz and 35KHz respectively. The flatband response shown is at -24dB because the input voltage signal is divided by a 1.2 megaohm resistor to generate a current input signal.

Figure 5 shows the detector output for a 4nA input signal with a 1μA DC offset. Note that the 1μA DC 'noise' component has been filtered out. The graininess of the scope plot is due to the operation of the background subtractor and actual system noise. A step response of the bandpass filter is shown in Figure 6. A 1.36v input (12.36μA via a 110Kohm resistor) step is applied to the readout detector input. We see that the circuit "subtracts" out this DC background current in 8msec (5 time constants) which corresponds to our 100Hz high pass pole.

ACKNOWLEDGMENT

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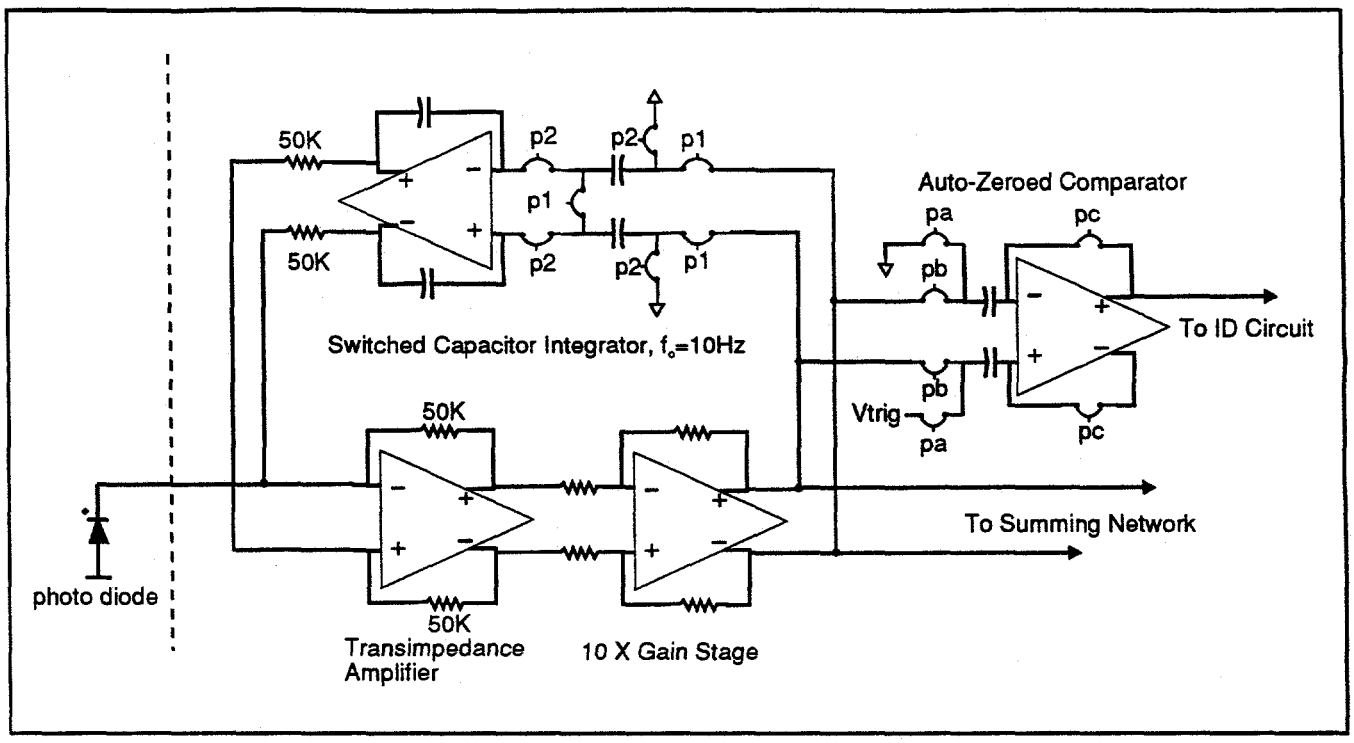

Figure 1. A single pixel readout detector signal processing module.

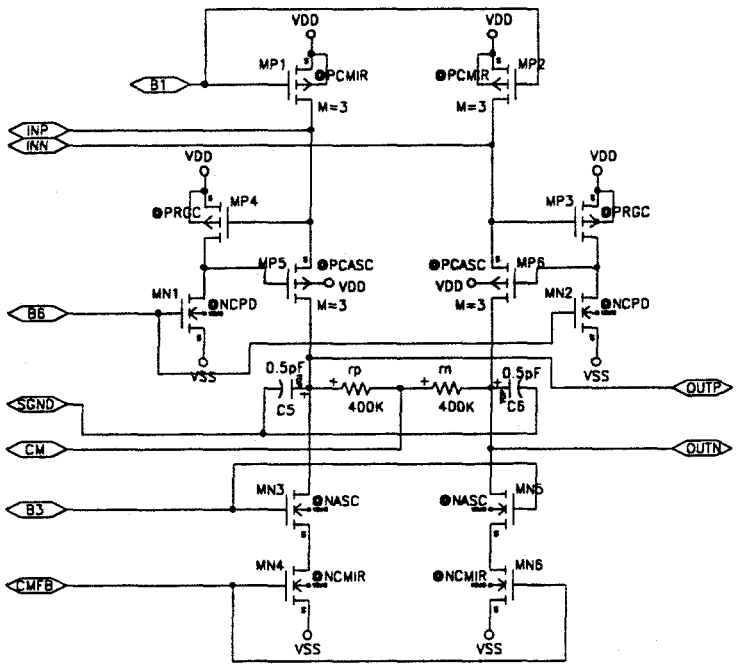

Figure 2. Circuit schematic of an improved version of the transimpedance amplifier.

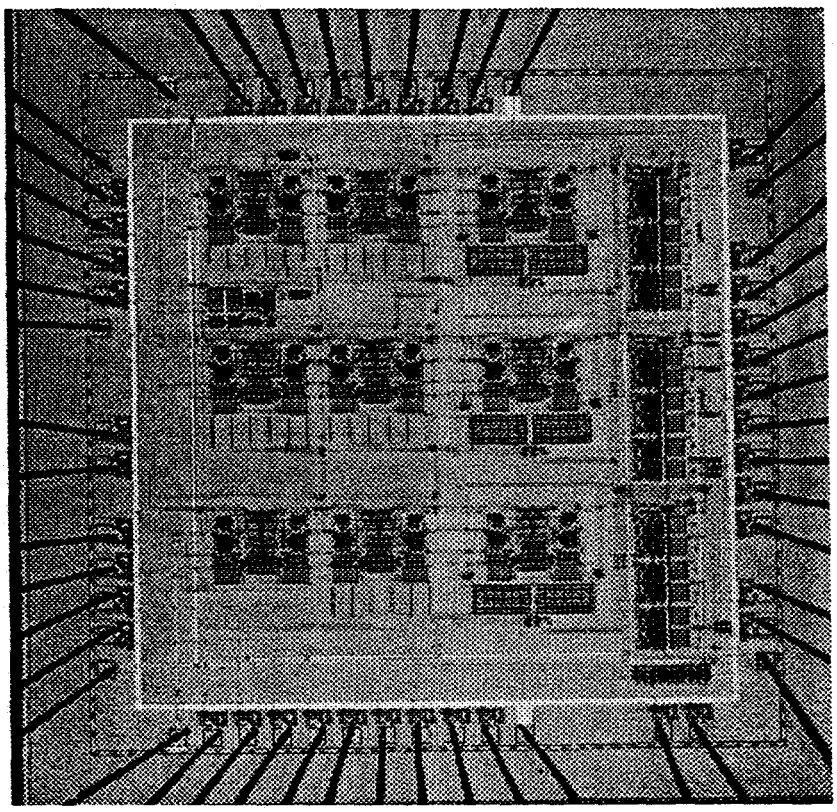

Figure 3. Die photo of the 3 pixel readout detector integrated circuit.

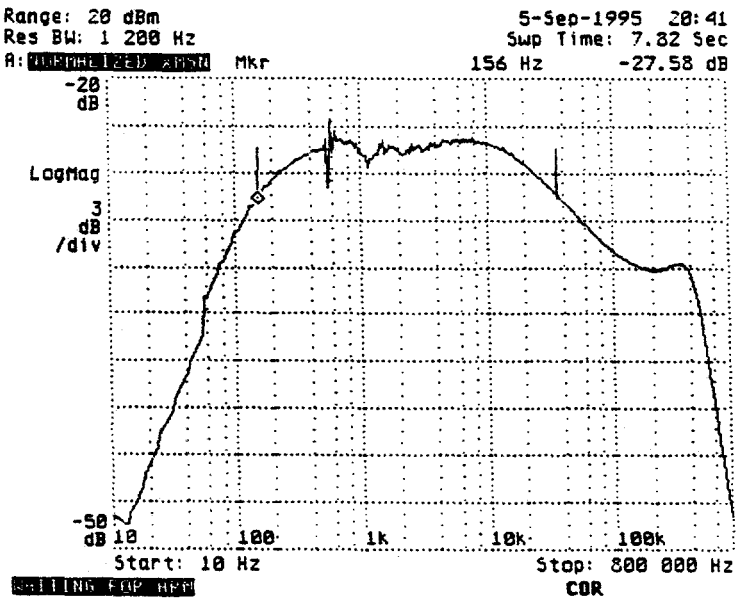

Figure 4. Frequency response of bandpass filter function in the readout detector channel.

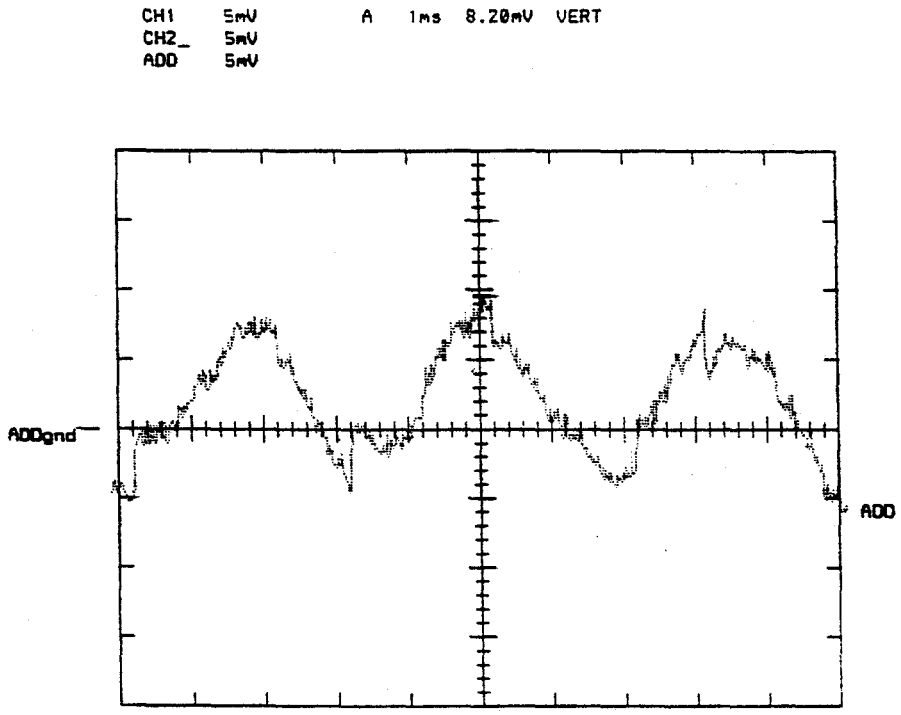

Figure 5. Output signal voltage response from a 4nA input sinusoid with a 1uA DC offset at 300hz.

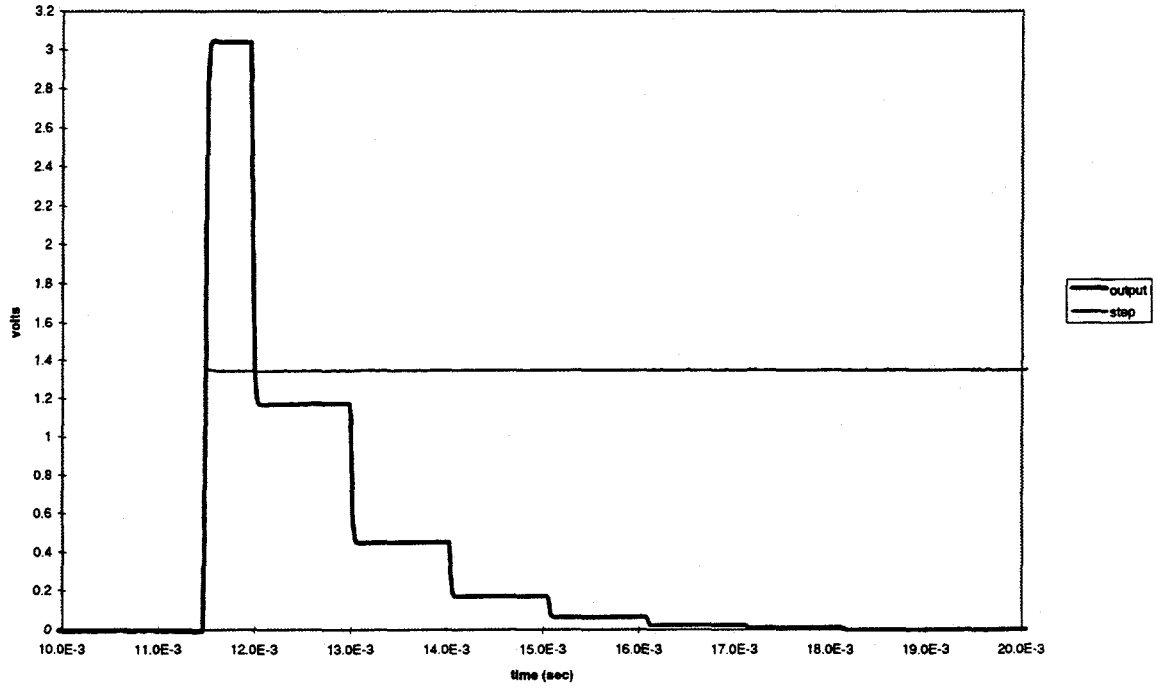

Figure 6. Step response of a readout detector loop.

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