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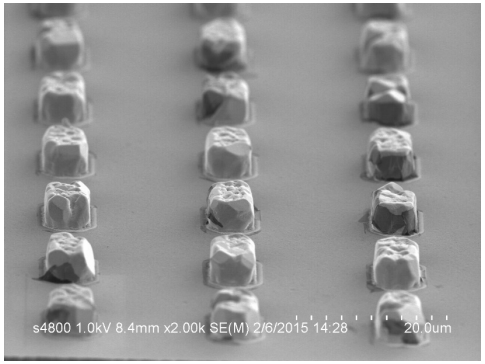

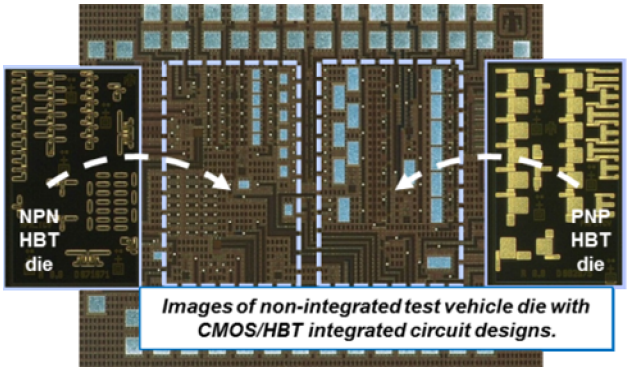

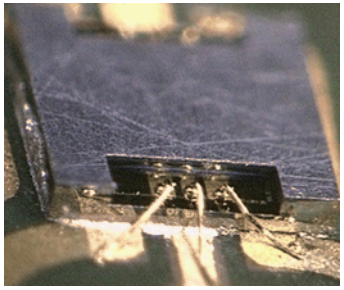

Heterogeneous Integration @ Sandia National Laboratories

Acknowledgement; Sandia Authors

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July 12, 2017

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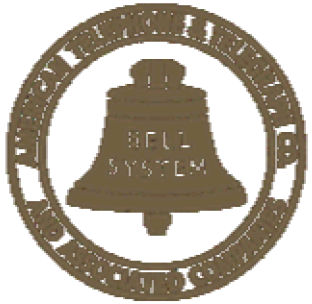
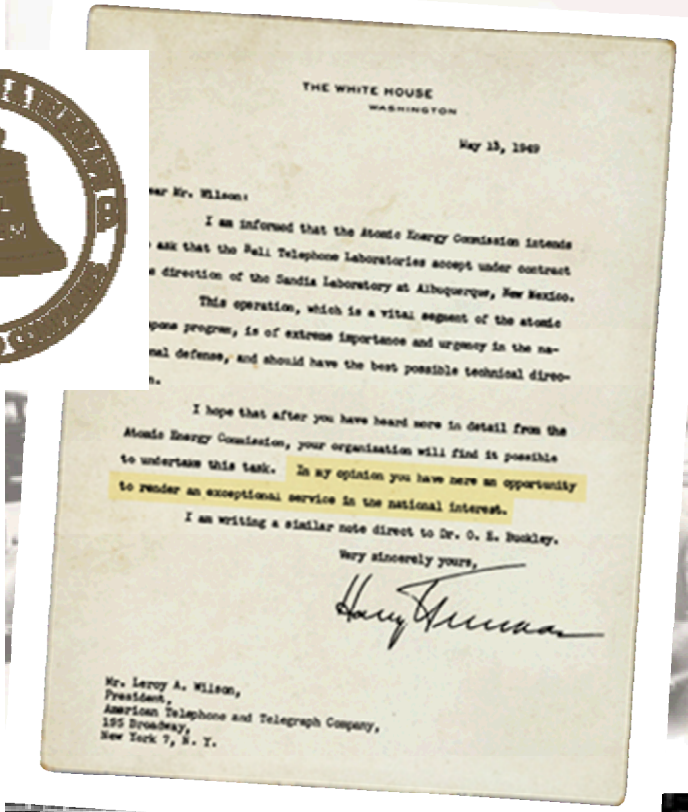
Sandia Corporate Overview

Sandia's History

Exceptional service in the national interest

- July 1945: Los
  creates Z Divi
- Nonnuclear c
  engineering
- November 1,
  Sandia Labora
  established





THE WHITE HOUSE
WASHINGTON

May 13, 1949

Dear Mr. Wilson:

I am informed that the Atomic Energy Commission intends to ask that the Bell Telephone Laboratories accept under contract the direction of the Sandia Laboratory at Albuquerque, New Mexico.

This operation, which is a vital segment of the atomic bomb program, is of extreme importance and urgency in the national defense, and should have the best possible technical direction.

I hope that after you have heard more in detail from the Atomic Energy Commission, your organization will find it possible to undertake this task. In my opinion you have here an opportunity to render an exceptional service in the national interest.

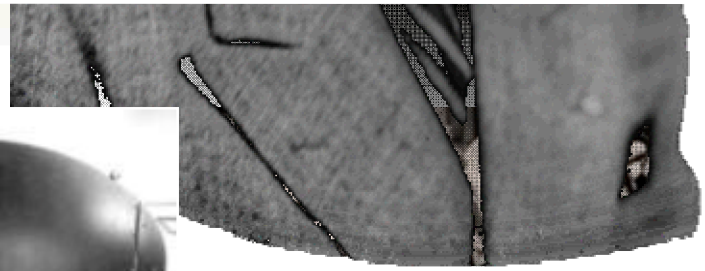
I am writing a similar note direct to Dr. O. E. Buckley.

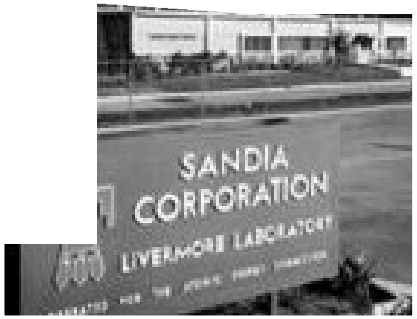
Very sincerely yours,

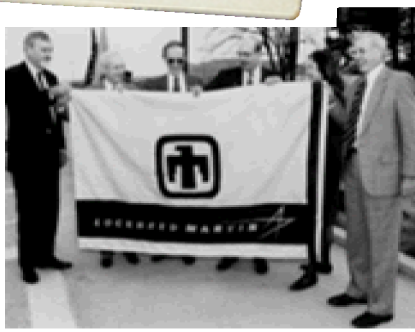
Harry Truman

Mr. Leroy A. Wilson,
President,
American Telephone and Telegraph Company,
195 Broadway,
New York 7, N. Y.

to undertake this task. In my opinion you have here an opportunity to render an exceptional service in the national interest.







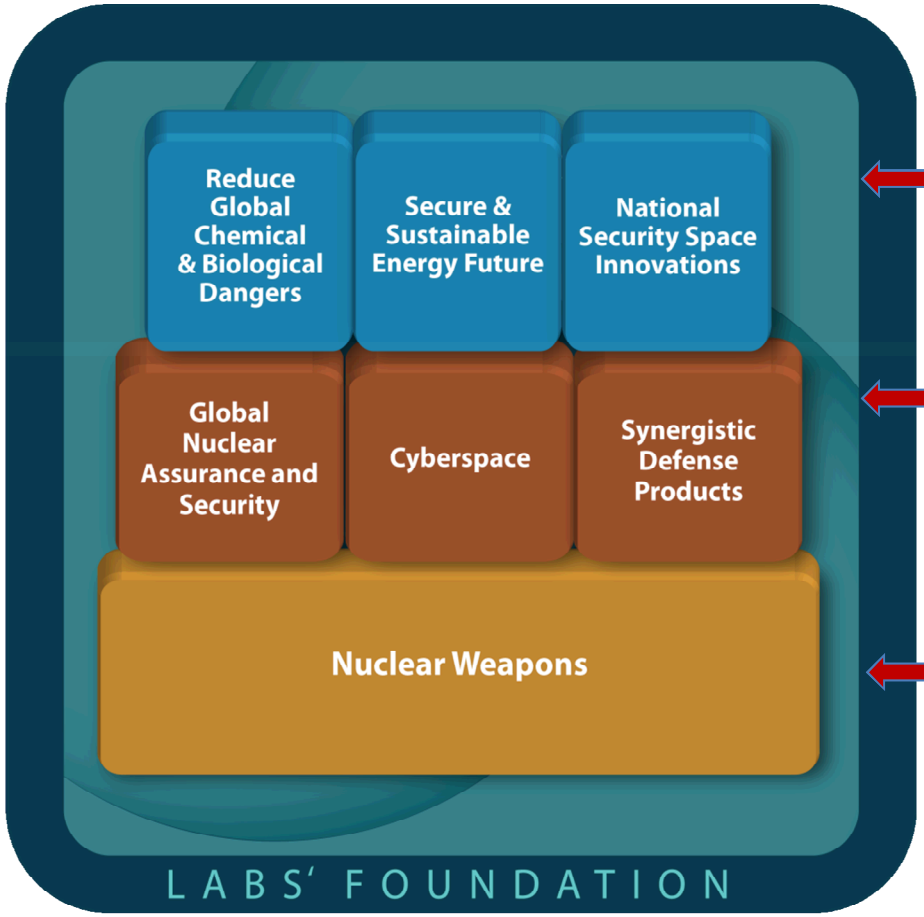
Governance of Sandia Laboratories

Sandia Corporation

- AT&T: 1949–1993
- Martin Marietta: 1993–1995
- Lockheed Martin: 1995–2017
- National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc.: 2017-present
- Government owned, contractor operated

Federally funded research and development center

National Security Focus Areas



- Top row: Critical to our national security, these three mission areas leverage, enhance, and advance our capabilities.
- Middle row: Strongly interdependent with NW, these three mission areas are essential to sustaining Sandia's ability to fulfill its NW core mission.
- Bottom row: Our core mission, nuclear weapons (NW), is enabled by a strong scientific and engineering foundation.

Sandia Addresses National Security Challenges

1950s	1960s	1970s	1980s	1990s	2000s	2010s
Nuclear weapons	Development engineering	Multiprogram laboratory	Missile defense work	Post–Cold War transition	START Post 9/11	LEPs Cyber, biosecurity proliferation
Production and manufacturing engineering	Vietnam conflict	Energy crisis	Cold War	Stockpile stewardship	National security	Evolving national security challenges

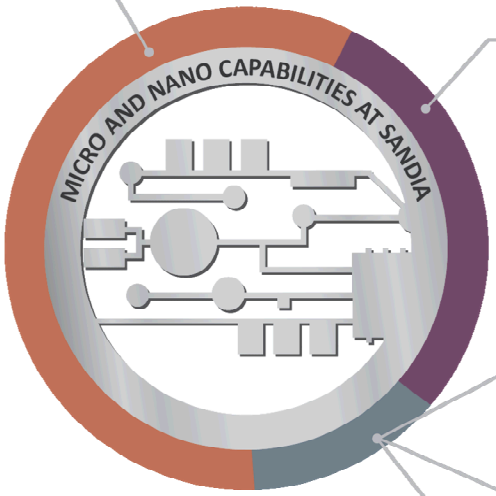
Sandia National Laboratories

Microsystems and Engineering Sciences Application (MESA)

Unique Facilities Differentiate Sandia's Micro/Nano R&D

MESA

MICROSYSTEMS
ENGINEERING SCIENCES
AND APPLICATIONS



CDC

COUNTERFEIT
DETECTION CENTER

CINT

CENTER FOR INTEGRATED
NANOTECHNOLOGIES

IBL

ION BEAM LABORATORY

ACRR

ANNULAR CORE
RESEARCH REACTOR

- Only source for custom strategic rad-hard microelectronics
- Largest government-owned foundry
- FFRDC with the broadest and deepest micro and nano expertise [derived R&D-product delivery work mix]

What is MESA?

Sandia National Laboratories

- Microsystems and Engineering Sciences Applications (MESA) is a $462M FFRDC-based development and production facility for any microsystem component or technology that cannot or should not be obtained commercially.

- MESA Develops and Delivers:
  - Strategic radiation-hardened custom integrated circuits (ICs)
  - Digital/Analog/Mixed-Signal/RF ICs
  - Trusted Products and Designs
  - 5-Level MEMS
  - III-V Compound Semiconductors
  - Optoelectronic/Photonic Devices
  - High-speed/RF Electronics
  - Qualified COTS
  - Failure Analysis/Reliability Physics
  - Advanced Packaging
  - Specialized Sensors

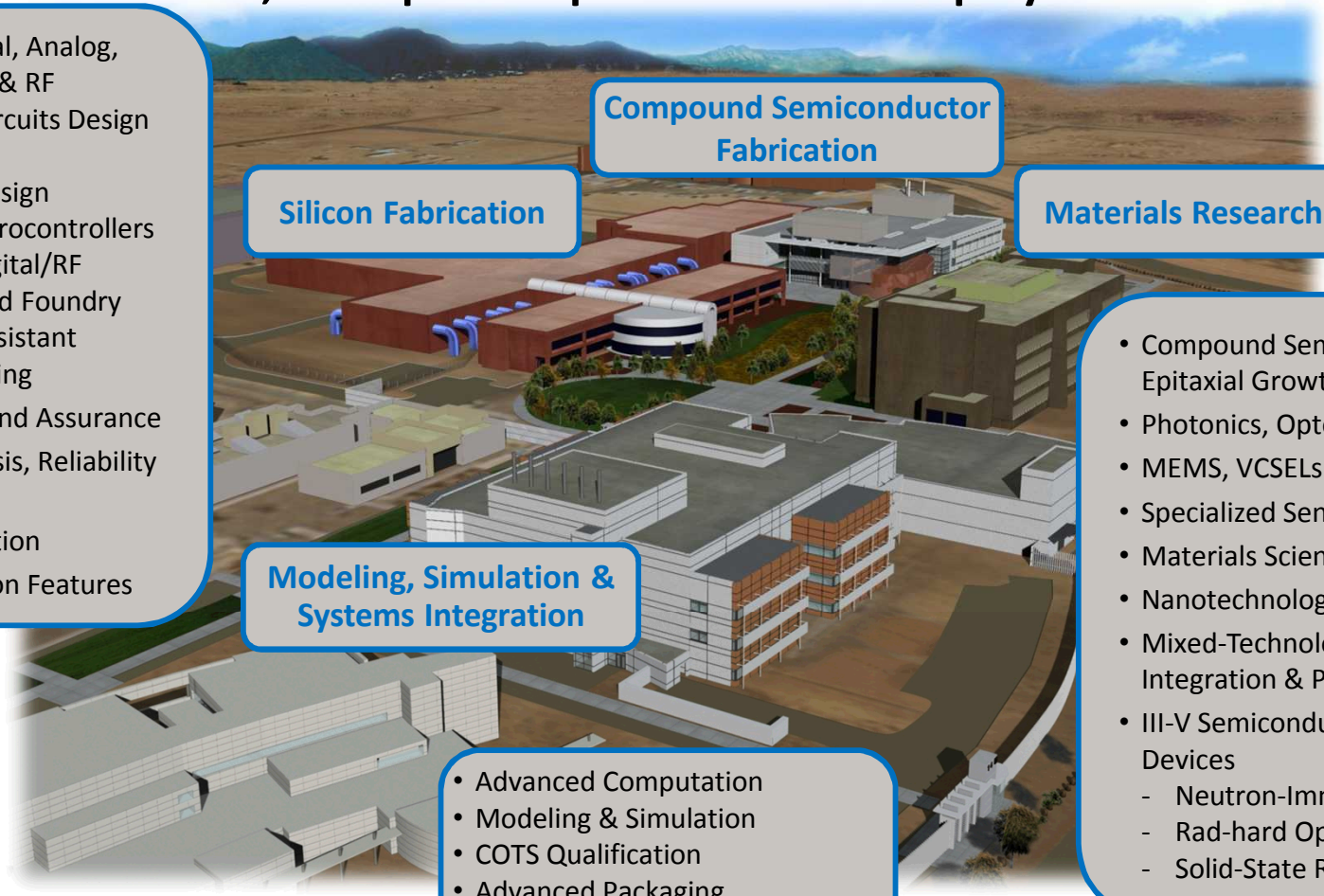
MESA bridges science to systems, providing an environment where multidisciplinary teams create ***microsystems-enabled*** solutions to our nation's most challenging problems.

Microsystems and Engineering Sciences Applications (MESA)

Sandia National Laboratories

400,000 Sq-ft Complex with >650 Employees

- Trusted Digital, Analog, Mixed Signal & RF Integrated Circuits Design & Fabrication
- Custom IC Design
  - Secure microcontrollers
  - Analog/Digital/RF
  - IBM Trusted Foundry
  - Tamper Resistant
- Micromachining
- RAD Effects and Assurance
- Failure Analysis, Reliability Physics
- Test & Validation
- 3-D Integration Features



- Advanced Computation
- Modeling & Simulation
- COTS Qualification
- Advanced Packaging
- Custom Electronic Components
- System Design & Test

- Compound Semiconductor Epitaxial Growth
- Photonics, Optoelectronics
- MEMS, VCSELs
- Specialized Sensors
- Materials Science
- Nanotechnology, Chem/Bio
- Mixed-Technology Integration & Processing
- III-V Semiconductor Devices
  - Neutron-Immune HBT
  - Rad-hard Optical Links
  - Solid-State RF Devices

History of Delivering Trusted Components to National Security Customers

Sandia National Laboratories

Trusted COTS and Custom Electronic Components

- Assure performance, quality & reliability
- Custom magnetics, capacitors, RF, optical, interconnects, transducers, clocks, connectors & cables

Trusted R&D

- Photonic Microsystems
- Acoustic Bandgap Science
- Advanced Sensors
- Quantum Information Processing

Trusted Design

- Secure design facility
- Disciplined design flow & methodologies
- Trusted Structured ASIC
- ISO9001 Certification
- DoD Category 1A Trusted Integrated Circuit Supplier for Design
- Design for Trusted Foundries

Trusted Fabrication

Custom, low-volume, high-reliability

- Silicon custom & radiation-hard process technologies
- DOE/NNSA War Reserve Supplier
- ISO9001 Certification
- DoD Category 1A Trusted Integrated Circuit Foundry

- III-V semiconductor epitaxial growth and processing
- Photonics, Optoelectronics
- Microsensors & Sensored Microsystems
- Microelectromechanical systems

Trusted Integration and Assessment

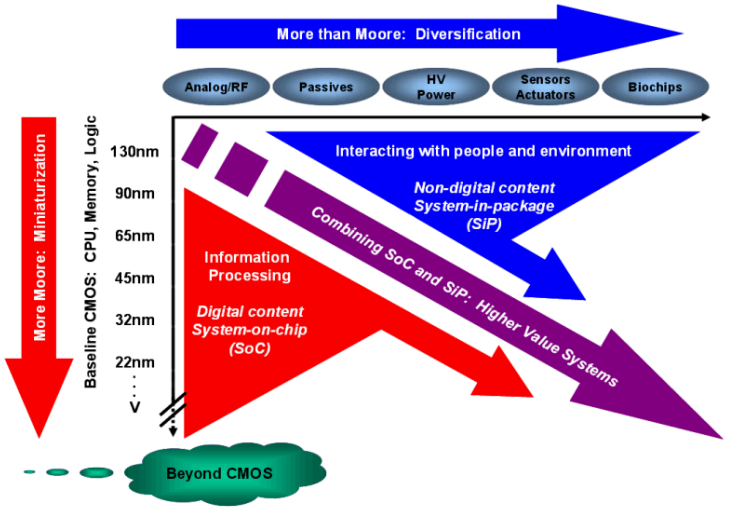
- Advanced Packaging
- 3-D Integration
- Test & Validation
- Failure Analysis & Reliability Physics
- Rad Effects & Assurance

Sandia National Laboratories

Heterogeneous Integration Overview

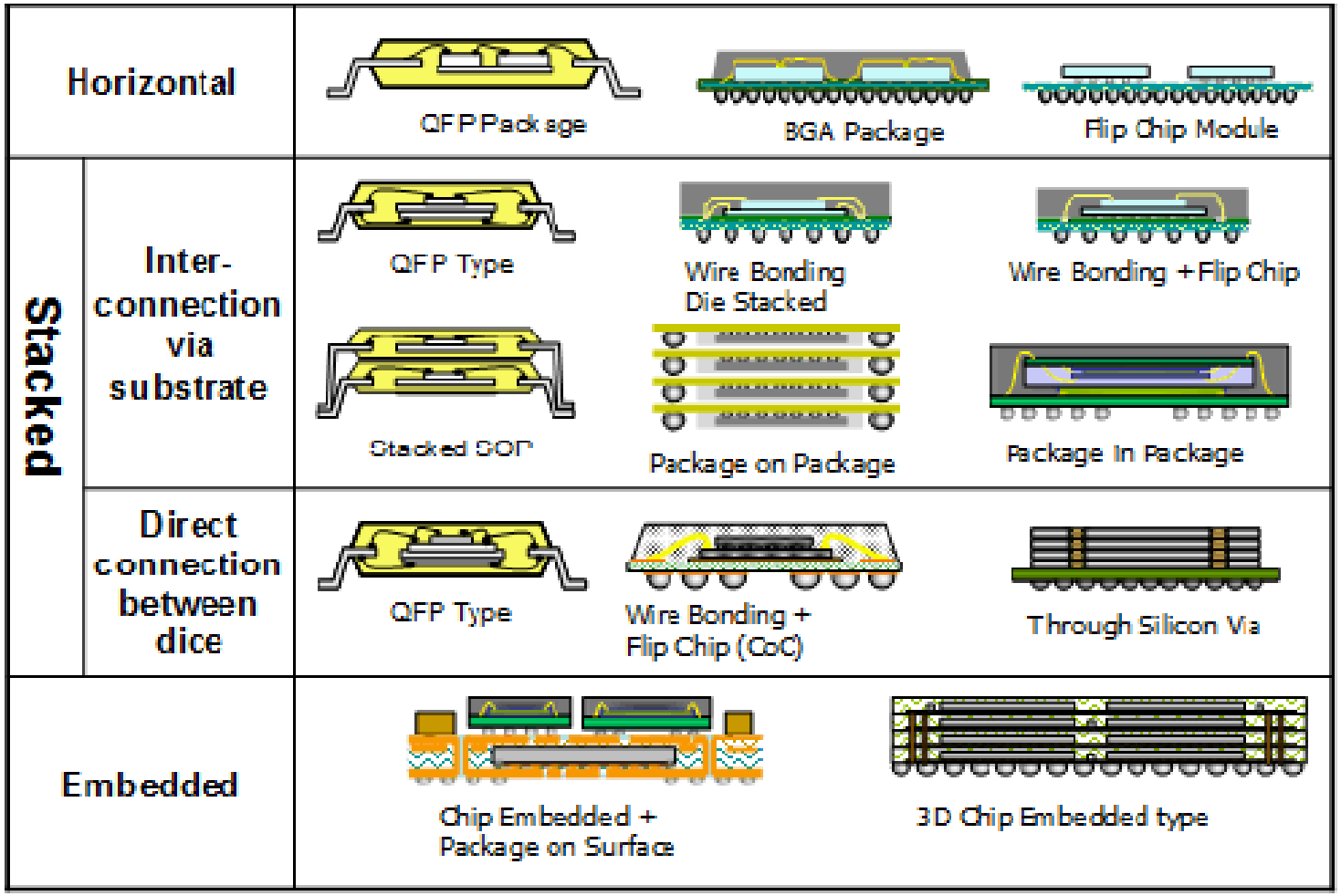
Heterogeneous Integration Overview

- Scope
  - Heterogeneous: diverse, varied, mixed, different
  - Integration: combining separate parts
  - Beyond "post-fabrication" assembly: dense, 3D, interconnects, new materials
- Rationale
  - SWAP-C – size, weight, and power; cost
  - Performance – combining technologies, interconnect density and length
  - Diverse functionality – optical, RF, MEMS, analog, chem, bio, …
  - Trust – Secure environment
- Our customers want performance and more-than-Moore functionality



Source: ITRS Roadmap; 2010

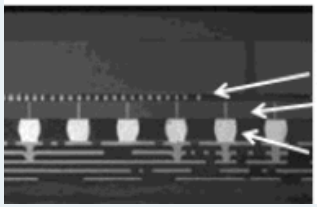
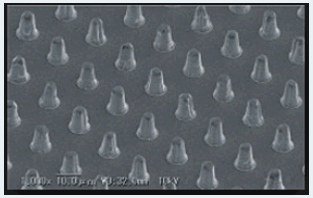
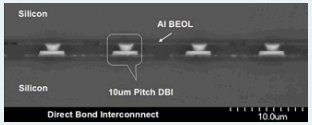
Integration Techniques



- Selected approach is driven by… Application, IP Availability, Performance, …
- Substantial flexibility but… can significantly impact cost & development time

Source: ITRS Roadmap 2.0; 2015

3D Bonding Technology SoA

	C4	µBump	Indium Bump	DBI (Ziptronics®)
Density	Low	Moderate	Moderate	High
Minimum Pitch	300µm	150-20µm	10-15um	3µm
Method	D2D, D2W	D2D, D2W	D2D	W2W, D2W
Underfill	Yes	Yes	Yes	No
Maturity	High	High	High	Moderate
Images				

W2W = Wafer-to-Wafer Bonding
D2W = Die-to-Wafer Bonding
D2D = Die-to-Die Bonding

Integration: Current State / Future State

- **Current State:** Driven by commercial market need for low-cost and high volume OR individually developed integration approaches
  - Commercial: Wafer-level-integration for low-cost, high volume, parts
  - Government: Multi-chip module, interposer, or similar piece-part assemblies
  - Research: Boutique processes for intimate III-V/CMOS integration

- **Desired Future State:** Integrate dissimilar technologies and devices into die-level form factors with high functional density and low parasitic interconnection.
  - Si: MPW CMOS or SiGe die, COTS piece-parts, Si Photonics, Si detectors
  - III-V electronics: GaAs HBT, InP HBT, GaN HEMT, Sb FETs, GaAs opto, InP opto
  - RF technologies: microresonators, high-Q passives, ferrite devices
  - Sensors and Detectors: MEMS, piezoelectric, FPA's, CCD, etc.

Integration: Guiding Principles

Sandia National Laboratories

- Build Microsystems **Around High-Value Functions** in Custom Technologies
  - Focus on truly differentiating technologies and capabilities
  - Buy items that already exist
- Incorporate **Range of Technologies from Multiple Vendors**
  - Integrator has little or no control over process or part details
  - Available as wafers, bare die, or packaged parts
  - Must be able to handle and post-process small parts
- Interconnect and Integration Must **"Unlock" Technology Performance**
  - Three-way compromise: Size, Performance, Cost
  - Different interconnect needs for different applications
- Integration Approach Must Allow for **Fast Turn-Time**
  - Focus energy on desired solution rather than integration
  - Integration can't occupy substantial portion of budget or schedule
  - Desire: From customer inquiry to prototype in <1 month

Research Integration: Challenges

Sandia National Laboratories

- **Customers are interested in Solutions**, not Integration
  - Integration realizes the potential of differentiating technologies
- **Wafer size mismatch** is only getting worse as silicon goes from 6” -> 8” ->12” -> ?
  - GaAs – 6” at best (3” at SNL); GaN – 3” typical; InP – 4”…..
- Limited **availability of whole wafers** of advanced technologies
  - Mostly accessed through MPW runs – individual die only
  - Cost prohibitive to obtain sufficient material for whole-wafer solutions
  - Drives towards die-level integration
- **Through-substrate-vias** are essential but require significant development ($$)
  - Needs and requirements vary from application to application
  - Mixed Signal: small size, high density
  - RF/Microwave: low parasitic capacitance, low resistance, good isolation
- Need **post-processing capability** on bonded die / wafers
  - Reduce footprint and can add functionality
  - High-temperature intimate bonding
- **Thermal management**
  - Need good thermal path from top levels to heatsinks
- MEMS devices require clean **hermetically sealed voids**
  - Additional challenges over just stacking

Sandia National Laboratories

Heterogeneous Integration Capability @ MESA

MESA Heterogeneous Integration

- **Technologies**
  - Indium Bump
  - Oxide-Oxide Bond (DBI/Zibond)*
- **Low Volume**
- **Custom Platforms R&D**
- **Heterogeneous Integration (III-V, Etc.)**
  - III-V (GaAs, InP, Etc.)
  - Resistive Memory (Memristors)
  - Aluminum Nitride (AlN) Resonator
- **Applications**
  - Si
  - Photonics
  - Detectors
  - RF
  - III-V
  - Memory
  - Quantum Devices

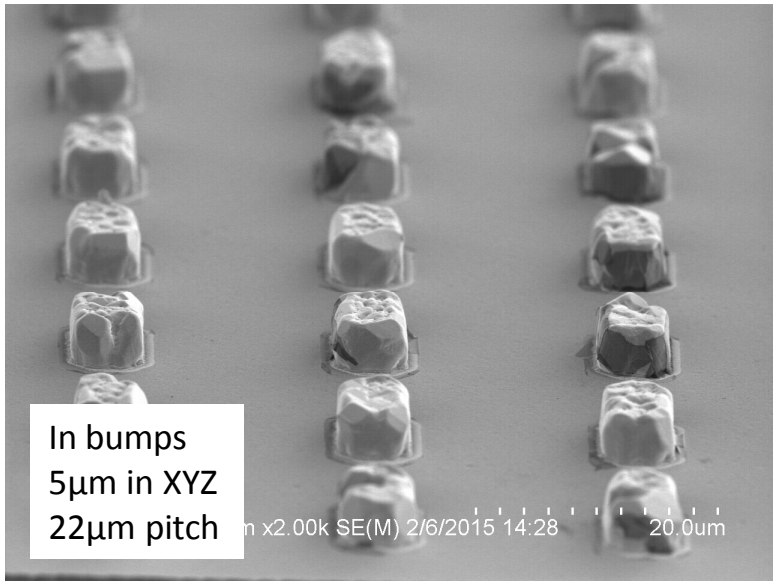
	Indium Bump	Oxide Bond
Density	Moderate	High
Minimum Pitch	10-15µm	<10µm
Method	D2D, D2W	W2W,D2W
Underfill?	Yes	No
Maturity @SNL	Moderate	In Development

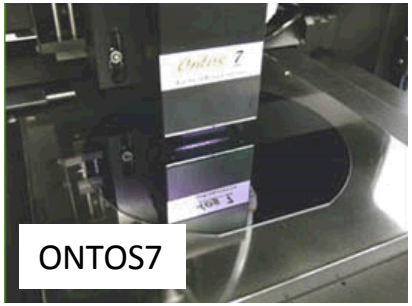
W2W = Wafer To Wafer Bonding
D2W = Die To Wafer Bonding
D2D = Die To Die Bonding

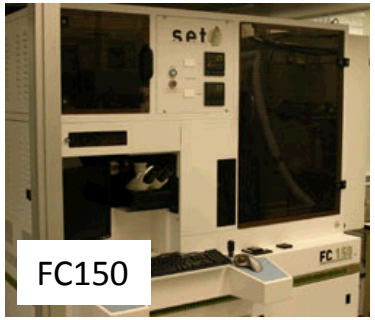
*Licensed From Ziptronix/Invensas.

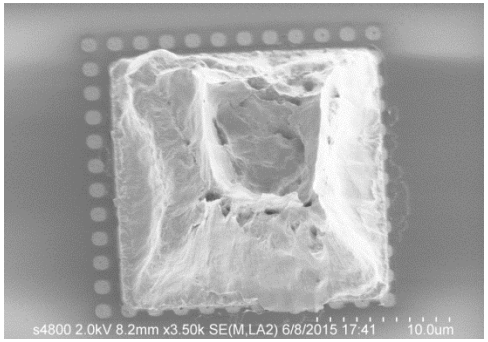
Bump Formation & Flip Chip Assembly

- Bump metallurgies: In and Au, primarily.
  - For In in particular, carefully controlled deposition parameters and careful consideration of UBM.
  - Rigorous inspections during processing to maximize yield.
- Flip Chip Assembly using SET FC150.
  - Three FC150's on site. FC300 planned.
  - CRADA with SETNA in support of DAAHTA.
  - Ontos7 for surface prep prior to assembly.





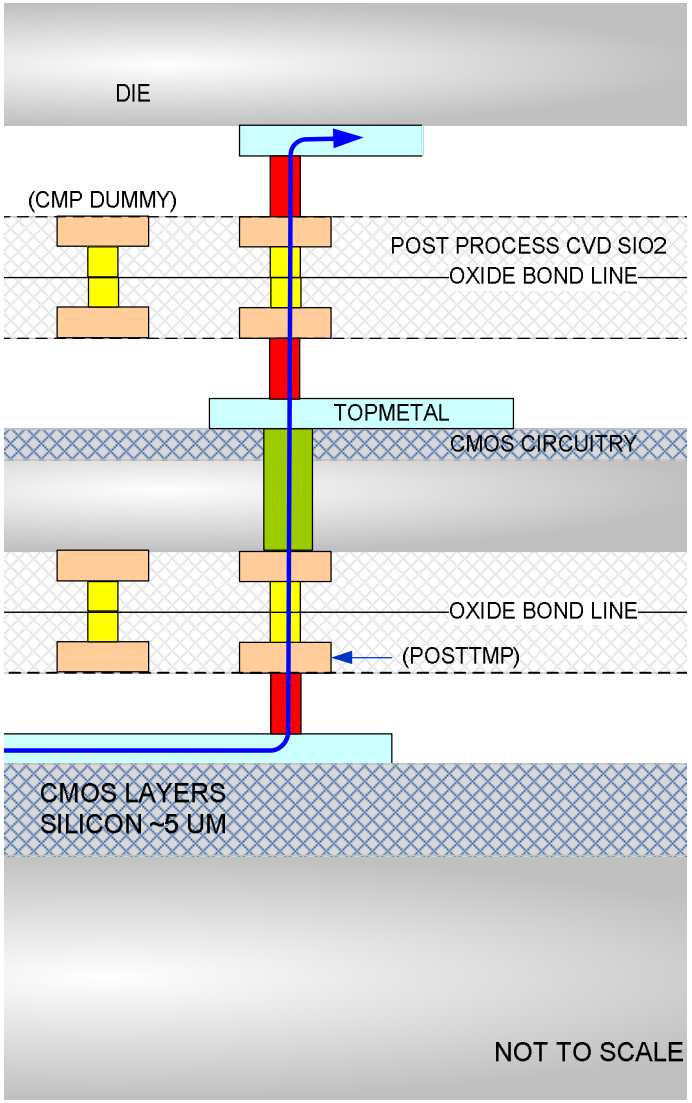




In bump after ductile failure

Direct Bond Interconnect (DBI)*

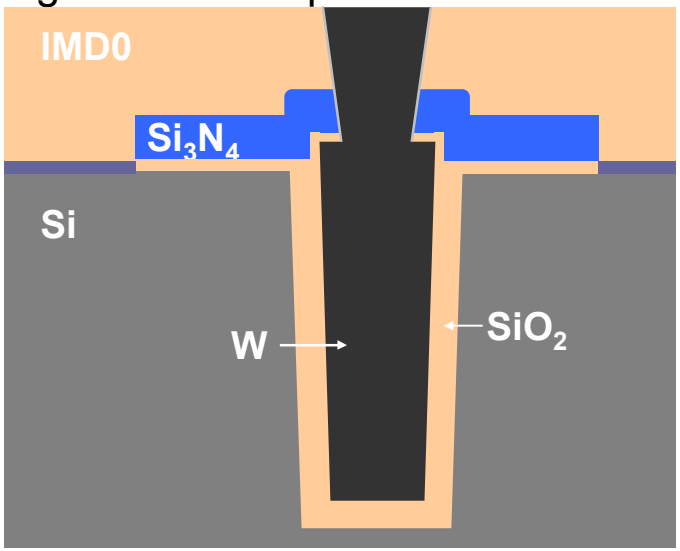
- DBI developed by Ziptronix.
  - Prepare wafers with plugs terminated near dielectric surface.
  - Clean and chemically activate the dielectric surfaces.
  - Precisely align and assemble parts (W2W, D2W).
  - Anneal to permanently bond the dielectrics and form diffusion bond between adjacent plugs.
- Sandia has licensed the technology and is working on process transfer in the µfab.

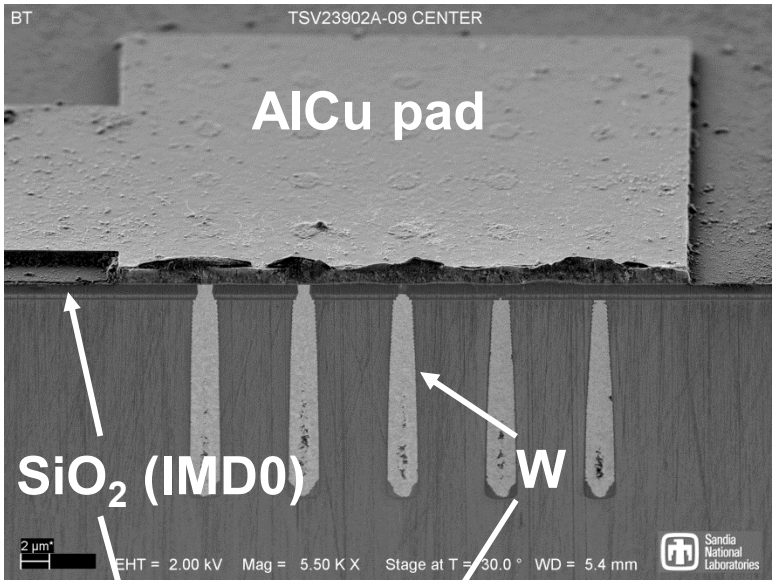


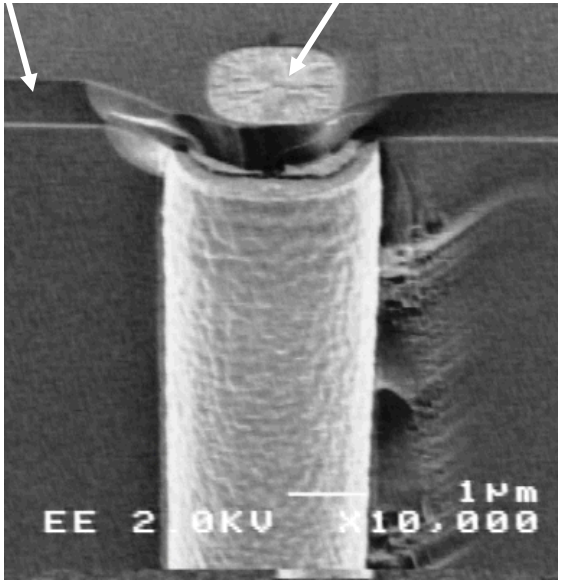
*Licensed From Ziptronix/Invensas.

FEOL TSV Integration

- Fully FEOL-compatible TSV process with W interconnect material and dielectric isolation by thermal oxide.
- W integration in FEOL TSVs is facilitated by using Si as a sacrificial material to fill the via hole while FEOL processing is completed.
- Small diameter vias (2 μm) on small pitch (20 μm) provide high spatial density (250,000/cm^2) vertical interconnects for 3D integration.
- High density, high aspect ratio TSVs enable integration of complex 3D structures.

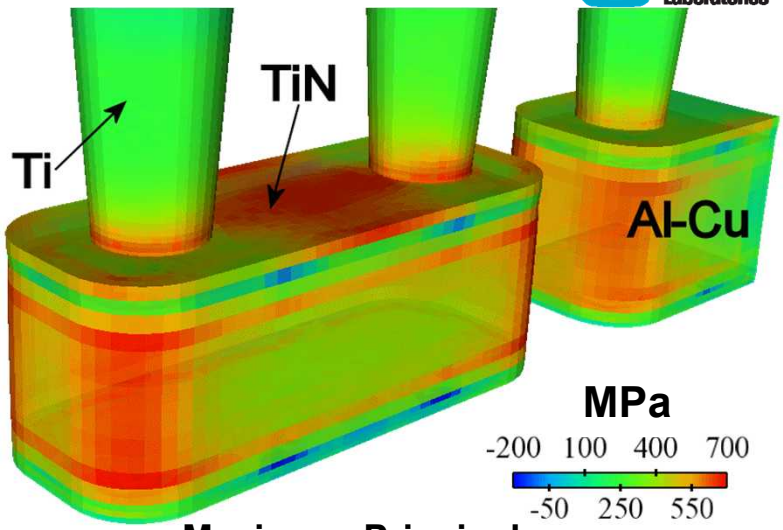




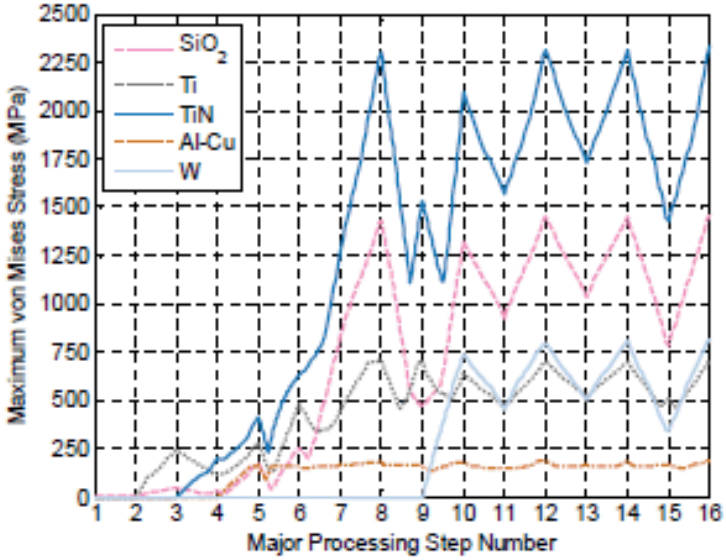


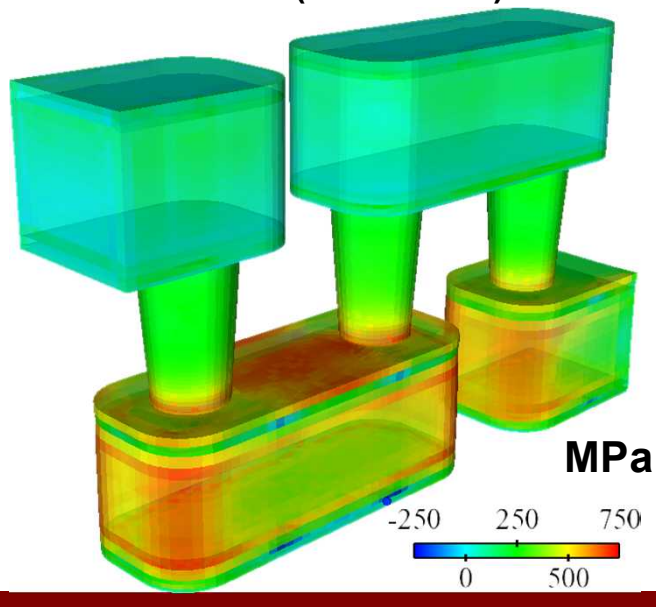
THERMOMECHANICAL MODELING OF 3DI STRUCTURES

- Design complexity of 3D ICs introduces reliability concerns for structural interactions
  - Multi-level thermomechanical interactions;
  - Interconnects through materials with varying CTEs.
- Need understanding of internal stress and deformation (difficult to assess experimentally).
- *Use 3D FEM framework to examine thermomechanical response of 3D interconnects.*



Maximum Principal Stress Distribution (Final State)



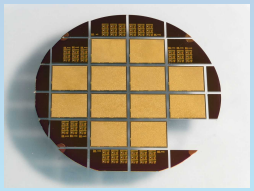
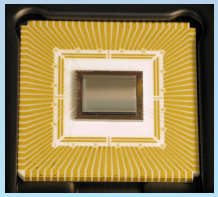
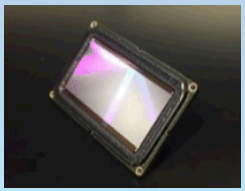
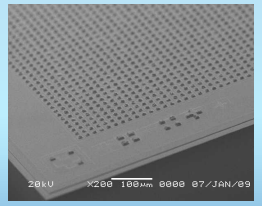


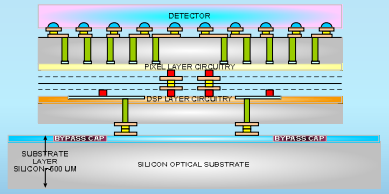
Current/Recent Heterogeneous Integration SNL Program Work & Research

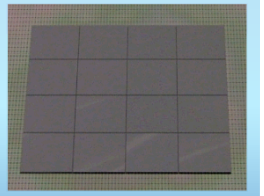
Heterogeneous Integration for National Security

Sandia National Laboratories

Visible/IR Imagers ROIC & Detectors

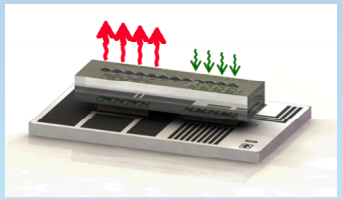
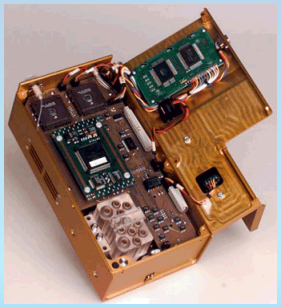
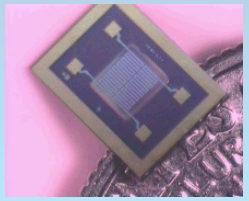
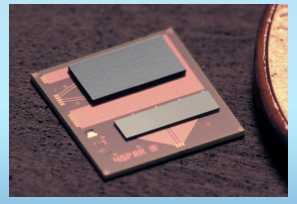
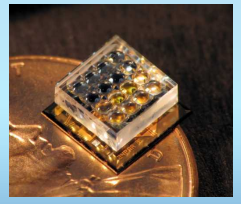









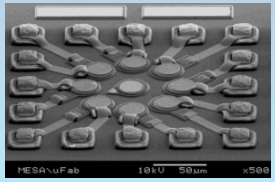
- large format FPAs
- indium and DBI hybridization
- GaSb MWIR/LWIR & Si Visible detector arrays

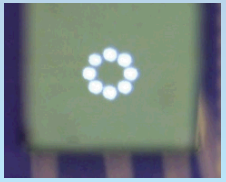
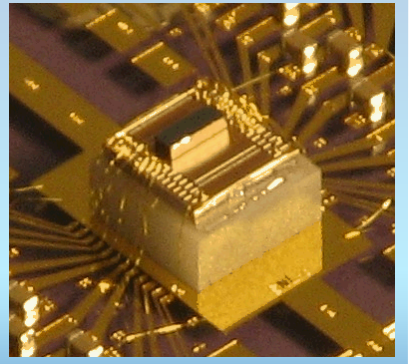
Optical and MEMS-based Microsensors

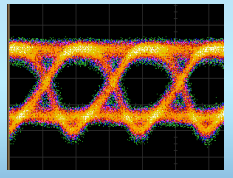






- chemical and bio sensors using MEMS and SAW devices
- g-hard optical microsensors with in-house photonics
- hybrid device integration with custom micro-optics

Optical Data Communications

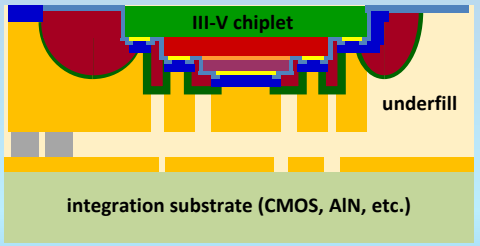


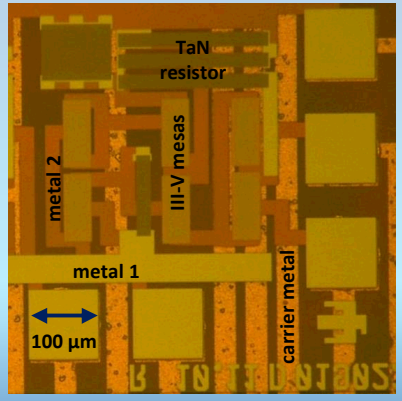





- GaAs- and InP-based VCSELs, modulators, photodiodes
- dense integration onto 32-nm and 45-nm CMOS

Heterogeneous III-V/CMOS Microelectronics



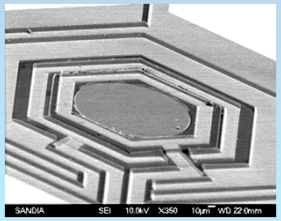


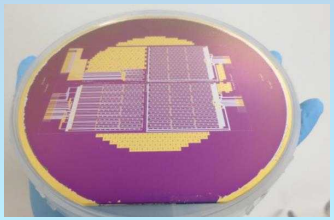
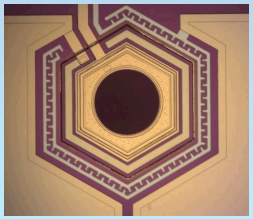
- complementary integration of GaAs and InP microelectronics
- III-V microelectronics circuitry on CMOS ASICs

Heterogeneous Integration for National Security

Sandia National Laboratories

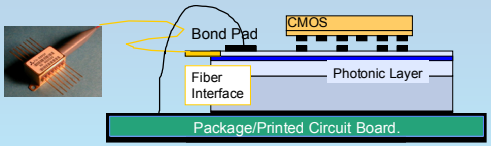
Microsystem-Enabled Photovoltaics

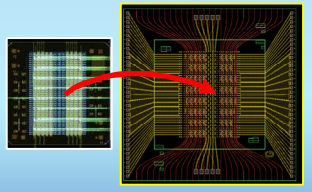
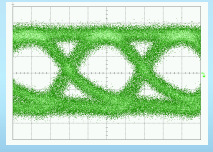
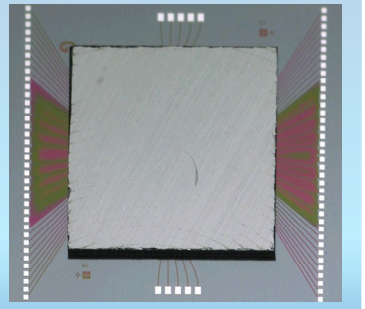


- wafer-level bonding for multi-junction solar cells
- InGaAsP/InP and InGaP/GaAs devices on silicon
- dielectric interfaces with III-V substrate removal
- integration with collection optics

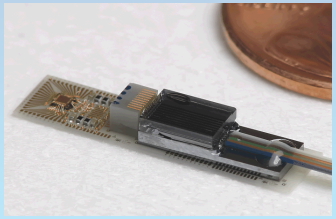
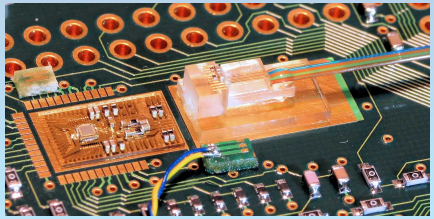
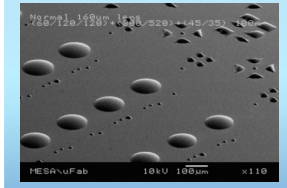
High Performance Computing

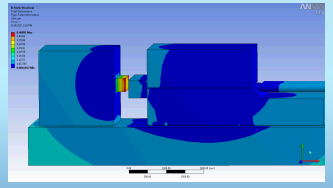
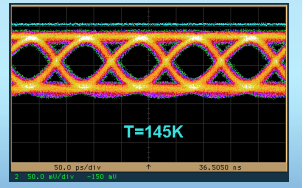


- silicon photonics on high-speed silicon ASIC
- independent optimization of electronics & photonics

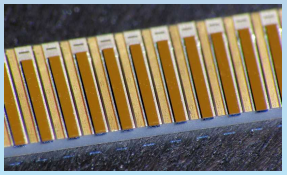
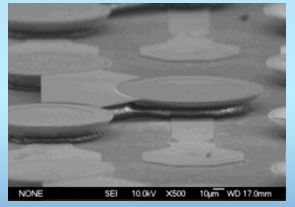
Extreme Environment Applications

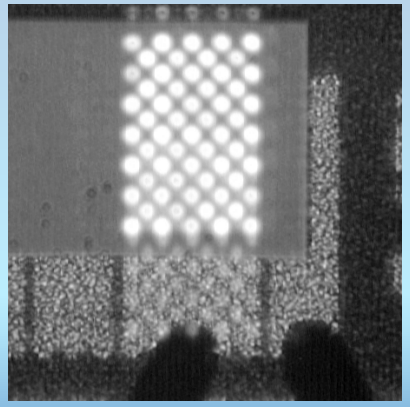




- custom photonics, optics, electronics for cryogenic interconnects
- advanced optoelectronics and integration for radiation hardness

High Performance Photonics

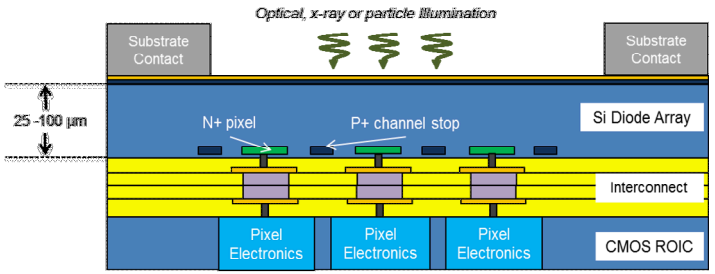



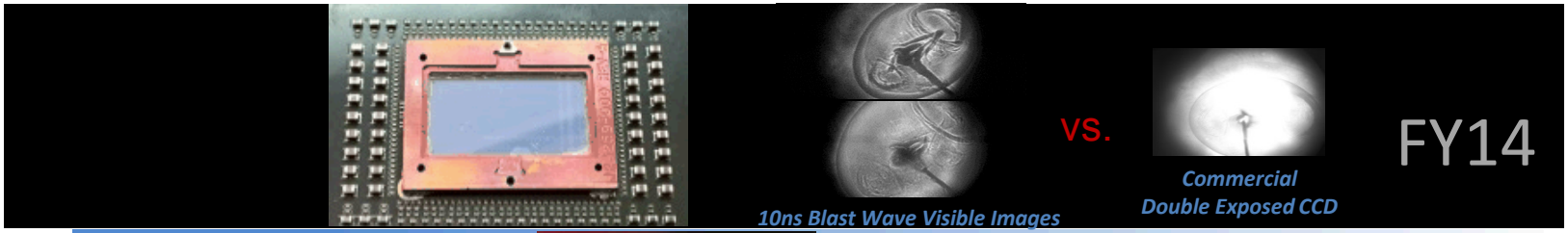


- high-power emitters on AlN and diamond
- RF packaging for high-speed test and measurement

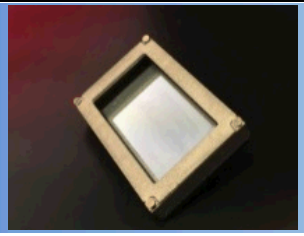
Ultrafast X-ray Imager Focal Plane Arrays

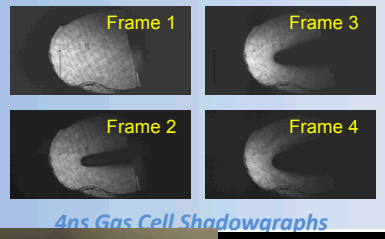
- The National Diagnostics Plan (NDP) named the UXI imagers as the #1 most transformational technology in HED industry.
- UXI camera systems offer transformational imaging capability for HED experiments at National Laboratories and facilities
  - SNL's Z-Machine to explore laser energy deposition in MAGLIF ga cells
  - LLNL's National Ignition Facility
  - LANL's OMEGA Facility





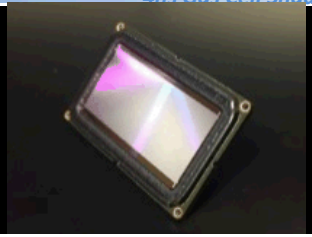
HIPPOGRIFF (FURI II)
1.5ns, 2-8 Frames (Interlacing)
448x1024 pixels
350nm Sandia Process





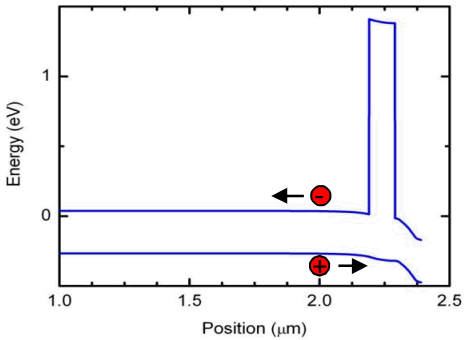
4ns Gas Cell Shadowgraphs

FY15



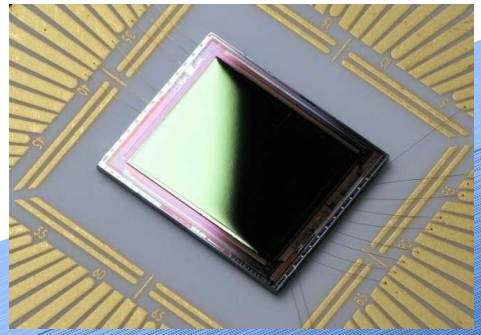
FY16-17

MWIR/LWIR nBn Focal Plane Arrays

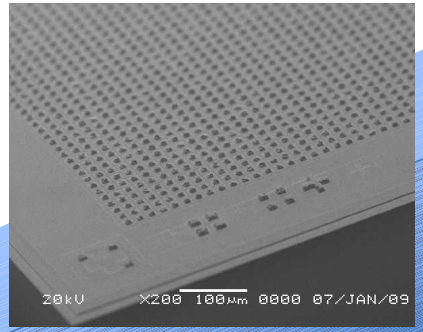


nBn band diagram

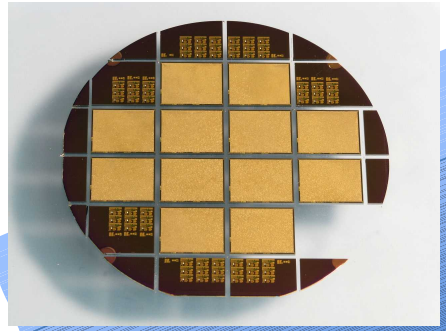
MWIR still frame, 160K



hybridized nBn FPA prototype



nBn array with indium bumps

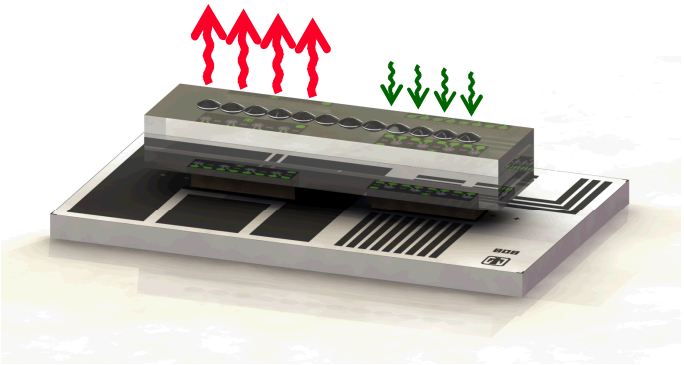


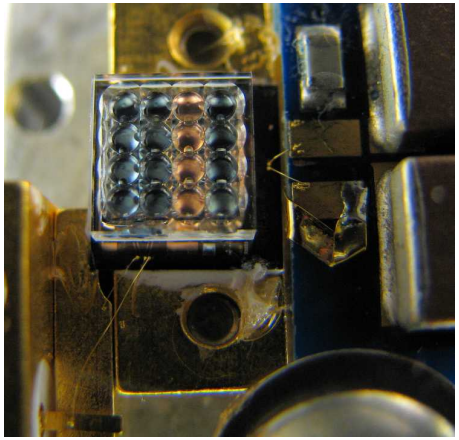
GaSb detector epitaxy

- **nBn rapidly approaching MCT sensor performance**
- **In-house development of nBn detector technology includes growth, fabrication, integration, and device/system testing**
- **Requires hybridization of large (≤1MP) GaSb detectors to CMOS ROICs**

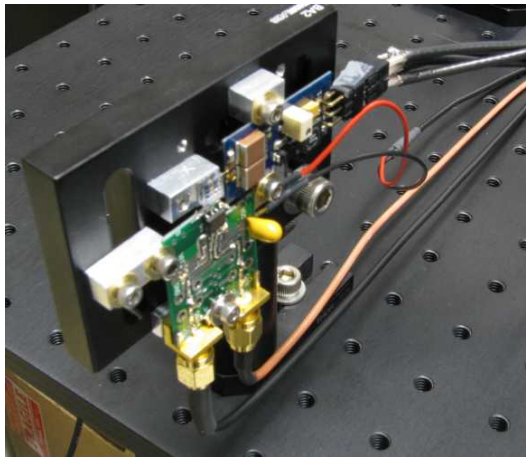
Microscale Optical Sensors

- Robust photonic proximity fuzes employ flip-chip optoelectronics and micro-optics
  - very compact, g-hard; high sensitivity; narrow FOV; immunity to RF jamming
  - requires high-power VCSELs; fast photodiodes at 980nm; micro-optics
  - flip-chip integration of optoelectronics on AlN or diamond heat spreaders

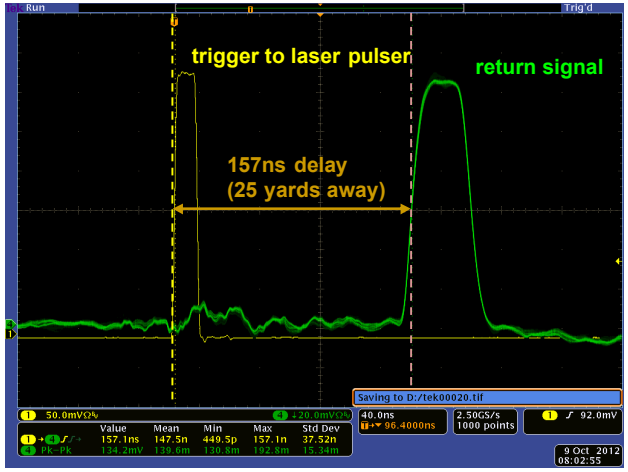




time-of-flight optical range sensor



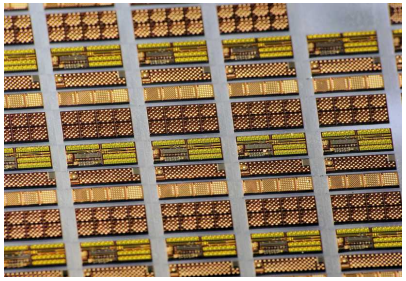
microfuze with support electronics



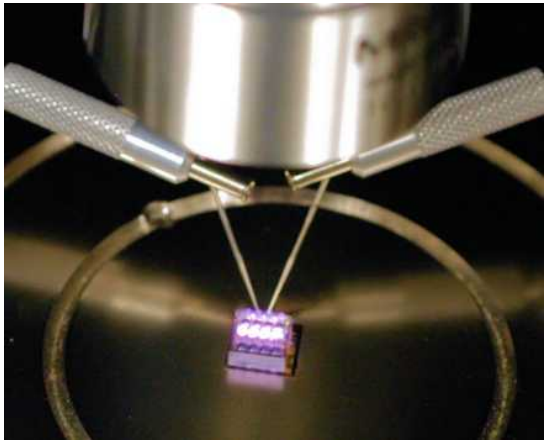
photonic fuzing demo with micro-optics and VCSEL transmitter array

Optical Microsystem Integration

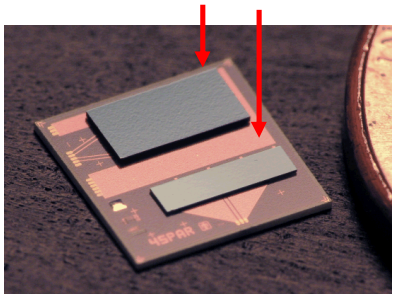
- Processes combined into photonics fabrication
  - solder dam, underbump metallization, solder bump
  - thinning and AR coatings
  - singulation (scribe and break)
  - flip-chip attach
- Micro-optics fab & align
  - diamond turning
  - molding in optical plastics
  - active alignment
  - UV epoxy attach



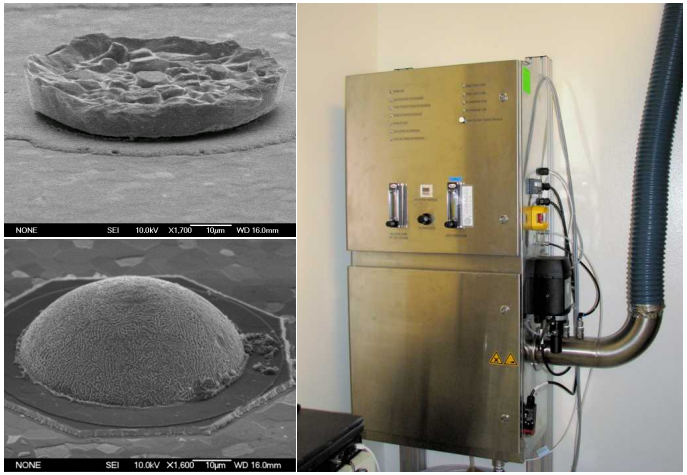
photodiode and VCSEL arrays



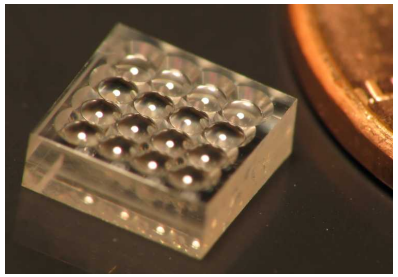
integrated component testing



populated fuse submount



indium solder reflow for thermal transfer



microlens array

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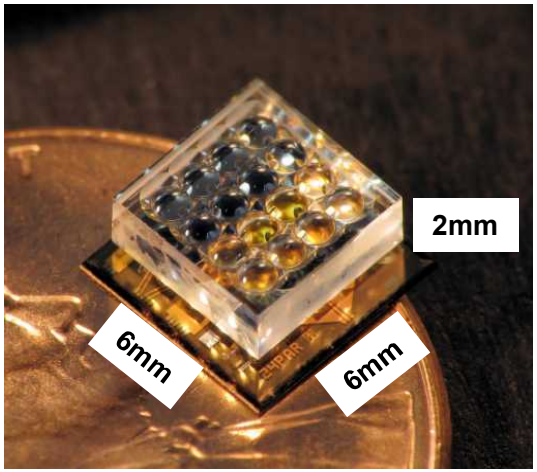
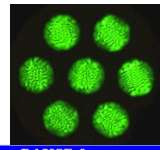
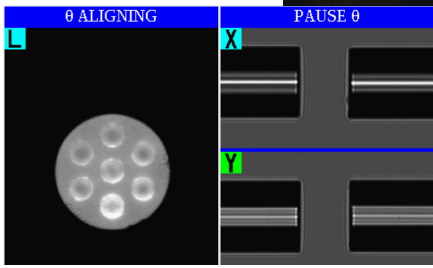


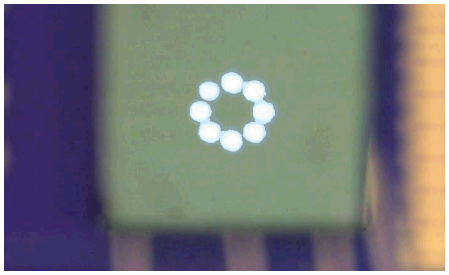
high-power optical proximity sensor

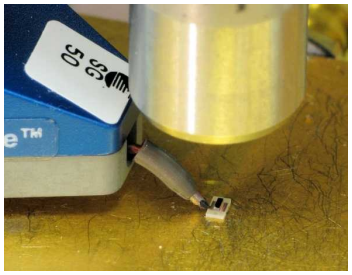
Interconnect Components

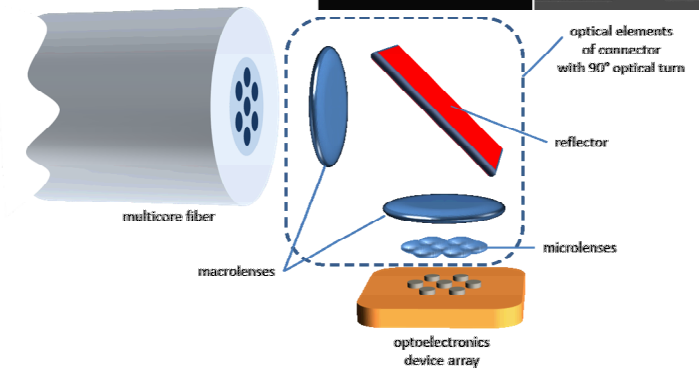
- Development of high-density optoelectronics arrays
  - low-power VCSELs designed for high BW at low drive current
  - photodiodes >40Gb/s with very low capacitance through flip-chip integration
- Micro-optics designed for coupling to multicore fibers
  - custom micro-optics developed for multicore fiber links

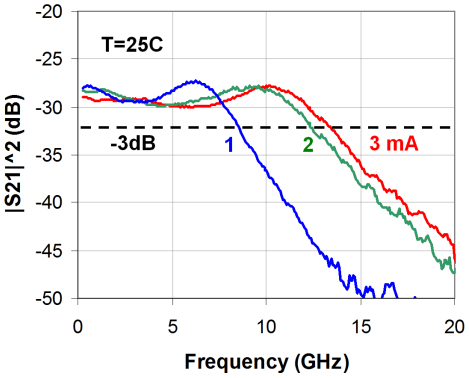




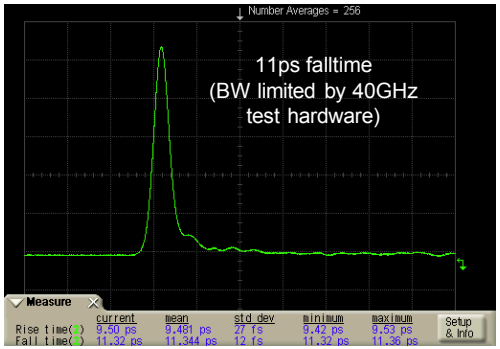




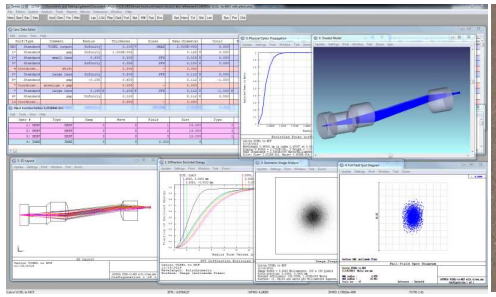


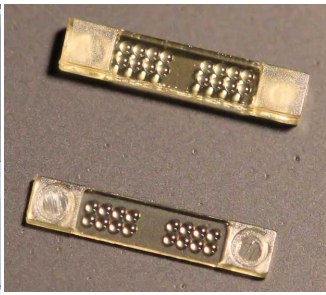


VCSEL performance



InGaAs photodiode performance

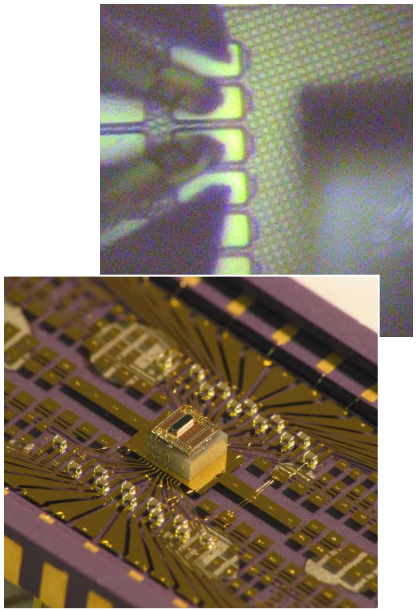




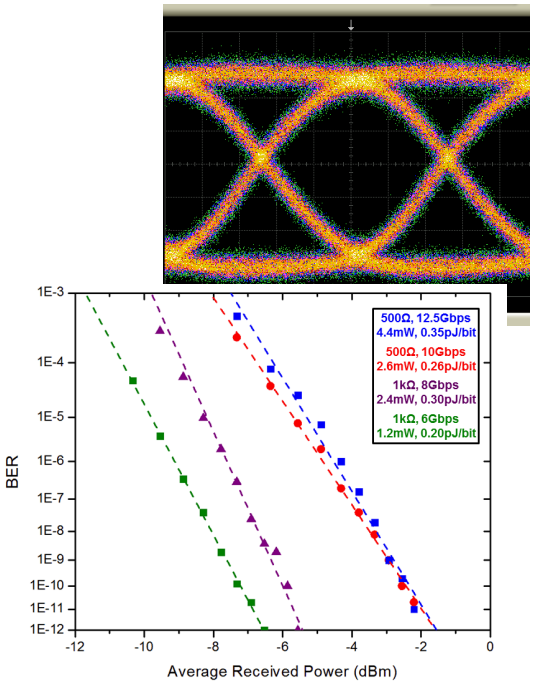
micro-optics and multicore fibers

Interconnect Testing

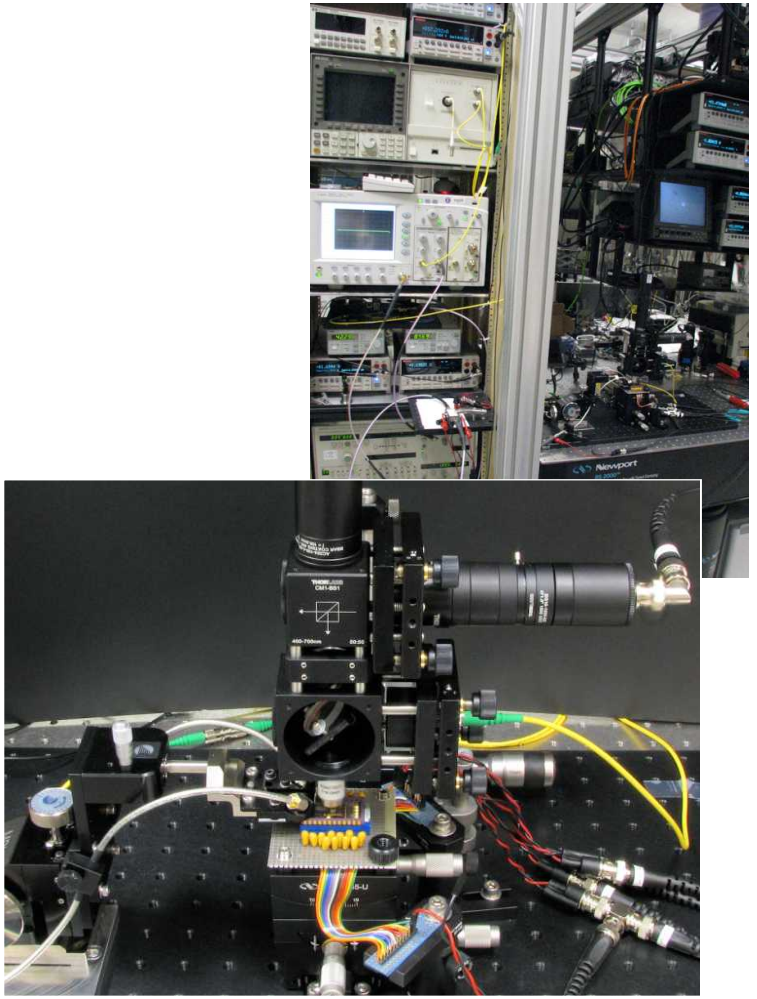
- Hybridized parts packaged for high-speed opto-electronic testing
  - DC wirebonding, RF probing
  - active fiber alignment
- Single channel links demonstrated using 45-nm CMOS
  - 10Gbps at 1.7 pJ/bit
- Ongoing characterization of new link and components
  - test & attach multicore fiber, micro-optics, and 32-nm IC



packaged CMOS/III-V photonics



system link testing

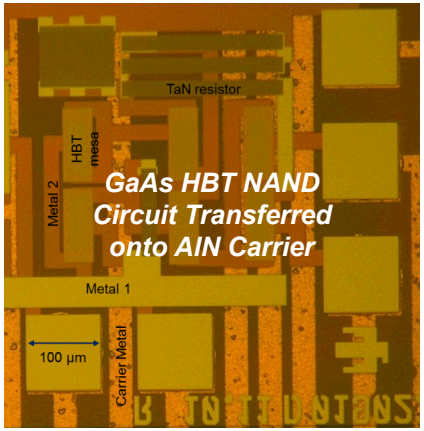


lab-to-lab link demonstration

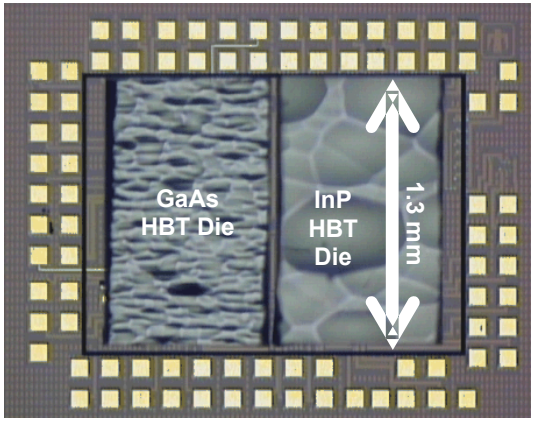
Heterojunction Bipolar Transistors Integration with CMOS

- Future Silicon – III/V Heterogeneous Integration needs
  - III/V Materials can implement functions that silicon cannot
    - The heterogeneous integration of the two material types provides new capabilities to the system designer

- Examples of HBT Functions
  - FET Driver
  - Regulator
  - Booster
  - Voltage Reference
  - Comparator
  - Precision Voltage Reference
  - Discrete Npn Transistor
  - Discrete PnP Transistor

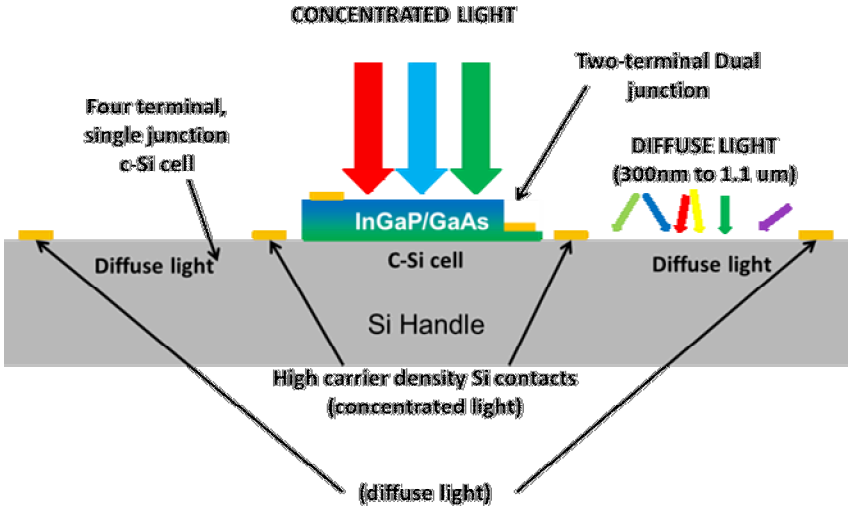


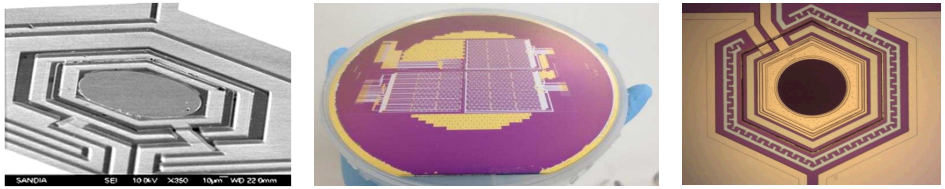
GaAs and InP HBT Circuits Transferred onto CMOS



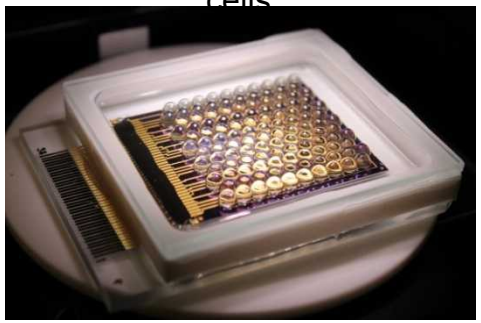
Microsystem-Enabled Photovoltaics (MEPV)

- Wafer-level bonding for microscale multi-junction solar cells
  - InGaAsP/InP and InGaP/GaAs devices on silicon
- Dielectric interfaces with III-V substrate removal
  - Re-use of substrates to reduce ultimate cost
- Photonic microsystem prototyping
  - Integration with collection optics





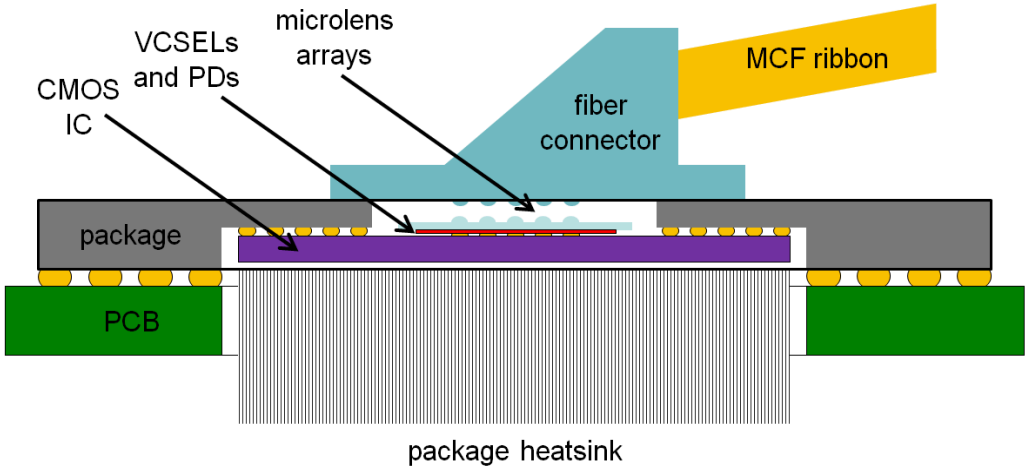
Wafer-level integration of III-V and silicon cells



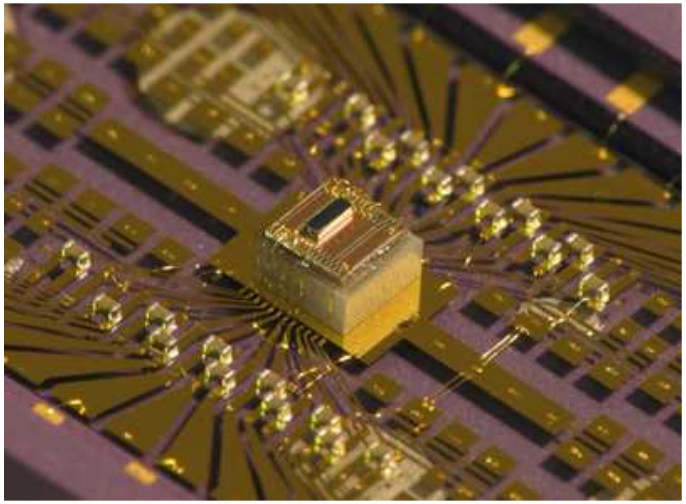
MEPV packaged module

Optical Interconnects for High Performance Computing

- Dense integration of photonics and CMOS for advanced interconnect technologies
  - hybrid integration for very high density and low electrical parasitics
  - targets <1 pJ/bit and >1 Tbps/mm^2
- Development of circuits, photonics, optics and integration techniques
  - transmit/receive circuits in 32-nm and 45-nm CMOS (TAPO)
  - combines VCSEL and photodiode arrays, micro-optics, custom fiber

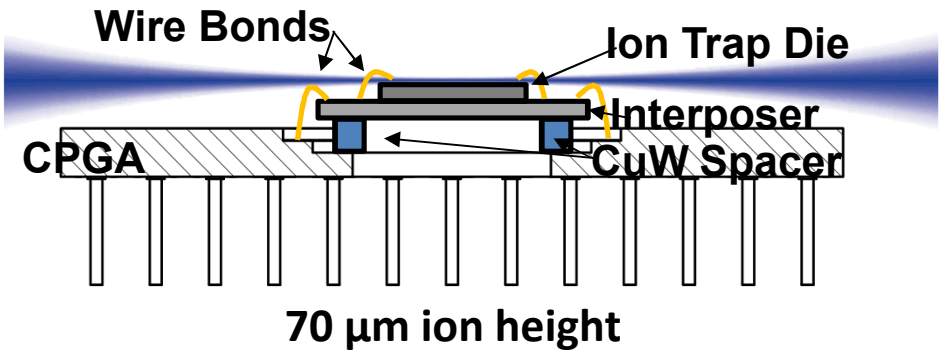


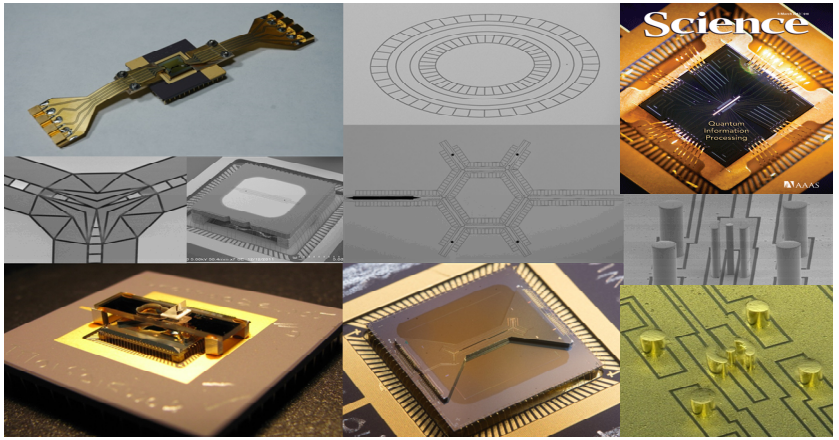
multichannel interconnect concept



packaged CMOS/VCSEL assembly

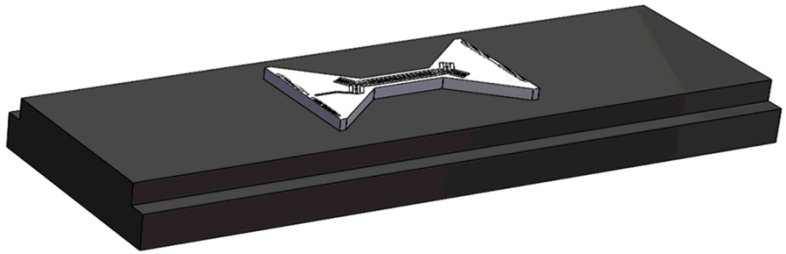
Cu/Tungsten TSV on SOI For Ion Traps

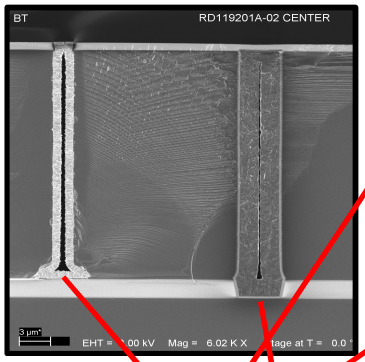




TSVs for Ion Traps

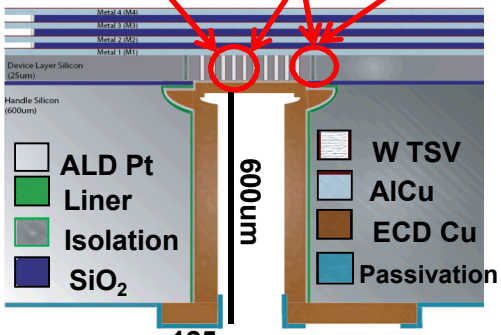
- Improve Optical Access
- Increase I/O per area
- Reduced electrical parasitics for RF and microwave signals
- Improved thermal sinking for cryogenic operation
- Simplify assembly

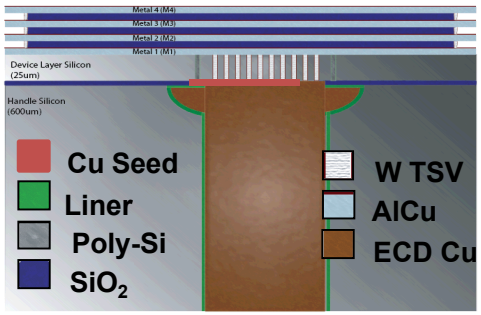




W vias to connect Cu TSV through BOX and top Si layer

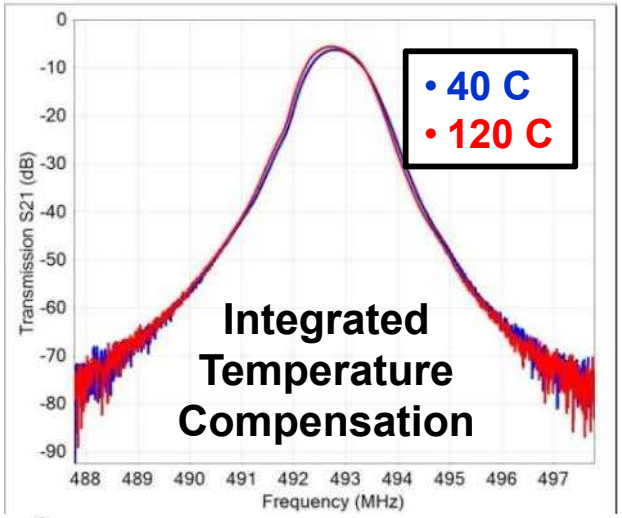
Isolation trench to electrically isolate the vias from the device Si layer

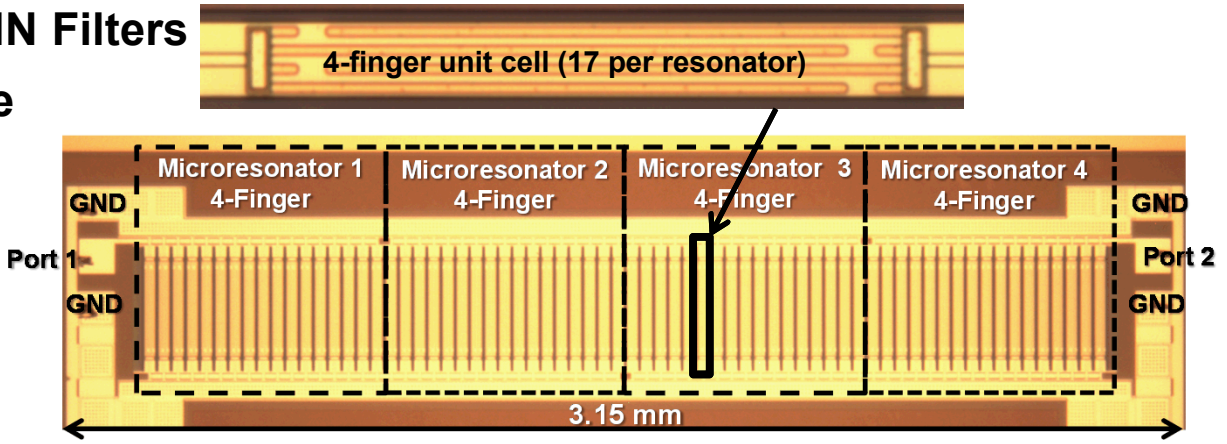


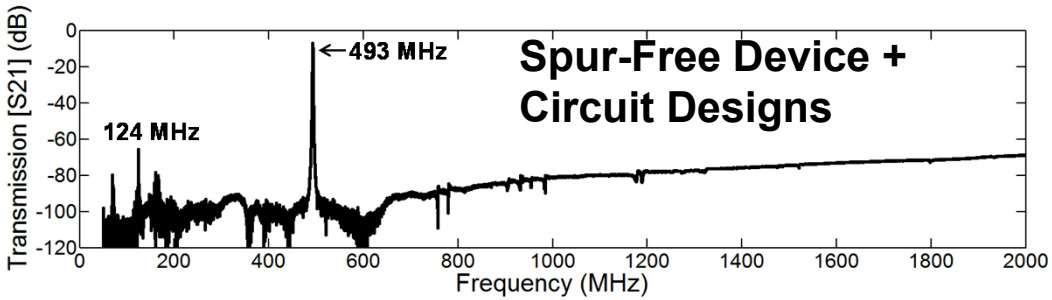


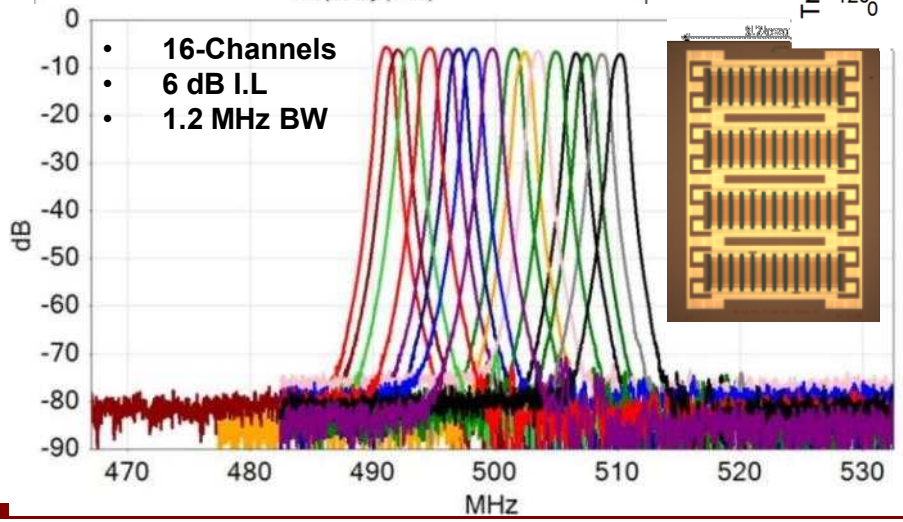
Integrated RF Filters

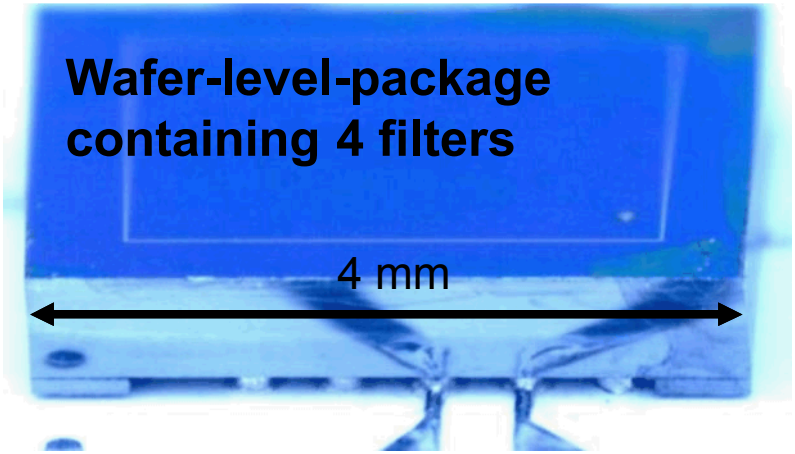
- Miniature High-Q On-Chip AlN Filters
- Multiple Frequencies Per Die
- <1 MHz to >10 GHz





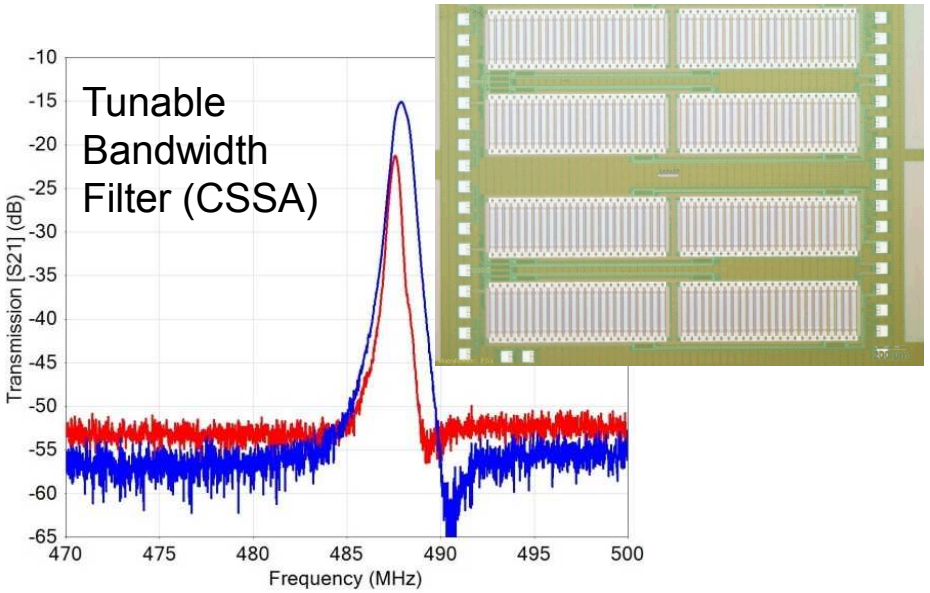


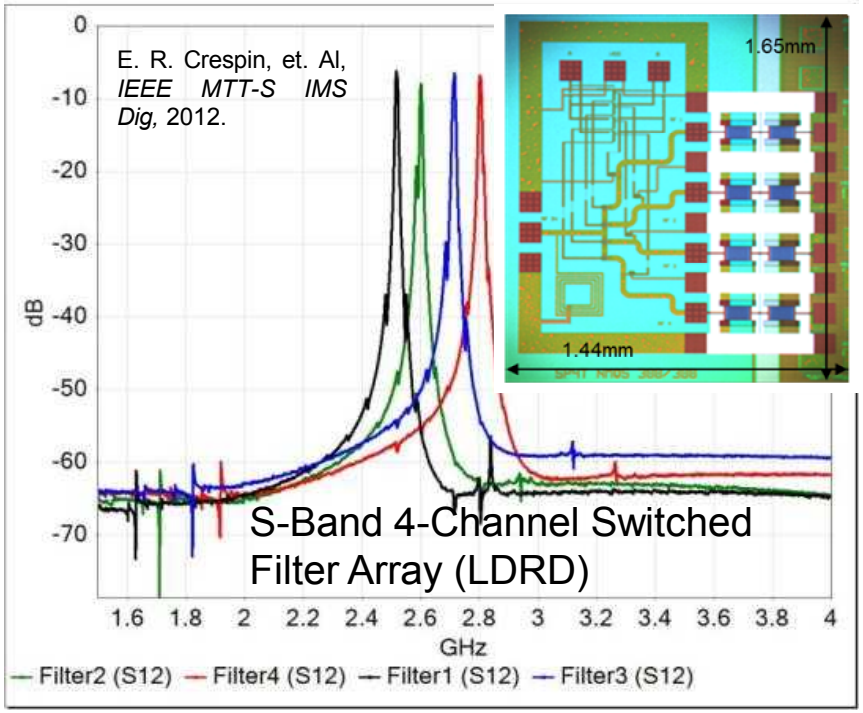




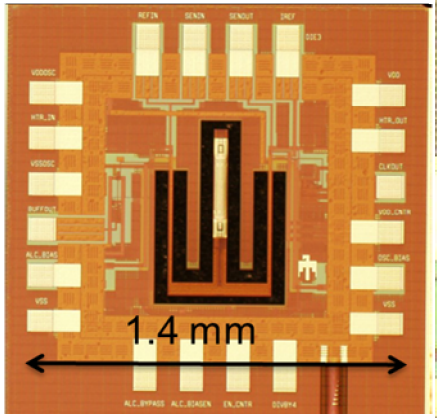
RF Integration: Resonators + CMOS

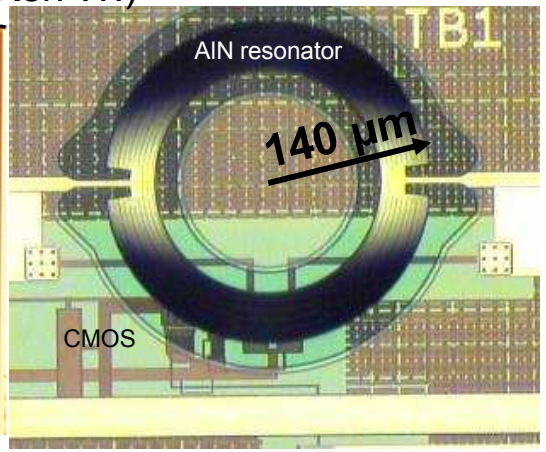
- A Unique Sandia capability
- Integration Reduces Size, Power, and Interconnect: Improved Performance, But….
  - Monolithic Integration Means That Process Times Add (to > 12 months)
  - Restricted to CMOS (low-ρ) Substrates
  - Limited to Internal CMOS7 Technology





Integrated Oscillators (Ken W.)

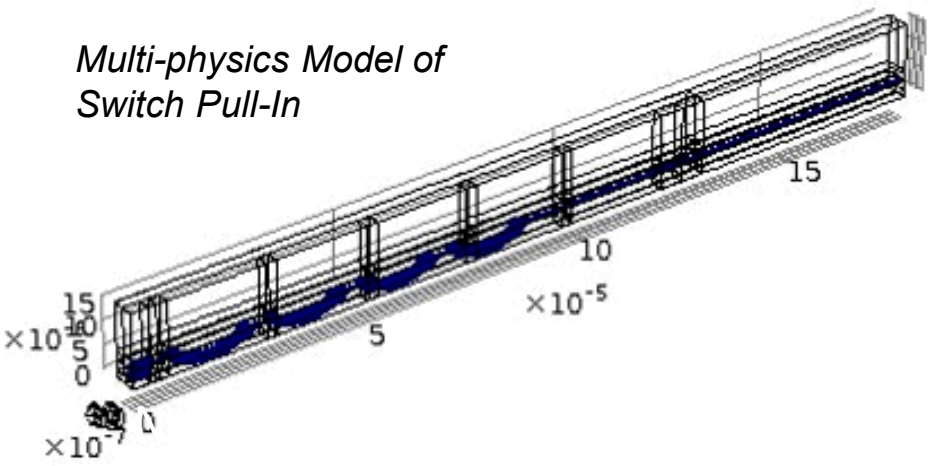


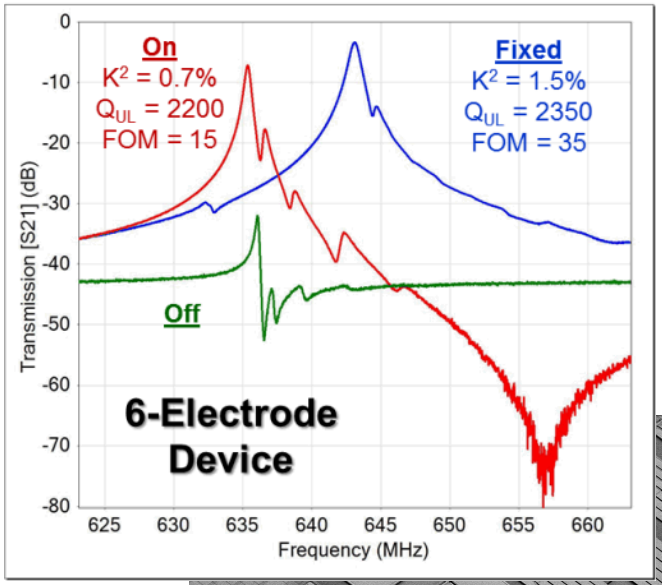


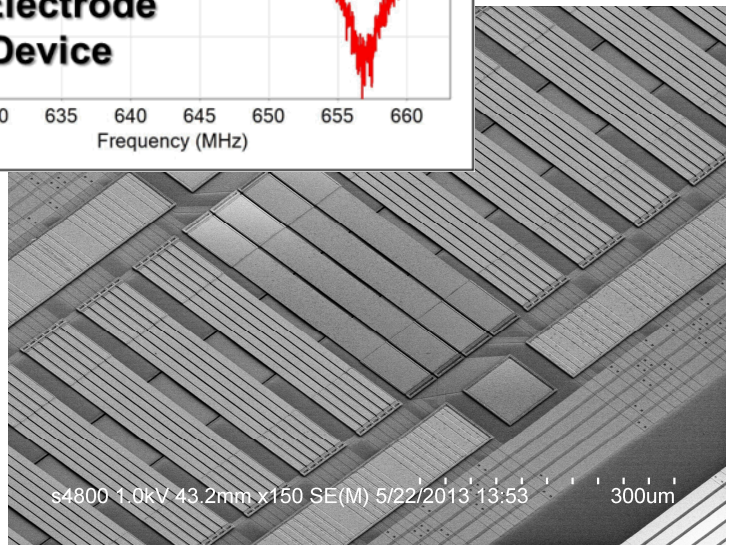
RF Integration: Resonators + Switches

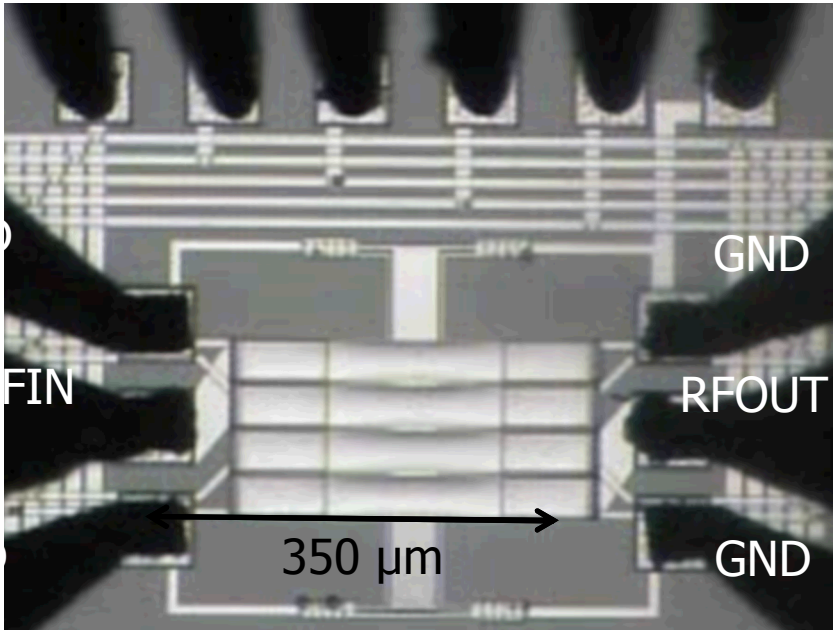
- Integrate MEMS Switches Into Resonator
- Improved Switched + Tunable Filters
- First On/Off Switched AlN Resonators

Multi-physics Model of Switch Pull-In









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