

Challenges in LTCC

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39th International Microelectronics and Packaging

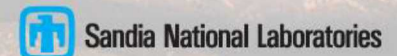
IMAPS Poland 2015 Conference

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Two Aspects of Challenge

- Opportunities in LTCC
 - Novel applications.
 - “Out of the box.”
- Limitations in LTCC
 - Within the realm of capability.
 - Emphasis: performance, cost, schedule, reliability.



Outline

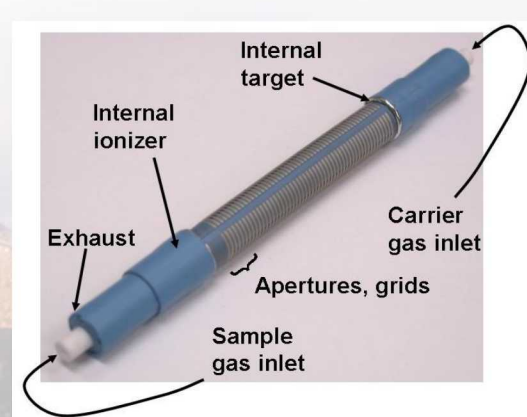
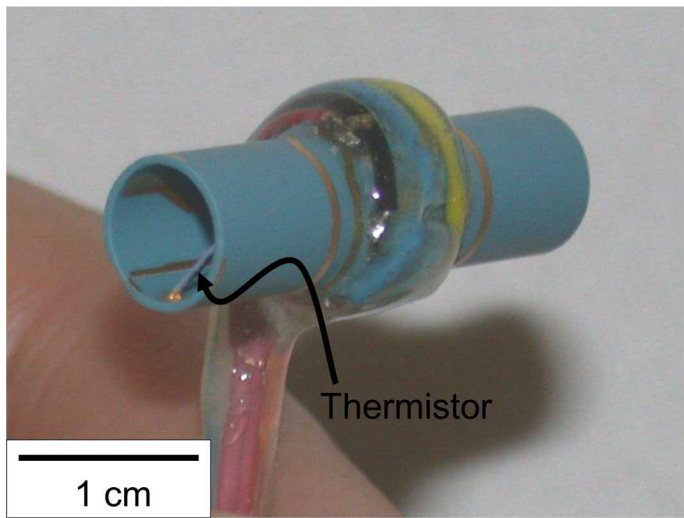
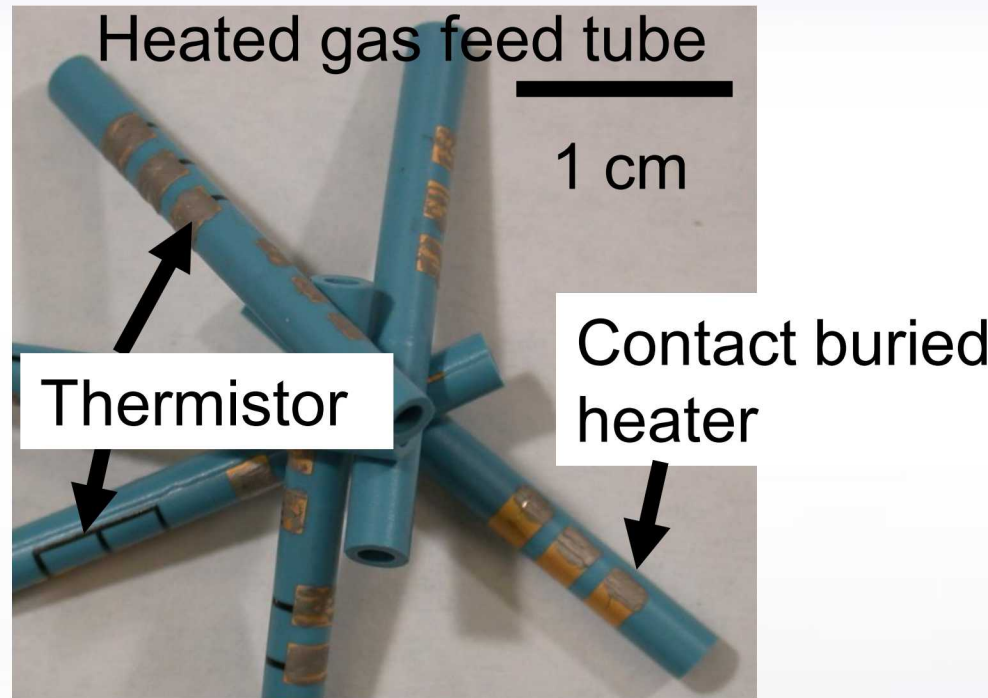
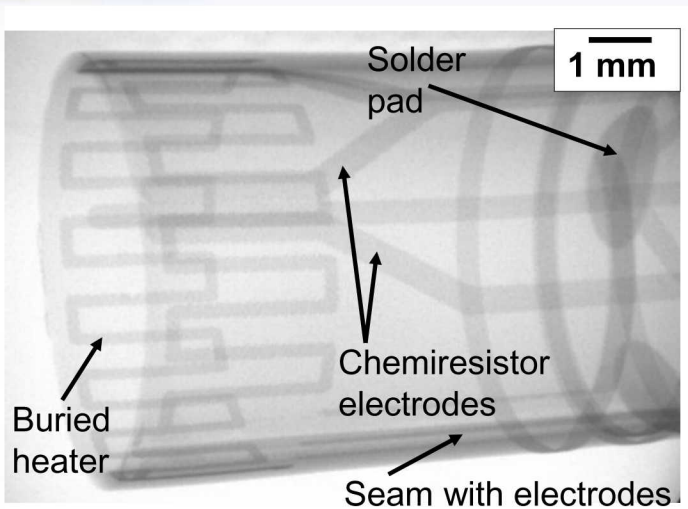
- Review novel processing
 - Shapes
 - Sacrificial materials
 - MEMS applications
- Review MCM structures & processing
 - Why thin film?
 - Shrinkage tolerance
 - Structuring
- Summary



Novel Applications- the Path Includes:

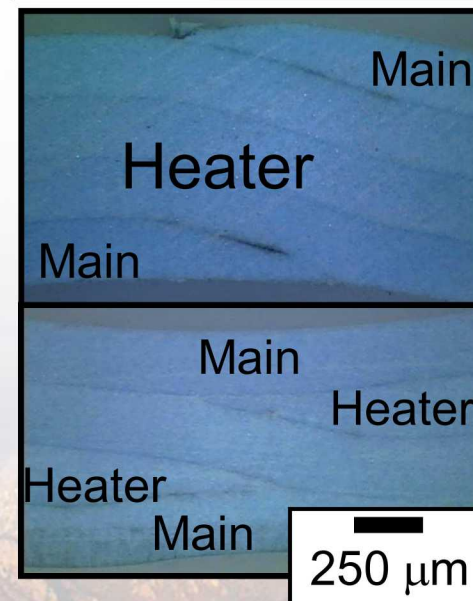
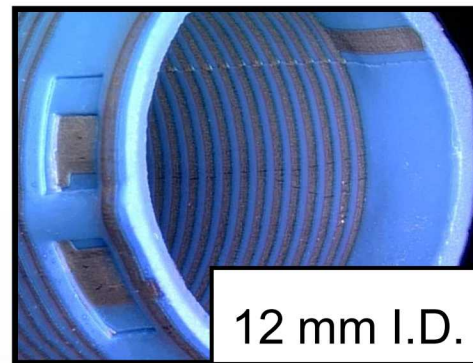
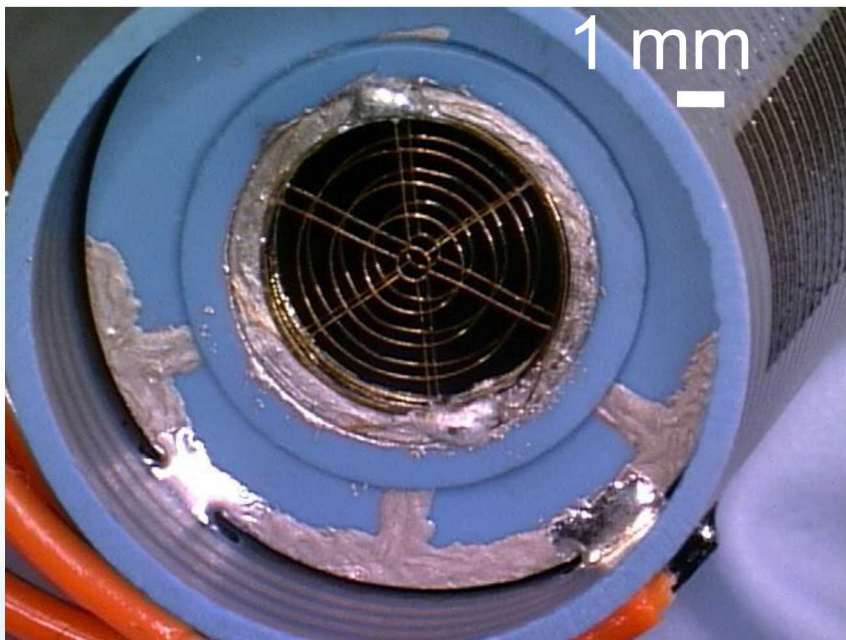
- Shaping (bending, rolling, molding, applique)
- Sacrificial volume materials (SVM)
- Multi-purpose--fluidic, electrical, mechanical, chemical,...
- Sensors, actuators,...

Tubular Devices

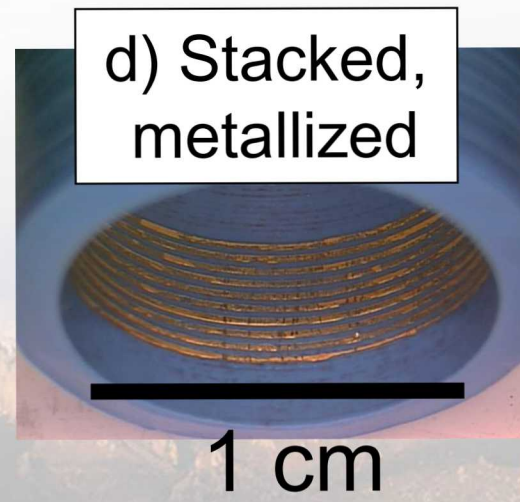
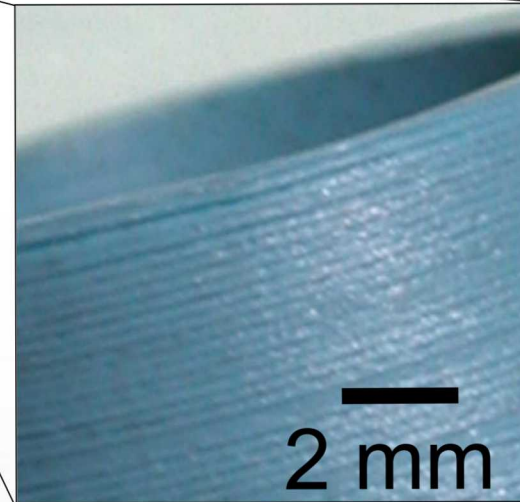


Forming of LTCC to Unconventional Requirements

Rolled ion mobility spectrometer (IMS) drift tube

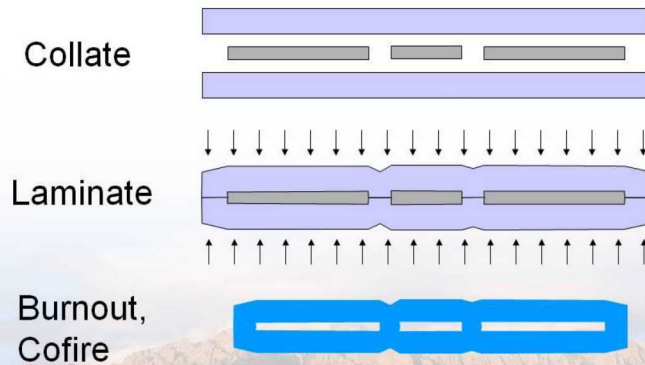


Stacking to 300 layers



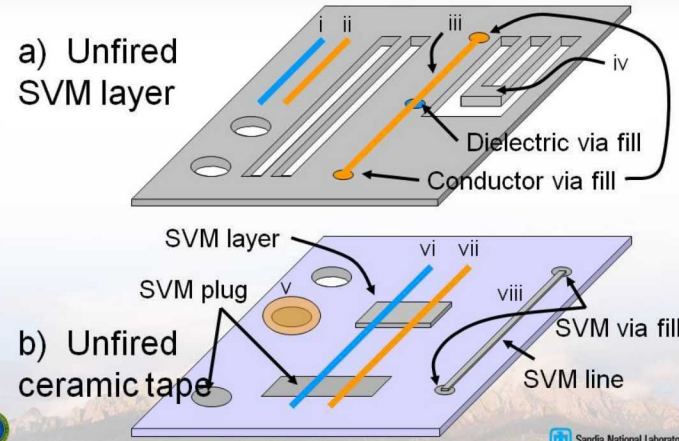
Novel Structures 1: SVM

SVM Technique



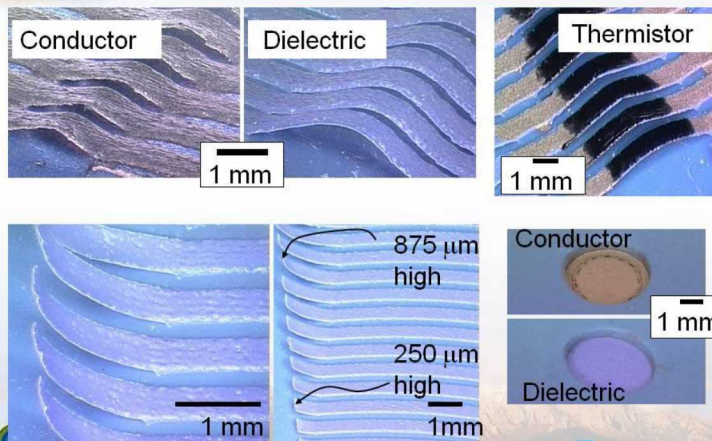
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SVM / LTCC Tape / Thick Film Combinations



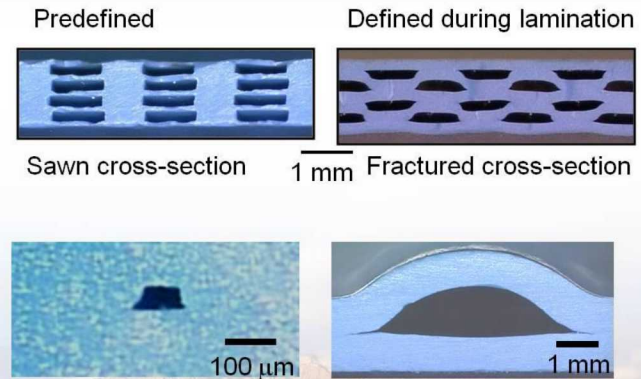
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Suspended Thick Film



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Meso/Micro-Scale Channels



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Novel Structures 2: Channels

Test Manifold

LTCC manifold
Nanoports
O-rings
Package
ZIF socket
Chip (back)
LTCC interposers
(l) back, (m) front, (r) metallized front

1 cm
1 mm

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Modular Microfluidic Standard Components

a) 1 cm
b) 1 cm
c) Microfluidic Ports 1 2 3 4 5 6 7 8 1234 5678 1234 5678 1 cm
d) 1 cm

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Biological Cell Sorter

LCC Socket
Fluidic ports
Completed part in socket
As-printed (unfired)
Cell sorter chip
Active area
Chip attach area

1 mm
4 mm

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View Ports

Embedded Windows, Channels

4 mm
250 μm
Channel Width
500 μm
1 mm

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“Flat Boards” - The path includes:

- High Frequency MCMs
 - Location of RF ground planes, features
- EMI-shielding
- Thermal issues
- Shrinkage tolerance vs. high-density circuitry
- Cavities, holes, valleys, ledges
- Surface topography
- Assembly—adhesives, solder, wirebond, braze, weld

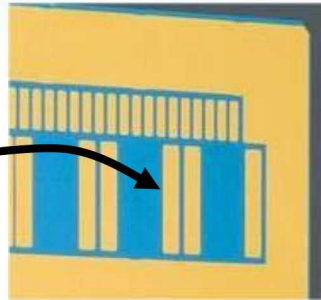


Marketplace

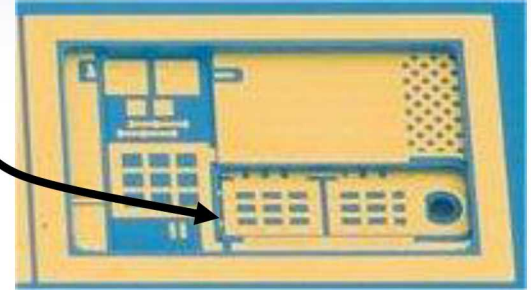
- Drive toward finer features, larger panels, lower cost.
- Maintain high quality, reliability.
- Competing technologies present risk of defection.

Planar MCM Features

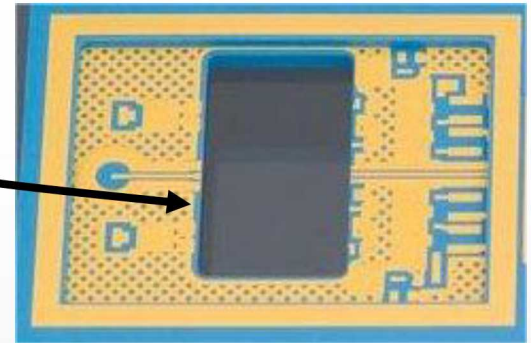
Discrete component pads



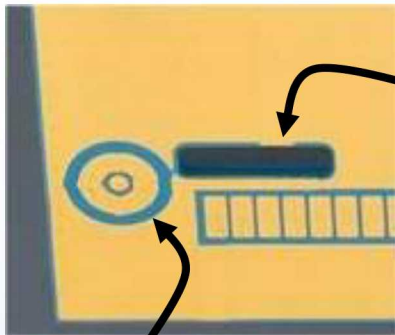
Multiple cavity levels



Cutouts for high-power devices



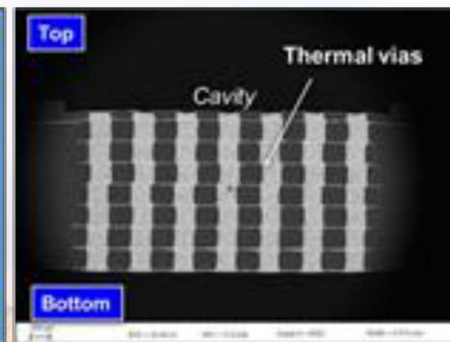
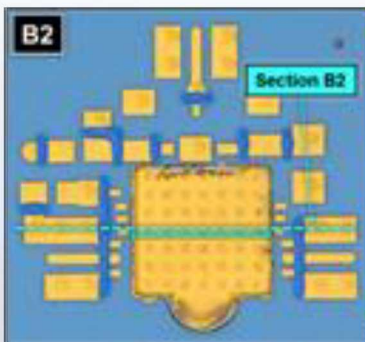
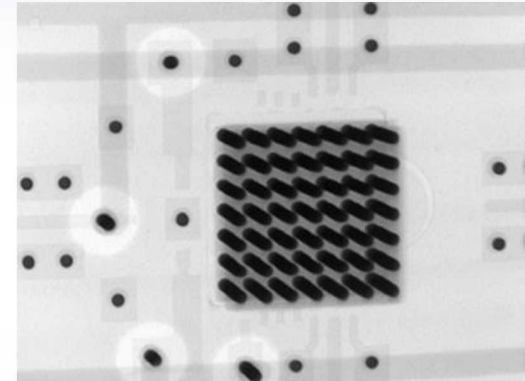
Connectors



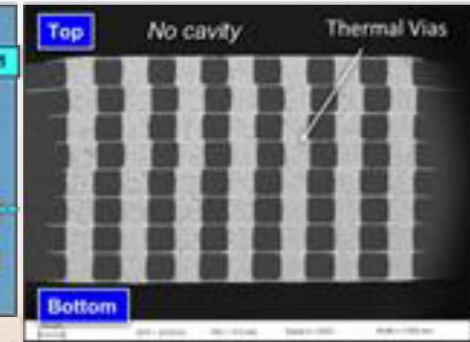
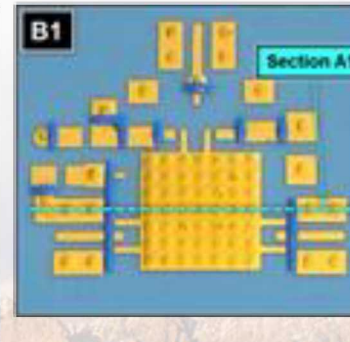
1 cm

LTCC Design for Thermal Management-- Thermal Via Design

- 10 mil TC501 Au vias are stacked through the entire LTCC structure
- 3x the via diameter spacing
- Die areas green machined to the layer 7 ground plane
- GaAs and GaN die epoxied to the heat spreader
- Heat spreader epoxied die attached into cavity
- No thin film in the cavity
- Cross sectioning of the thermal test vehicles completed. Du Pont TC 501 is path forward for thermal vias.
- The thermal vehicle which included 100% Ag and a mixed metal Au/Ag thermal via displayed material incompatibilities at the mixed metal/cover pad interface (bottom) due to unequal metal atom diffusion rates (Kirkendall voids), inter structure separation within the via, and internal layer cracks (layer one).

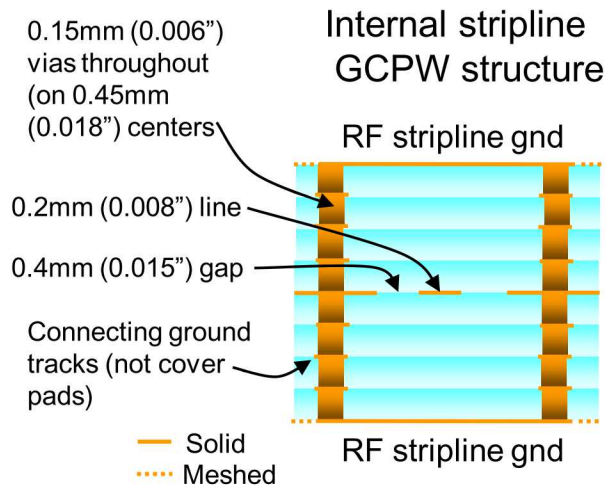


Baseline Design (Cavity)

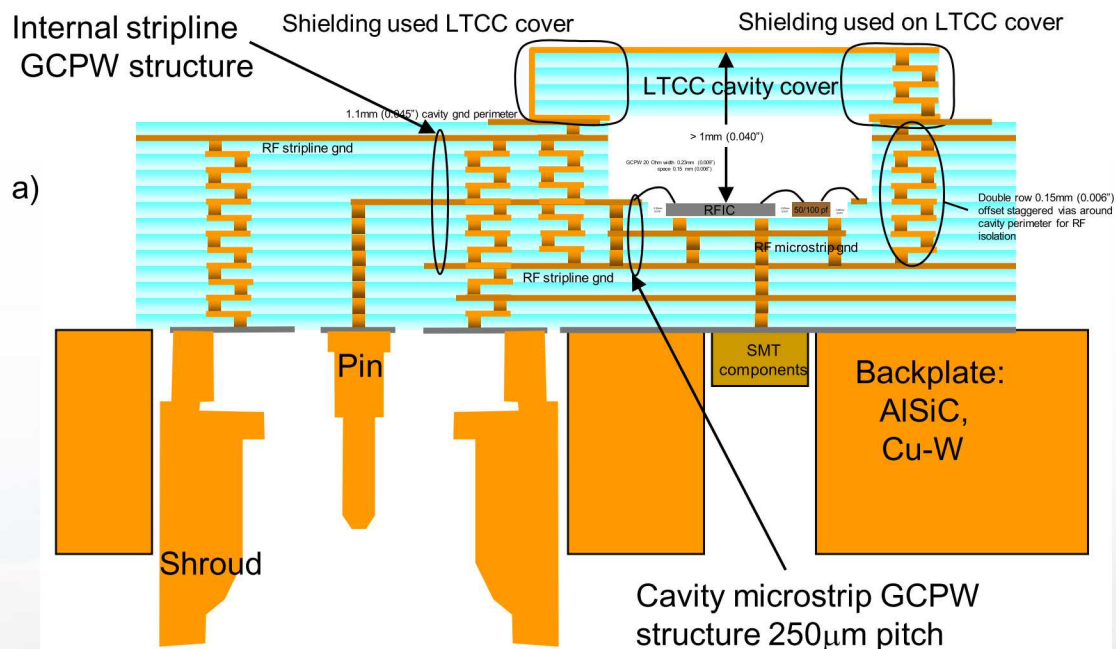
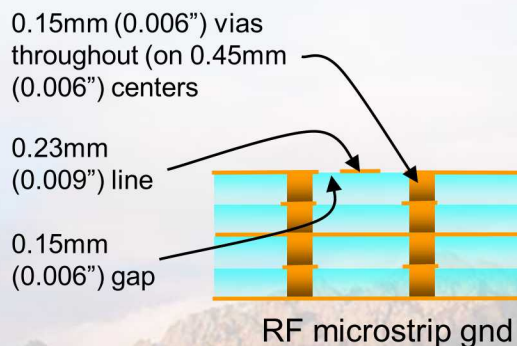


Improved Design (No Cavity)

MCM: Sectional View

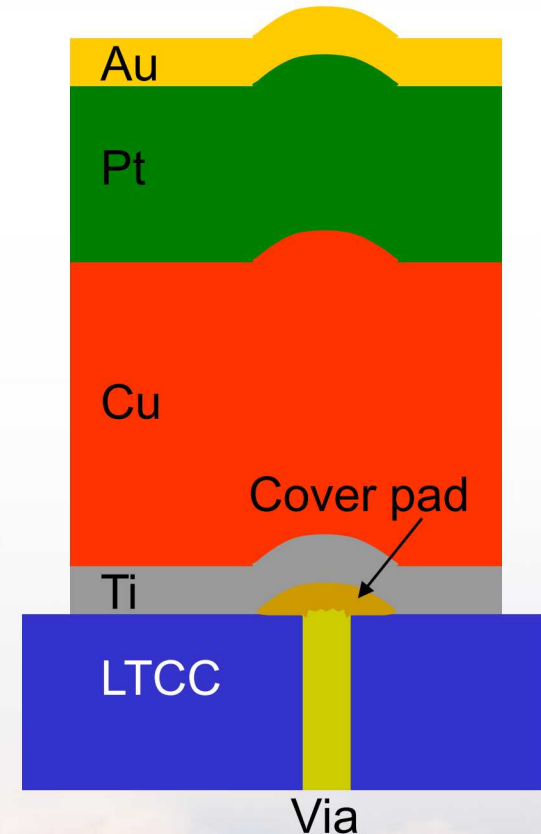


Cavity microstrip GCPW structure 250μm pitch



Thin Film Multilayer

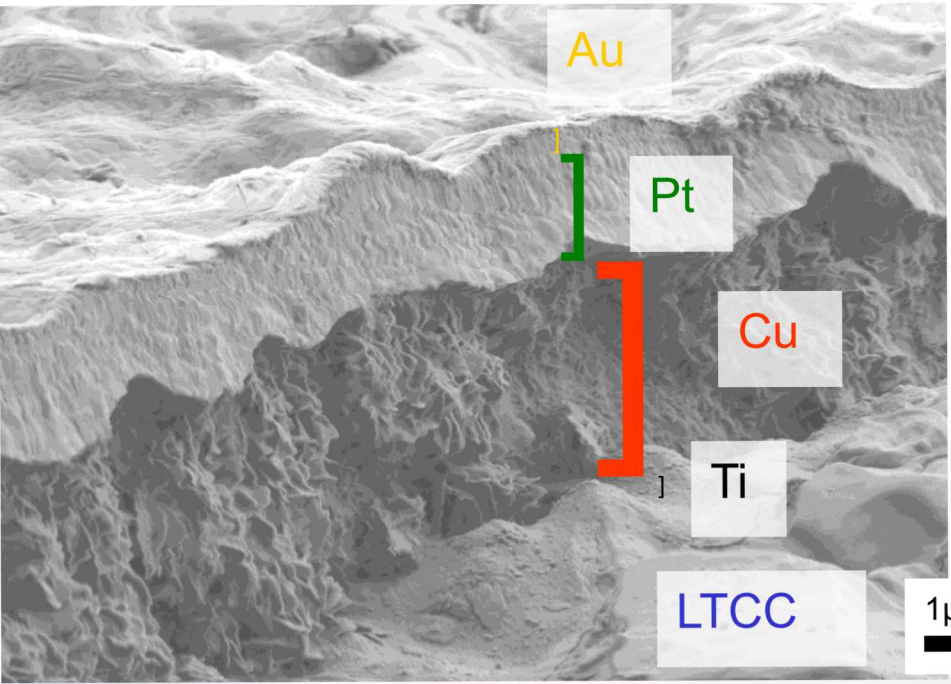
- Goal: single thin film material that satisfies all requirements:
 - Solder connectivity;
 - Wire bond connectivity;
 - RF conductivity;
 - Adhesion.
- Solution: Ti/Cu/Pt/Au multilayer (total $6.45\mu\text{m}$):
 - $0.2\mu\text{m}$ Ti \Rightarrow adhesion;
 - $4.0\mu\text{m}$ Cu \Rightarrow RF conductivity, pure metal;
greater than 2 times skin depth at
single digit GHz;
 - $2.0\mu\text{m}$ Pt \Rightarrow robust solder connectivity;
barrier for cross-diffusion of Cu
and Au or Sn;
 - $0.38\mu\text{m}$ Au \Rightarrow wire bond connectivity;
wetting for solder connectivity;
keeps layers inert over time;
 - Thick film cover pads over vias for topography
issues



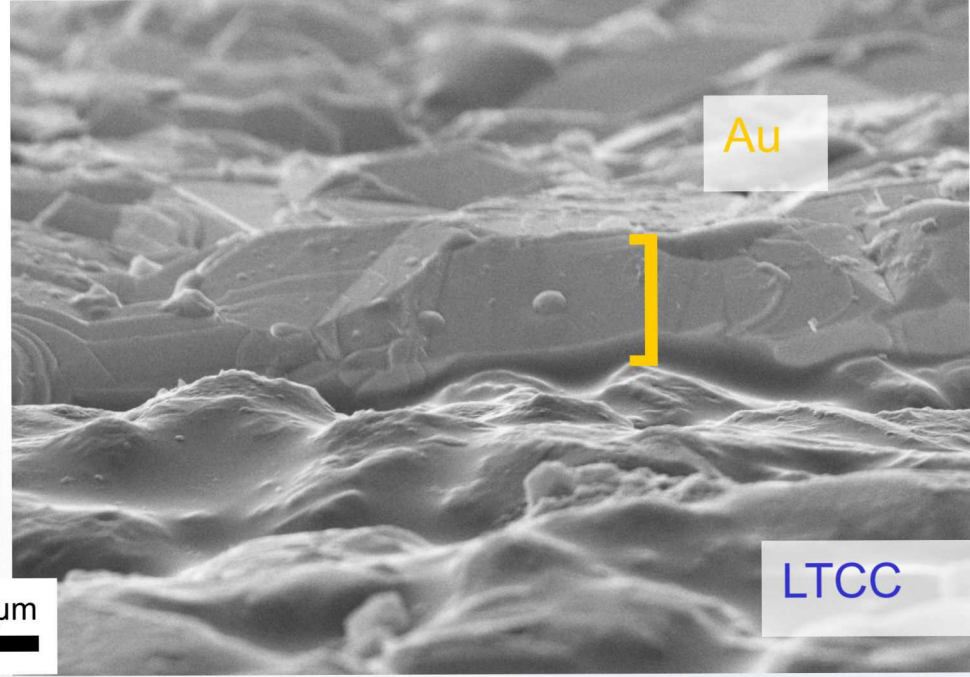
Thin Film Cross Section
(not to scale)



Thin Film vs. Thick Film



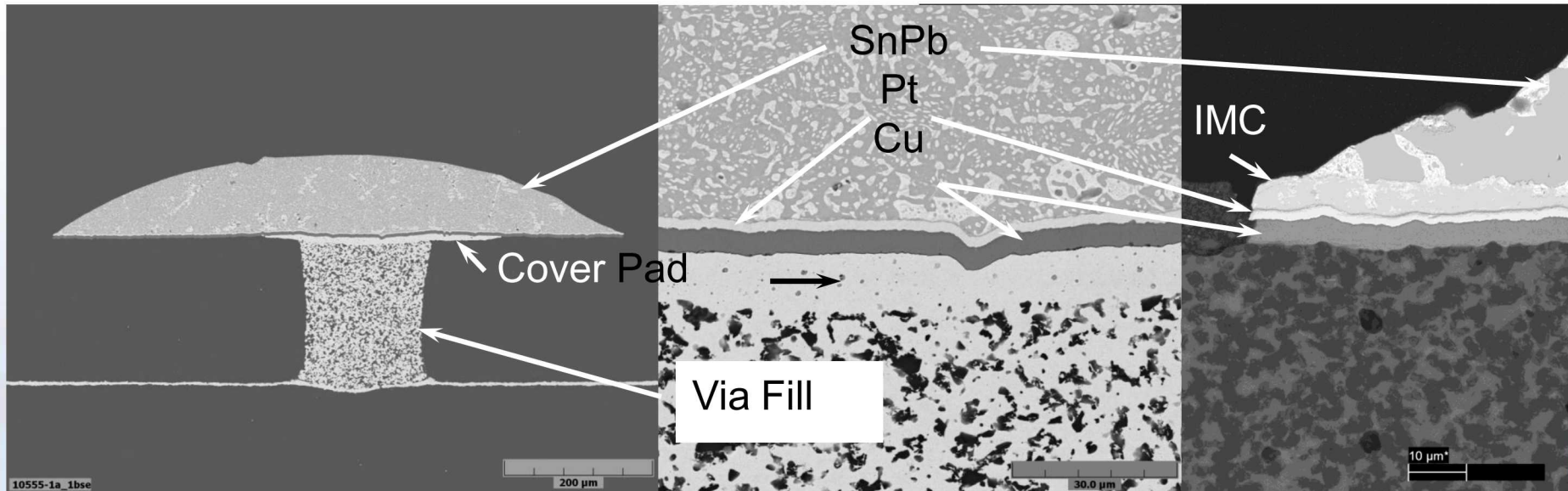
Thin film line edge



Thick film line edge

SnPb Solder Connectivity

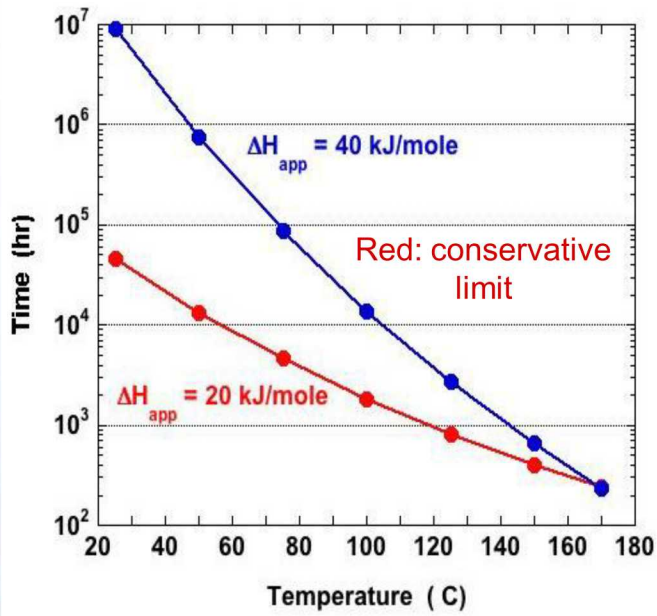
- Thin film surface wets extremely well.
- SnPb dissolves Au, forms intermetallic layer (IMC) with Pt.
- Solder joints exhibit excellent strength:
 - Shear test:
 - 0402 from 4.2lbs as soldered to 3.2lbs after aging at 170°C for 25 days;
 - 0603 from 6.0lbs as soldered to 4.6lbs after aging at 170°C for 25 days;
 - Sebastian-like pull test:
 - Soldering at 214°C: 35lbs after 15s up to 37lbs after 120s;
 - Soldering at 290°C: 27lbs after 15s down to 22lbs after 120s;
 - Approximately 24lbs constant after 1 to 15 5s solder-dipping cycles at 290°C.



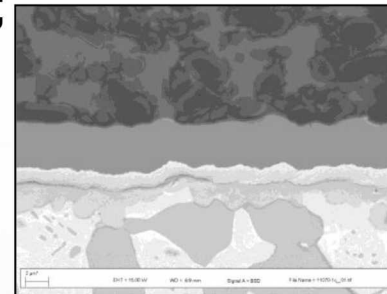
10555-1a_1bse

SnPb Solder Solid State Aging

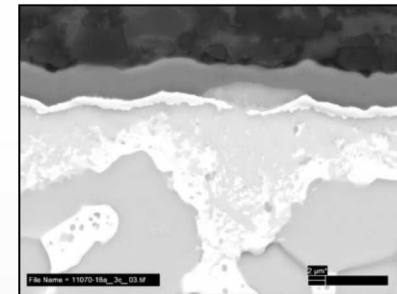
- Temperatures between 55°C and 170°C.
- Times between 2 and 25 days (longer times still under evaluation).
- Without solder: thin film layer thicknesses constant.
- With solder:
 - Breakdown of thin film structure at 170°C between 10 and 25 days;
 - Adhesion not lost after 25 days at 170°C;
 - Assume aging limit is 10 days at 170°C.



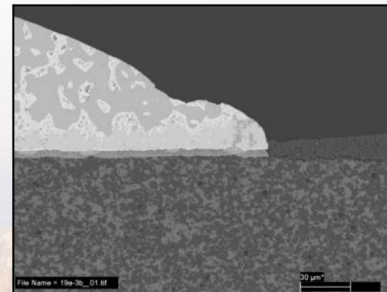
Lifetime limit based on temperature



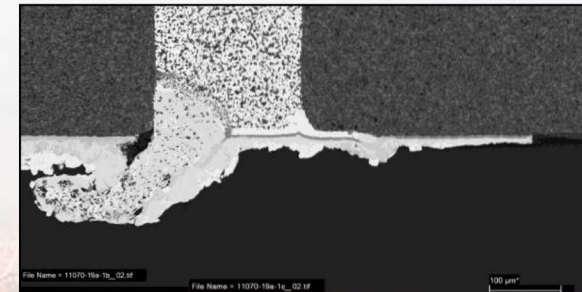
135°C, 10 days
large solder amount



170°C, 10 days
large solder amount



170°C, 25 days, edge,
small solder amount



170°C, 25 days, large solder amount



Benefits from Thin Film on LTCC

- Increased reliability.
- Robust in assembly.
- Versatile in assembly, multifunctional single metallization for soldering and wire bonding.
- Superior reworkability, soldering.
- Superior electrical and RF performance.
- Finer lines and spaces, smaller geometry.
- Enables higher frequencies.
- Positioning for thin film passives (e.g. Band Pass Filter (BPF), capacitors).
- Open to further development, e.g.:
 - AuSn soldering;
 - Fully integrated thin film passives.



The Bane of LTCC

- Shrinkage – not so bad
- Shrinkage tolerance is the problem
- Design rules
- Fabrication practices
- Production quantities--approach



Process Flow for LTCC

- Storage
- Conditioning
- Preparation
- Z-axis features (vias)
- X-Y axis features
- Collation
- Lamination
- Cofiring
- Post-processing



Print, dry cycles



Adaptive Techniques

- Laser direct imaging—custom PR exposure
- Laser ablation—custom dry-removal
- Additive manufacturing-direct write—custom paste placement
- Relaxed design rules



Structuring

- Punching
- Milling (unfired or fired)
- Laser-ablation (unfired or fired)

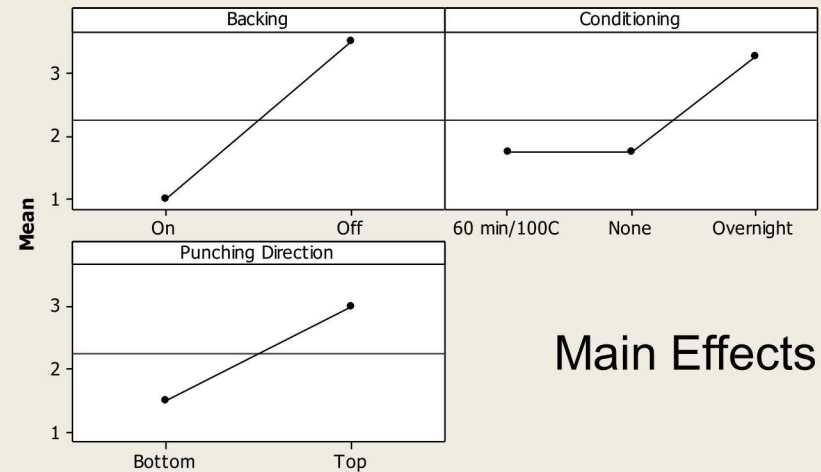
Designed Experiment: Punching

With respect to Surface Cracking
Experimental Matrix

Std Order	Run Order	Backing	Conditioning	Punch Direction	Surface Cracks	Bore Cracks	Perim. Surf. Def.	Ceramic Debris	Entrained Backing	Overall
1	1	On	1h@100°C	Bot	1	1	1	7	4	14
2	10	On	1h@100°C	Top	1	10	7	1	7	26
3	2	On	None	Bot	1	1	4	4	1	11
4	4	On	None	Top	1	1	7	1	1	11
5	6	On	16h@20°C	Bot	1	1	1	4	4	11
6	11	On	16h@20°C	Top	1	7	7	1	1	17
7	9	Off	1h@100°C	Bot	1	4	4	4	1	14
8	3	Off	1h@100°C	Top	4	4	7	4	1	20
9	5	Off	None	Bot	1	4	4	4	4	17
10	8	Off	None	Top	4	10	4	1	1	20
11	7	Off	16h@20°C	Bot	4	7	4	7	1	23
12	12	Off	16h@20°C	Top	7	10	10	1	1	29

Main Effects Plot for Surface Cracks

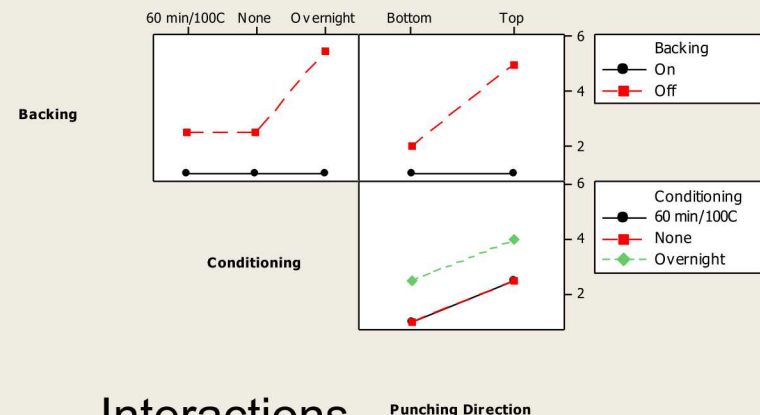
Data Means



Main Effects

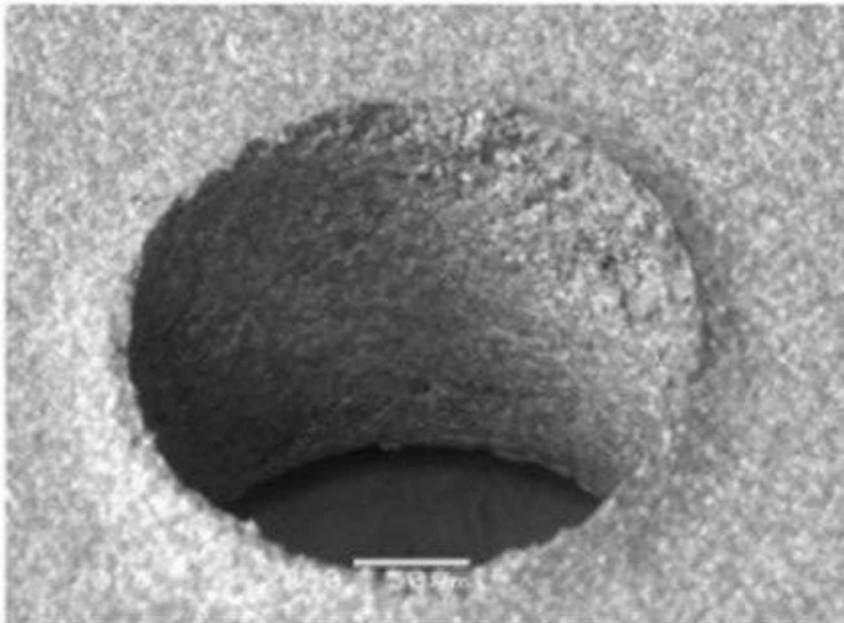
Interaction Plot for Surface Cracks

Data Means

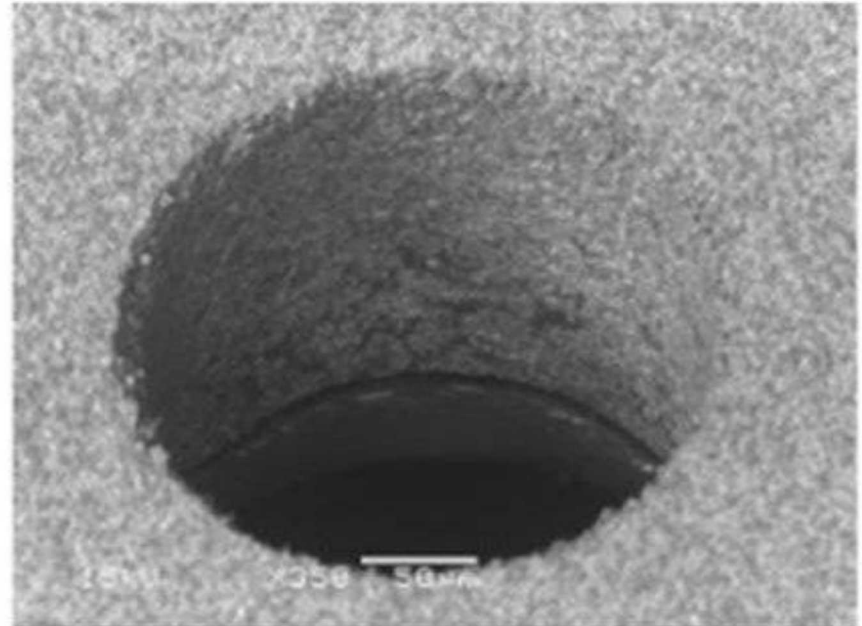


Interactions

Examples



a)
Backing: Off
Pretreat: Room temperature, Punch
direction: Bottom
Equipment: 1
Top View



b)
Backing: On
Pretreat: Room temperature, Punch
direction: Bottom
Equipment: 1
Top View



Milling: “Green-Machining”

- Why Mill Unfired Tape?
 - The best mold insert possible
 - Superior to
 - Metal, elastomer,
- Metallized cavity floors/walls
 - Sense-mode machining
- Drawbacks to Milling
 - Machining rates/material behavior
 - Dulling of tools from a ceramic/glass loaded polymer
 - More time/labor intensive than punching

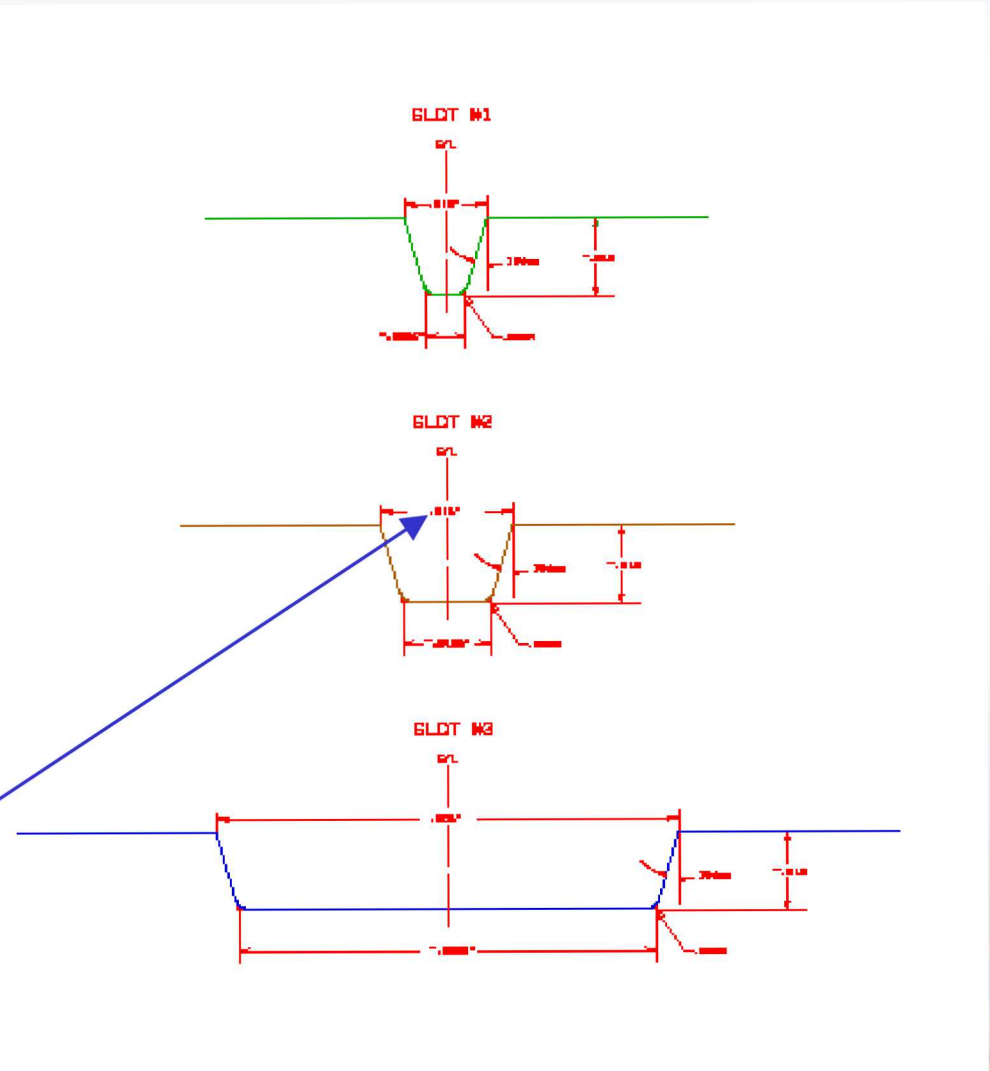
Schmoll Tooling



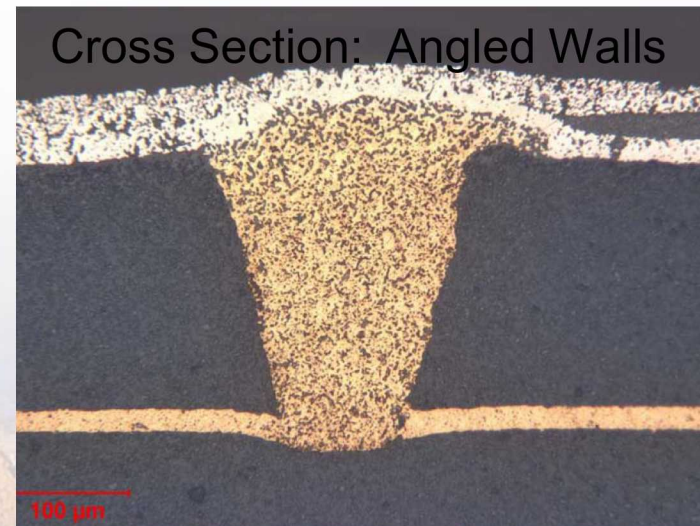
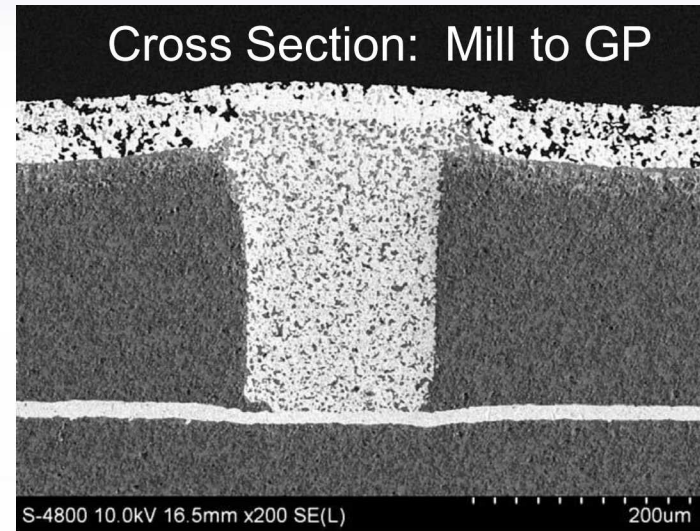
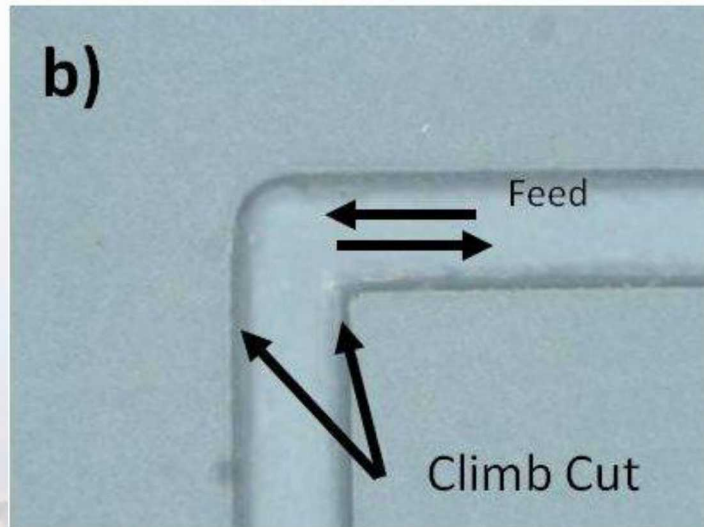
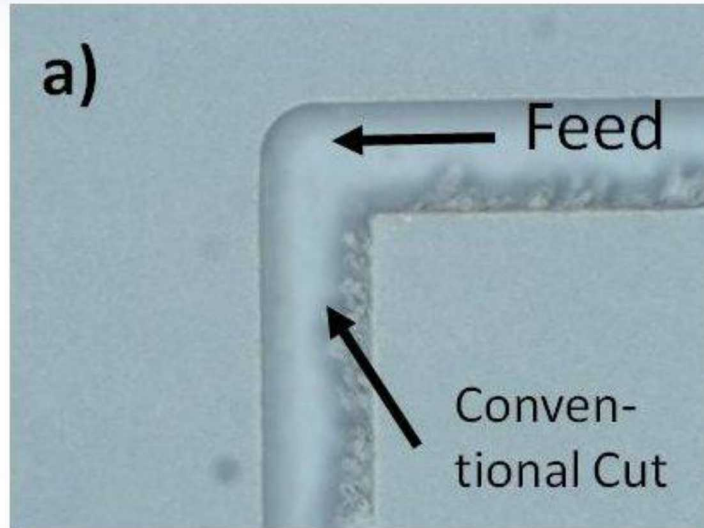
.010" Ø Single Flute End Mill



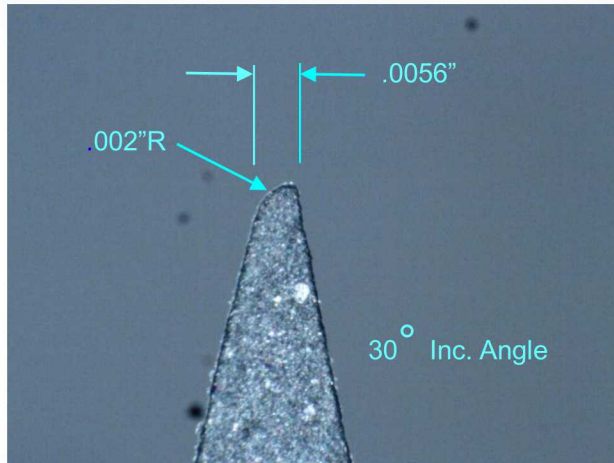
Pantograph Style Tool



Green Machining

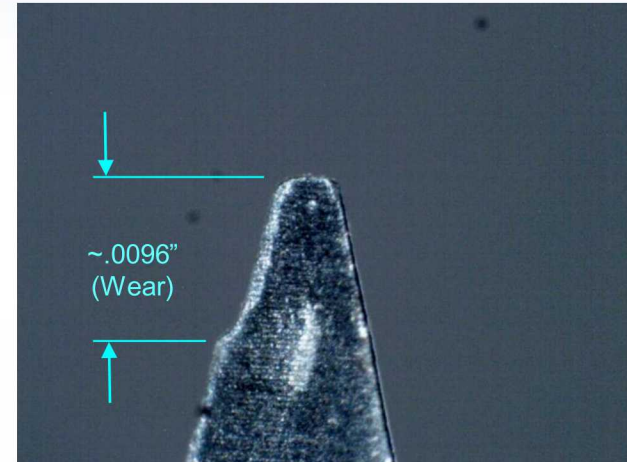


Tool Wear – Engraving Cutters

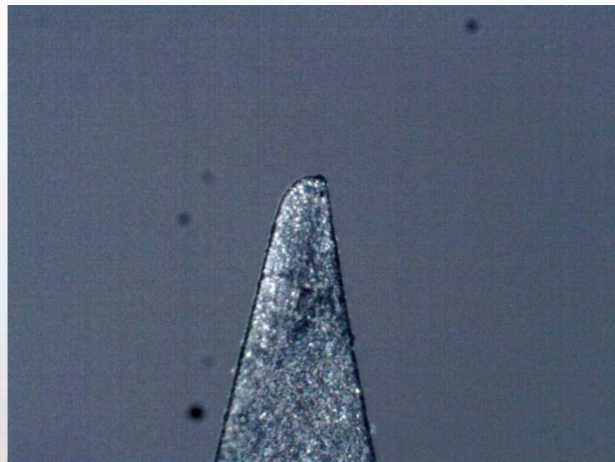


Unused CVD .010" Ø Pantograph Tool

(115x)



Worn non-Coated .010" Pantograph Tool after Milling ~400 linear inches



Used CVD Coated Pantograph Tool after Milling ~2400 linear inches

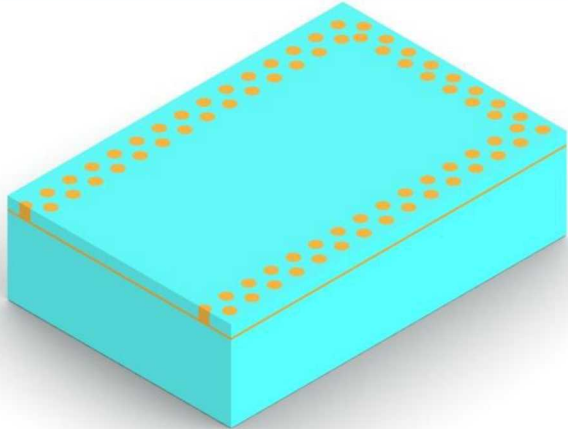
- CVD Diamond Coating 8-10 micron thick “Grown” Directly on Micro-Grain Carbide Tool
- Hardness (88-98 GPa) & COF (.05 - .3) = Diamond
- Provides 50x Cutter Life
- Non-Conductive - Does Not Support Conductive Sensing) Depth Control
- Investigate: Boron Ion Doping of Diamond Coating Cryogenic Treatment (Tempering)



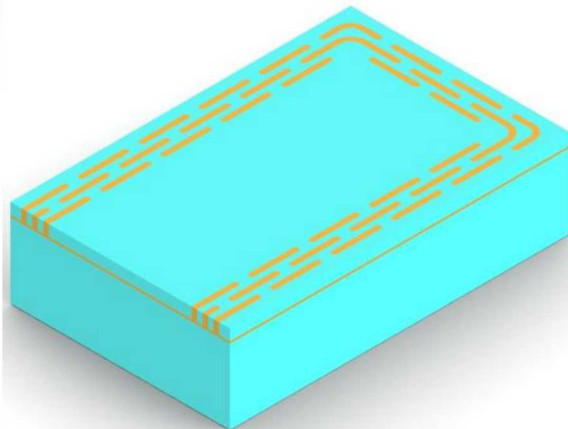
Milled Faraday Structures

- Open trench demonstrated lower stress in seal frame SnPb solder attach
 - Evolution from prior work FTTF to current configuration
- Trench milling process variations
 - “To the ground plane” (continuity-sense milling)
 - “Through the ground plane” (controlled-depth milling)
- Yield issues when milling “to the ground plane”

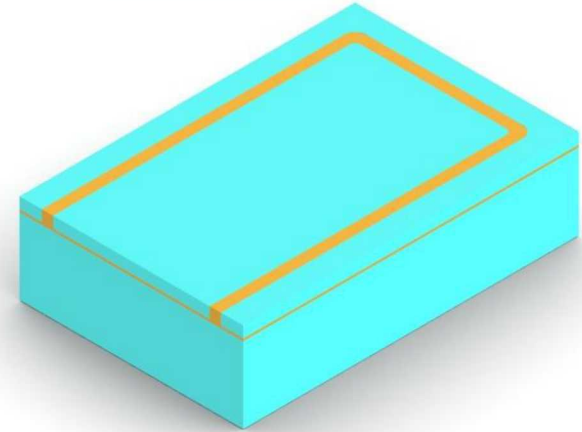
Faraday Cage Evolution



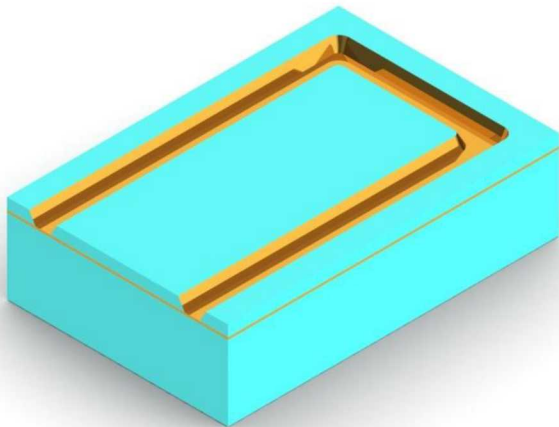
Typical via fence configuration



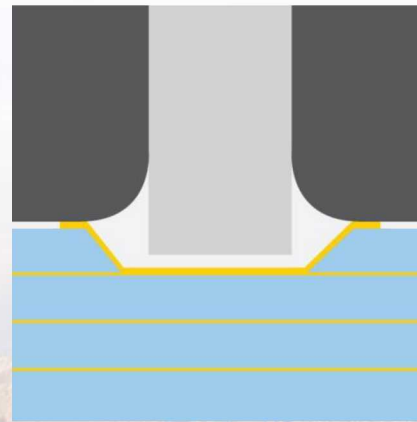
Staggered "racetrack" slot configuration



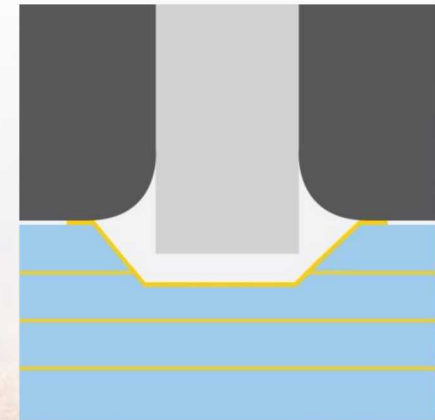
FTTF forming continuous isolation structure



Green state milled valley



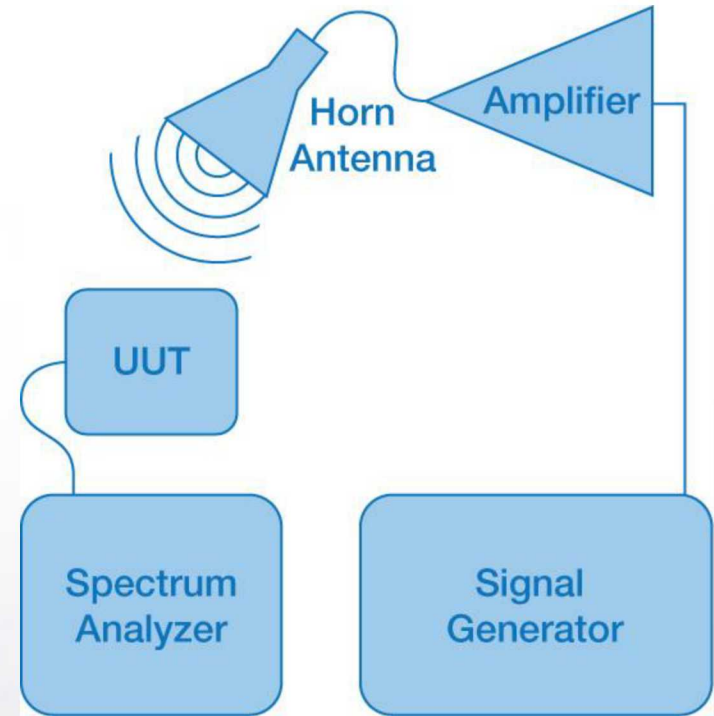
Continuity-Sense Milling



Controlled-Depth Milling

EMI Isolation Test

- Built receivers using both processes
- Tested in anechoic chamber
- Terminated RF input (no signal)
- Generated external RF “interferer” directed at UUT with horn antenna
- Measured output on spectrum analyzer from multiple EMI frequencies
- Calculate EMI isolation delta between two processes



Results

- Controlled-depth milling found to degrade EMI isolation
- Average reduction in isolation of 16.6 dB
- Equates to 45.7 times greater signal power entering receiver
- Expect twice as much degradation in system
 - 33.2 dB reduced isolation
 - 2089.3 times more signal leaking from transmitter to receiver
- May or may not be tolerable – system dependent

Applications of Laser Etching

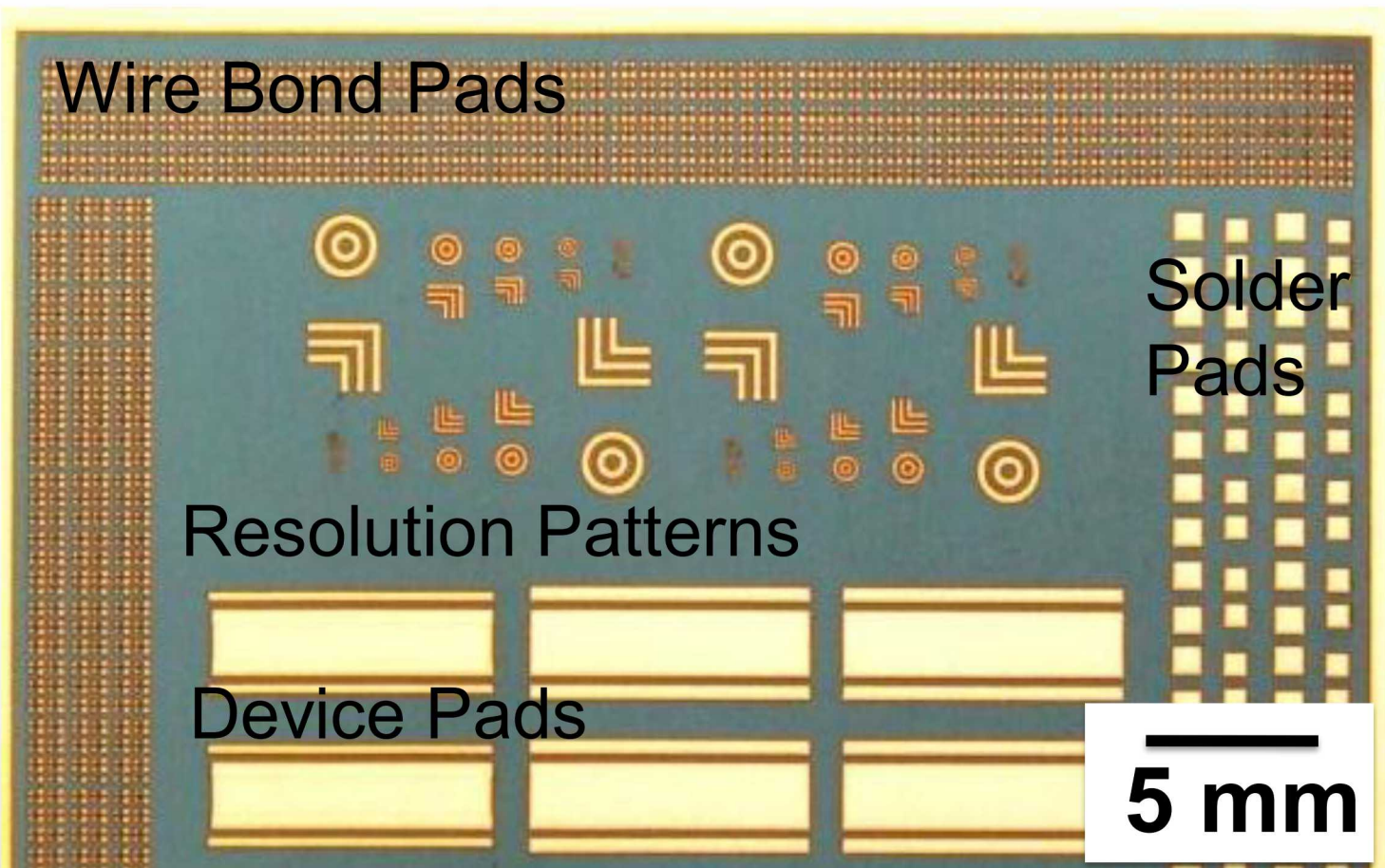
- Definition of conventional circuitry
- Minimal etching approach
- Definition of unfired circuitry
- Depth engraving to a buried ground plane

DOE Summary

- 355 nm diode-pumped, tripled Nd:YAG UV Laser
- Thin film stack:
 - 0.20 μm Ti
 - 4.0 μm Cu
 - 2.0 μm Pt
 - 0.38 μm Au
- Hatch – parallel raster, single direction
- Cross-hatch – two hatch cuts in orthogonal directions
- Analysis (top view, cross section)
 - Optical photos
 - SEM
 - a) Secondary electron
 - b) Back scattered electron - EDX maps of elements

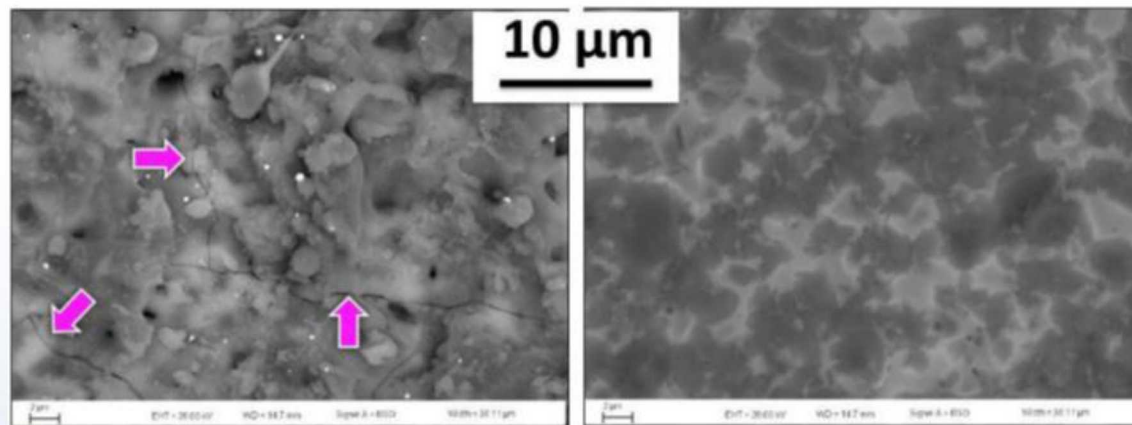
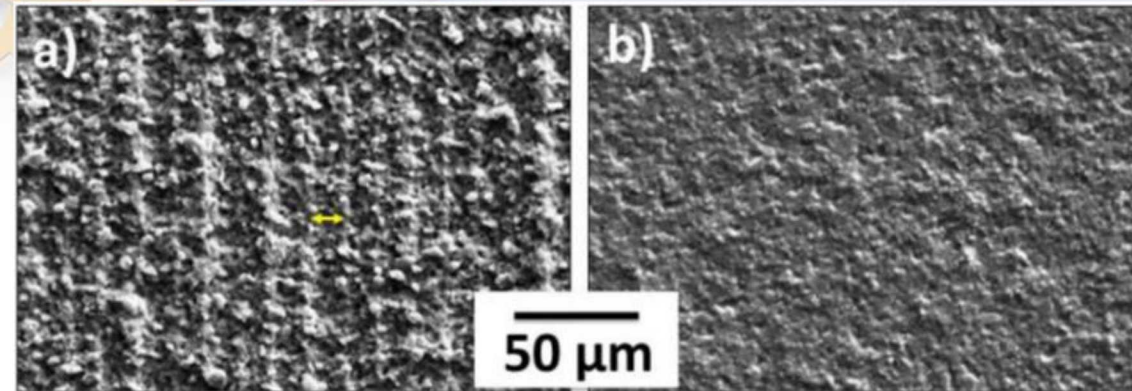
Experimental Phase	1	2	3	4
Laser Model	U	U	U3	U3
Power (W)	2.5 - 3.0	2.5 - 3.0	6.7	1.1 / 0.5
Frequency (kHz)	150	150	150	75
beam spot size (μm)	20	20	15	14
beam pulse (μs)	15	15	12	7
Travel Speed (mm/sec)	75	100	100 - 250	600
Air Knife	NO	NO	NO	YES
Contour Reps	2	1	1	0 - 2
Hatch Reps	2	1	1	1-6*
			* Cross-hatch used	

Sample Features



- LPKF U1 UV Laser
- SEM/SE and BSE images follow [W](#) Sandia National Laboratories

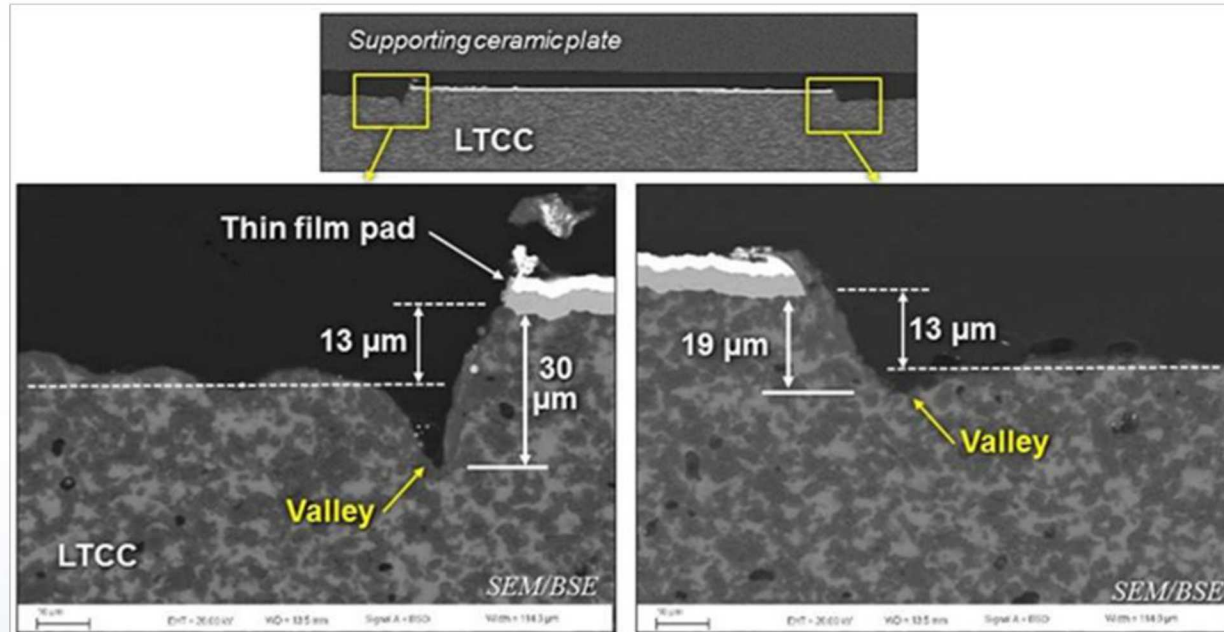
Phase Two Cont.



- Can next-assembly environmental shock-and-vibration conditions cause catastrophic failures ?

- Hatch cut, single orientation (top-to-bottom)
- Grooves, 10-15 μm wide (yellow arrow)
- Redistribution of the SiO₂ and Al₂O₃ phases.
- Increased porosity
- Rapid melting / resolidification of the LTCC surface (rounded particles).
- Surface cracks (magenta arrows)

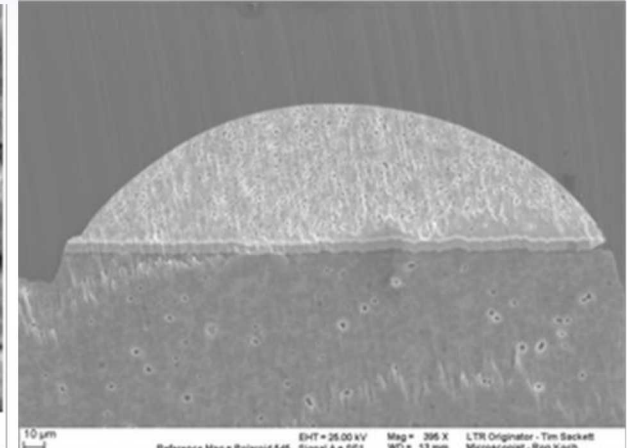
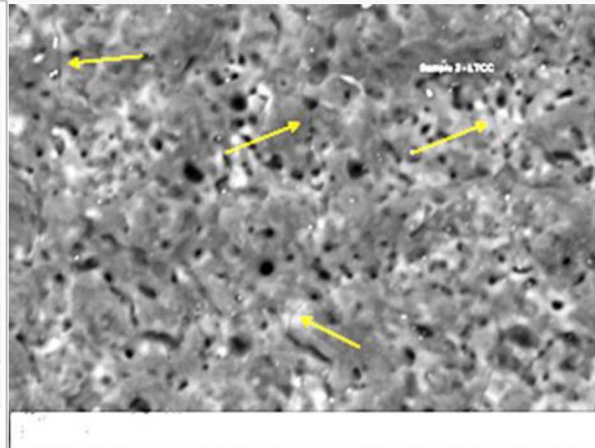
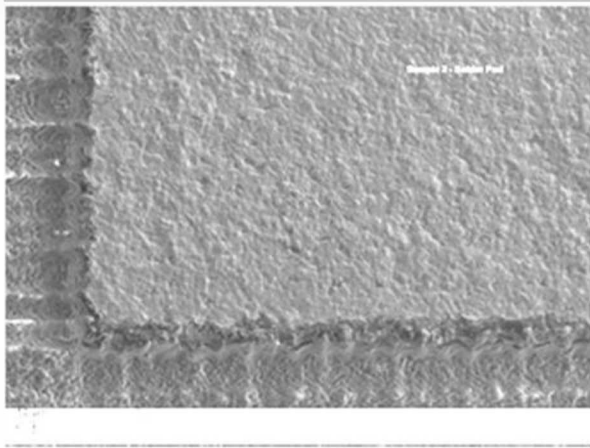
Phase Three Structure



U3 process parameters:

- 6.67 watts laser power
- 15 μm beam spot size
- 12 μm beam pulse width
- 250 mm/s travel speed
- One hatch/contour pattern

Phase Four



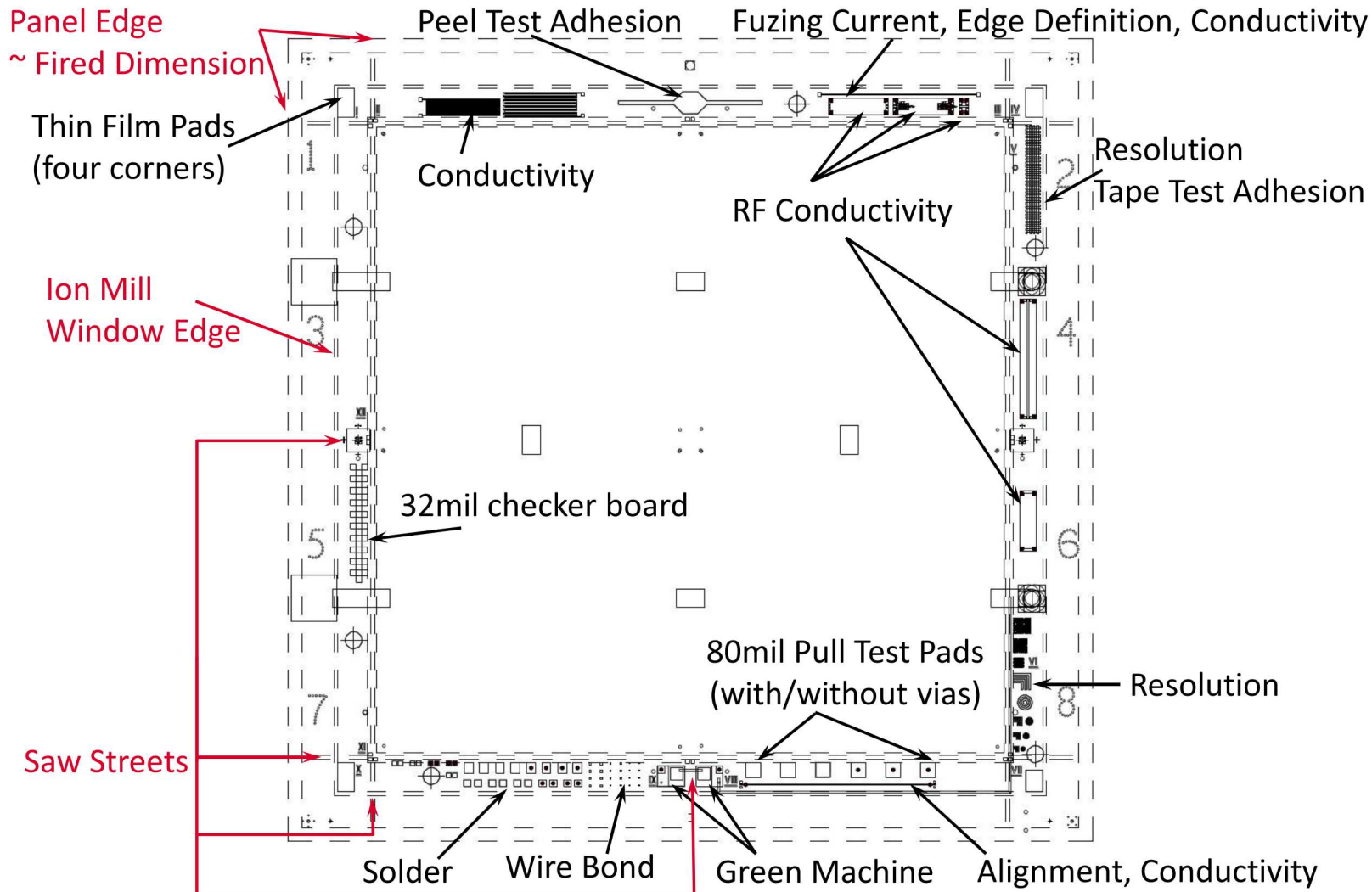
U3 process parameters:

- 1.1 watts laser power
- 75KHz beam frequency
- 14µm beam spot size
- 17µm beam pulse width
- 600 mm/s travel speed
- Four cross hatch cuts
- No contour cuts

Results

- Micro-cracking was reduced.
- Excellent wire bonding strengths, 12.25g avg pull strength, 0.77 std
- Solderability was excellent.
- Cleaning step was necessary to removal laser slag and FOD.

Thin Film Edge Monitor on LTCC



What do we want to test?

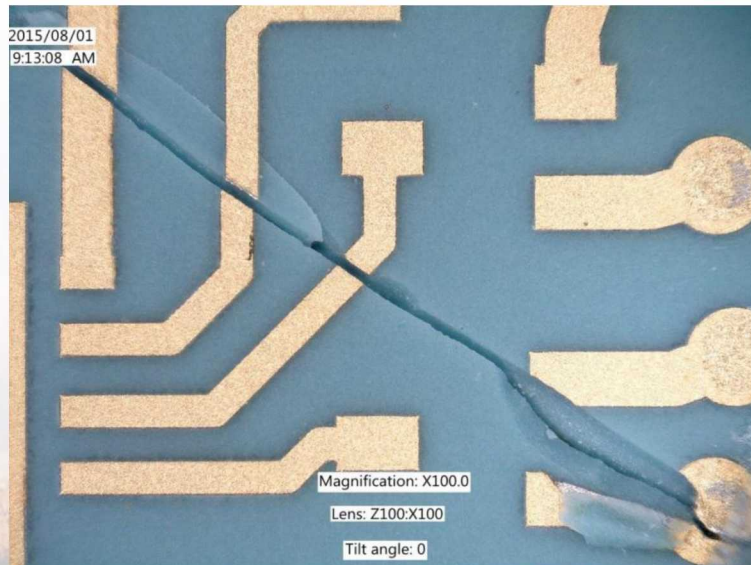
- Adhesion
 - Sebastian-like pull test
 - peel test
 - tape test
 - soldered device shear test
 - wire bond pull test
- Resolution
 - 10, 5, 4, 3, 2, 1mils lines and spaces
 - Checkerboard
 - 'L'-shape
 - concentric circles
- Edge definition/acuity
 - straight line conductor, 4mils
- Fuzing current
 - straight line conductor, 4mils
- Conductivity
 - straight line conductor, 4mils
 - meandering conductor, 4 and 6mils
 - thick film buried structure
- RF Conductivity
 - 50Ω line (6mils?)
 - de-embedding structures
- Solder test
 - 0402, 0603, 0804
 - with and without vias
- Wire bond test
 - 12, 8, 6mil pad pairs
- Alignment
 - TF to via to buried thick film structure
- Sheet resistivity
 - thin film pads
- Contamination
 - thin film pads
- Aging
 - thin film pads
- Green machine feature
 - two small (30mil?) features, tented with photo resist?
- Film thickness
 - off-substrate witness sample



Peel Origins

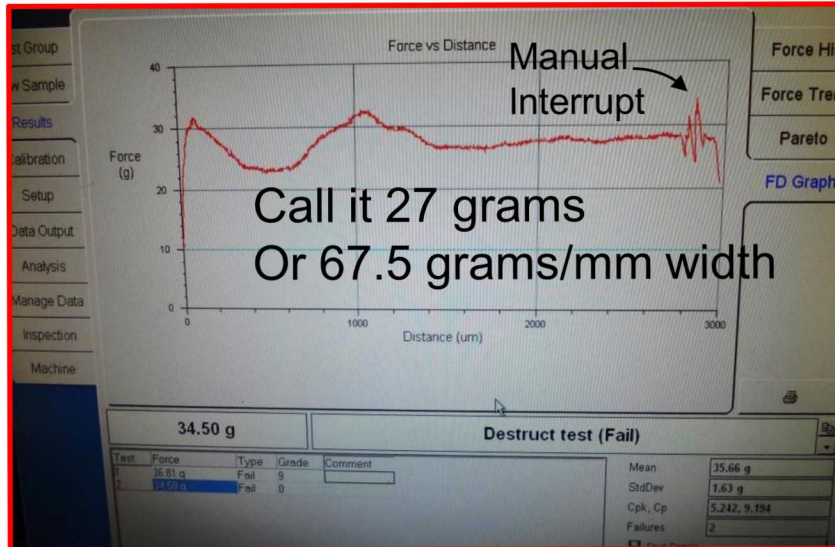


Other drastic measures to initiate peel

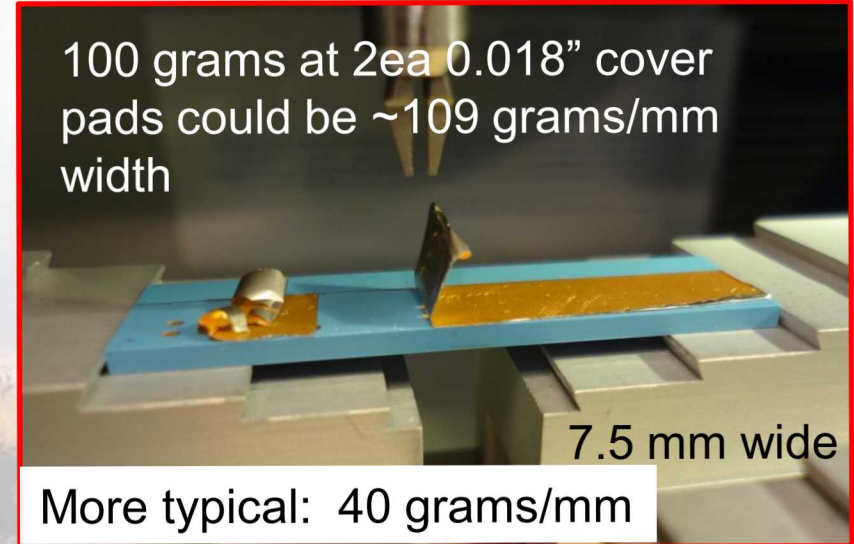
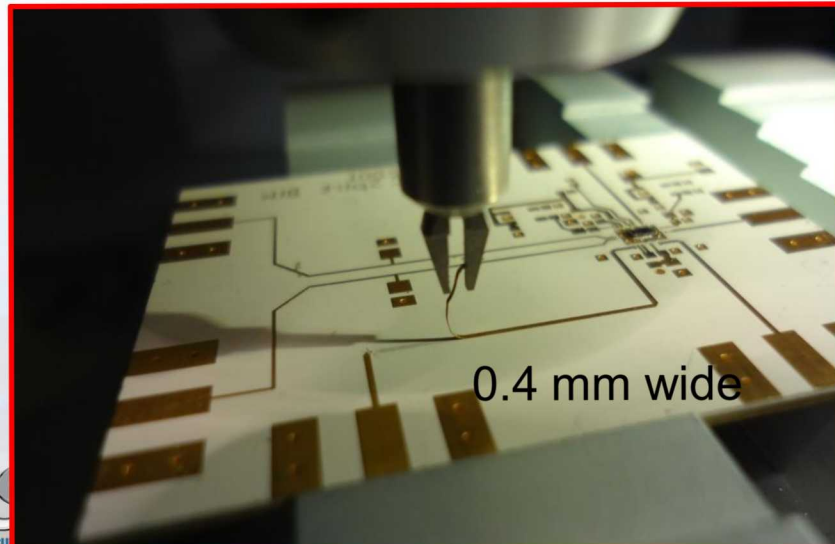
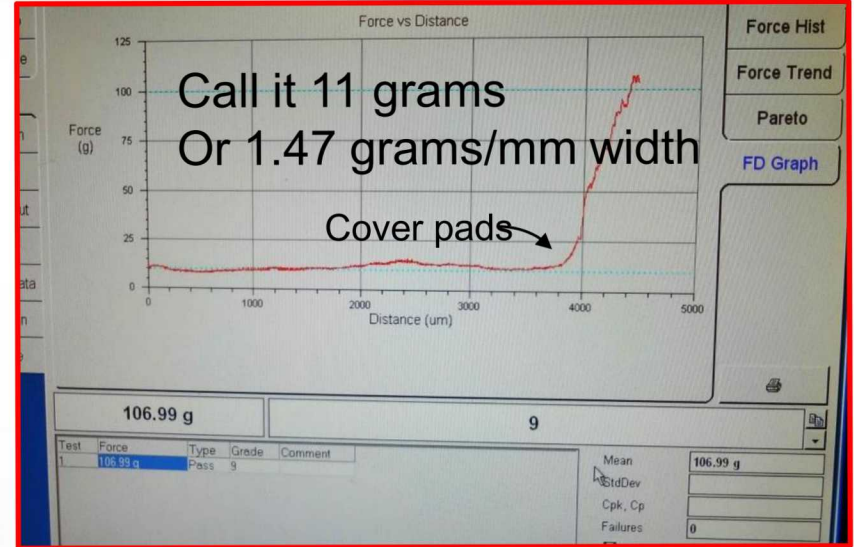


Quick comparison PWB - LTCC

PWB 400 micron wide trace



Thin film on LTCC Monitor





Summary

- Novel applications opportunities are vast.
- Shrinkage tolerance control is paramount.
- Structuring techniques continue to progress.
- Thin films are effective, if not conventional
- A reliable, integral thermal solution is desired.



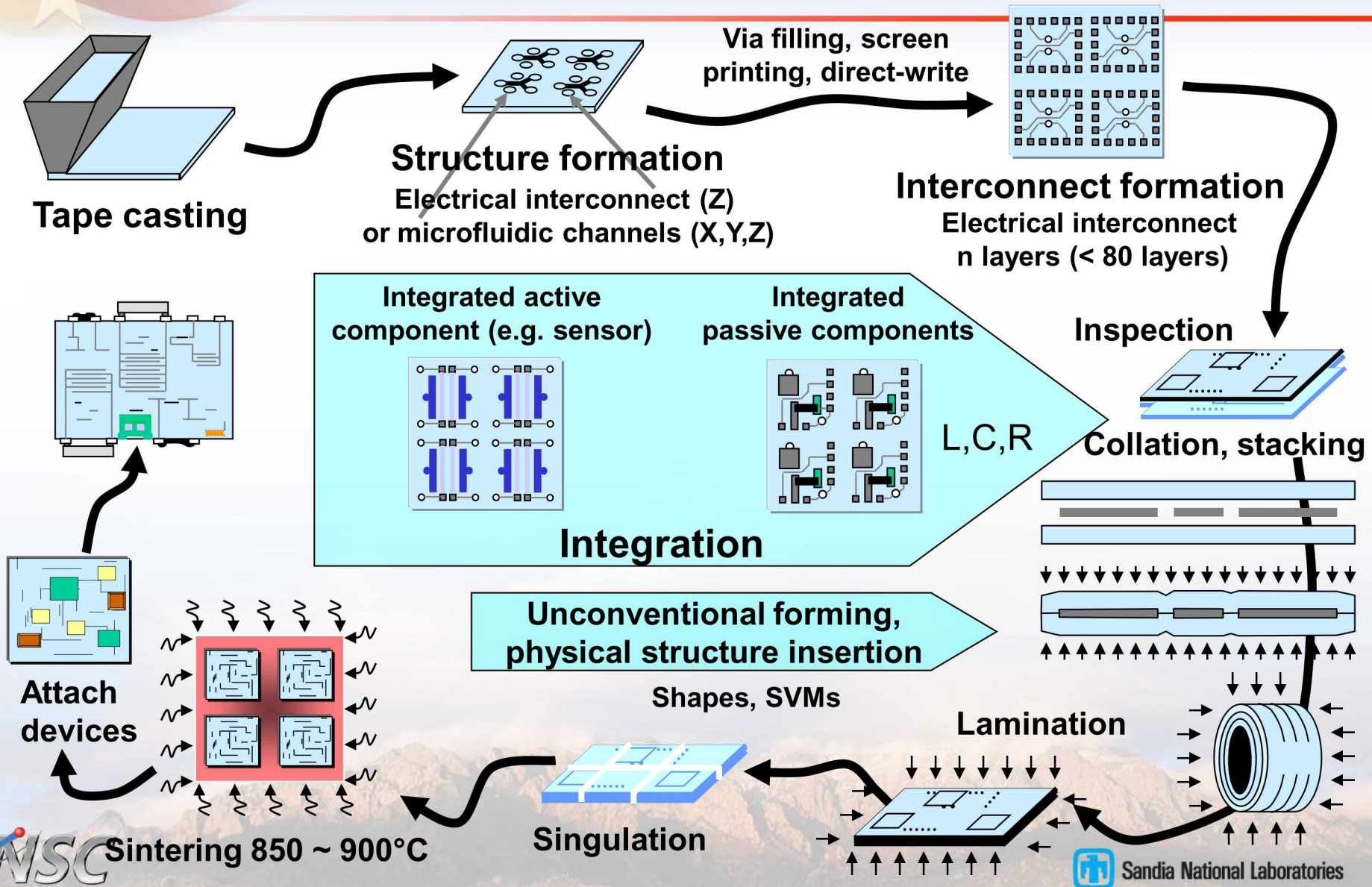
Acknowledgements

- Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.
- The Department of Energy's National Security Campus is operated and managed by Honeywell Federal Manufacturing & Technologies, LLC under contract number DE-NA0000622.
- Rory Grondin, LPKF



Thank you for your attention

LTCC Processing



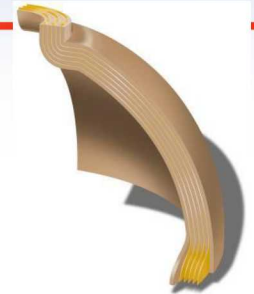
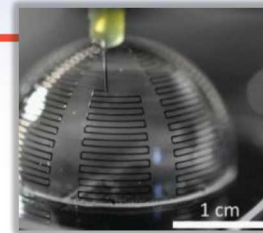
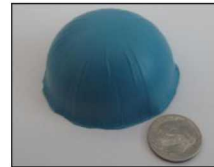


Bulk Inclusions

- EMI shielding structures
- Heat sinks
- Filters
- Familiar problem: What metamaterial achieves primary purpose while remaining integral to structure?
 - Adequate thermal conductivity with proper CTE?
 - Cofirable
 - Assembly (post-processing)

Direct Write Electronics

- No screen prints or photo masks
- Print circuits on complex shapes



Freeform Circuit Concept

Use Direct Digital, 3D printing technology in multiple materials to move away from traditional planar circuit shapes.

Aerosol Jet Printing

AJP Technology

Non-contact – aerosolized particles in sheath gas

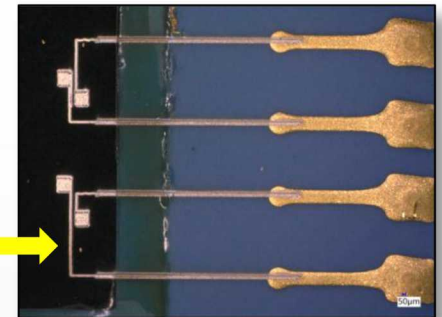
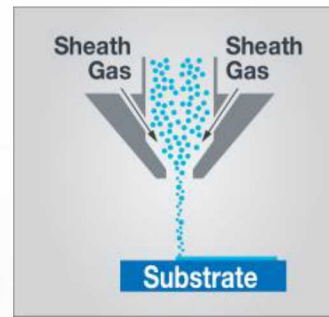
Work space – 12 x 12 x 2 inch

Minimum line width 10 μm

Minimum pitch 20 μm

Advantages: Resolution, surface standoff for non-uniform surfaces

Disadvantages: Build speed, material selection is limited



Micro Dispensing

Micro Dispensing Technology

Near contact – positive displacement pump

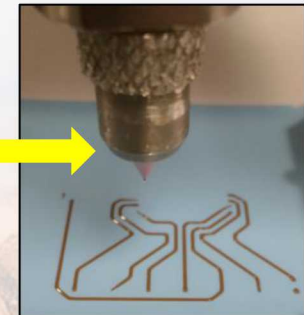
Work space – 12 x 6 x 4 inch

Minimum line width 50 μm

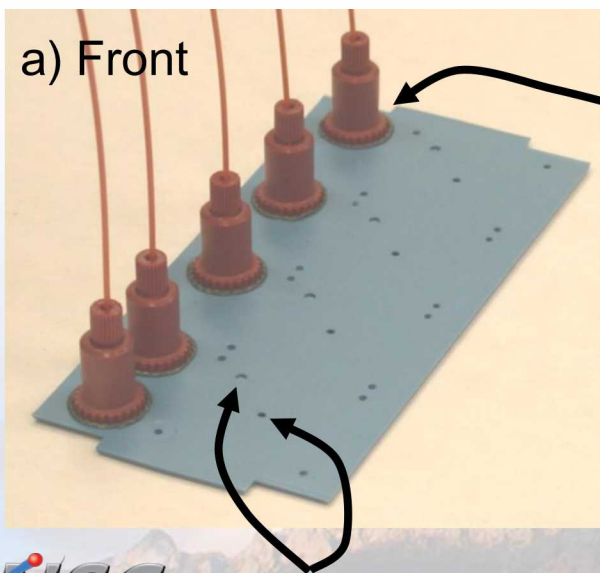
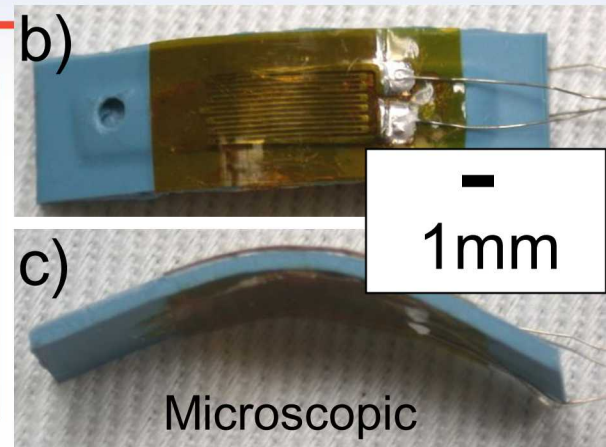
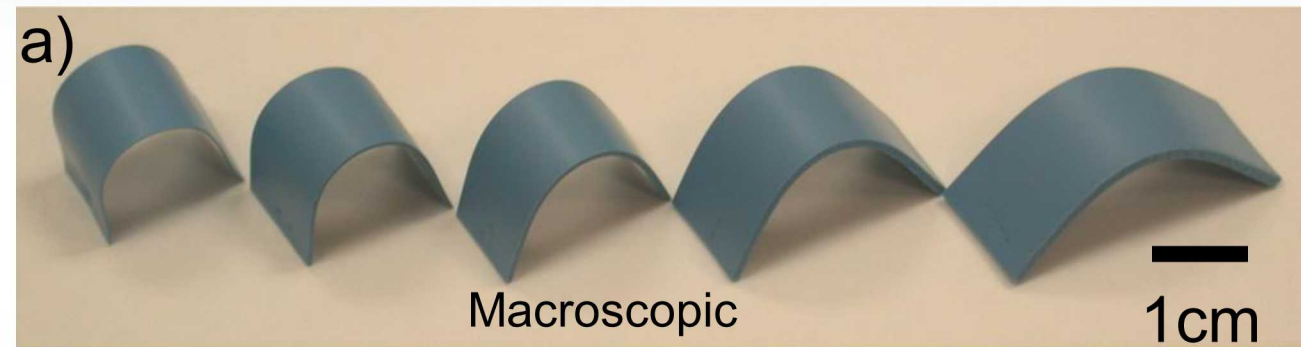
Minimum pitch 100 μm

Advantages: Utilizes WR qualified materials

Disadvantages: Limited ability to print on non-uniform surfaces



Shaped Structures



Commercial ports

