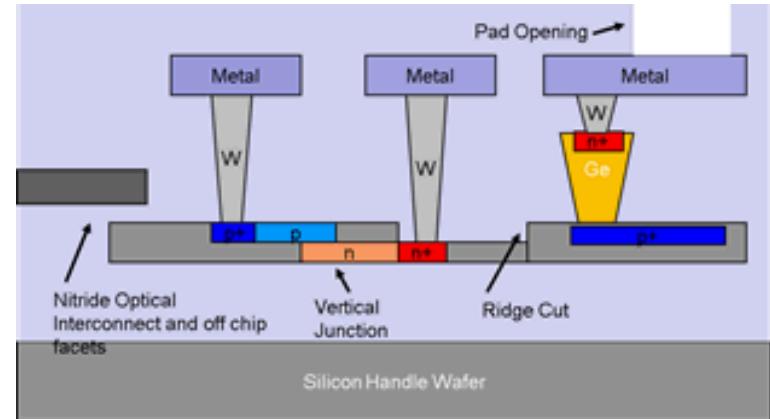
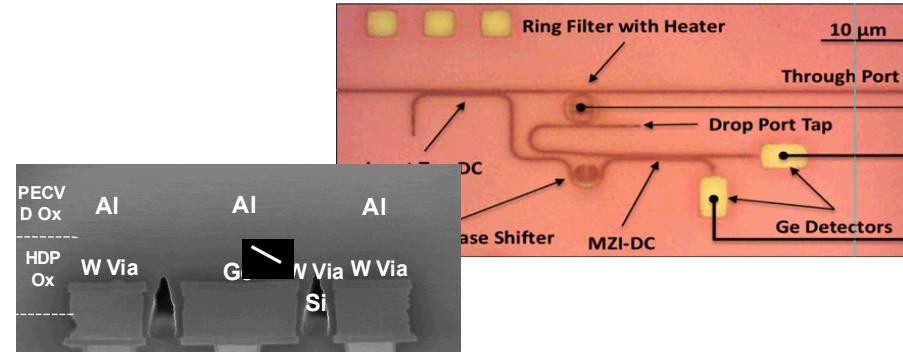


# Sandia Silicon Photonics MPW

- Sandia's Role
  - Not to compete with Industry
    - Focus on what you cannot get elsewhere
    - Collaborative research best
    - Custom work possible within MPW framework or separate program
  - Generally 2-3 offerings per year
- Process features
  - Silicon passives (silicon rib, ridge guides, silicon nitride guides)
  - Silicon actives (modulators, switches, efficient tuning devices)
    - Vertical junctions for efficient devices
  - Germanium detectors
- Contacts
  - Patrick Chu: [pbchu@sandia.gov](mailto:pbchu@sandia.gov)
  - Anthony Lentine: [alentine@sandia.gov](mailto:alentine@sandia.gov)
  - Michael Gehl: [mgehl@sandia.gov](mailto:mgehl@sandia.gov)
  - Chris DeRose: [cderose@sandia.gov](mailto:cderose@sandia.gov)



6.2.1 Si Cut (GDS layer 1)  
This layer is etched after the definition of the partial ridge etch. Fully etched waveguides, ring and disk resonators, directional couplers, etc. are all defined in this step. The design rules for this layer include the following:

- Minimum line width of 100 nm
- Minimum space (line to line) separation of 280 nm
- Minimum taper point 80 nm. (Note tapers coming to an 80 nm point should be less than 200 nm long)
- Minimum overlap with Ridge layer of 500 nm on all sides (Note: either Si overlaps Ridge or Ridge Overlaps Si). This rule may be difficult to implement in some cases, e.g. rib-to-ridge waveguides. In these cases, the design rules for the Ridge layer should be followed (see Section 7).
- Recommended waveguide width of 400 nm with a minimum bend radius of 1.75 μm.
- Recommended waveguide width to couple to ring/disk resonators of 320 nm.

The design rules for the ring/disk resonators are illustrated in Figure 6-1, and SEM images of the effects of design rule violation are shown in Figure 6-2.

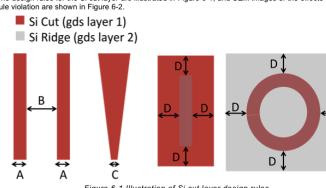
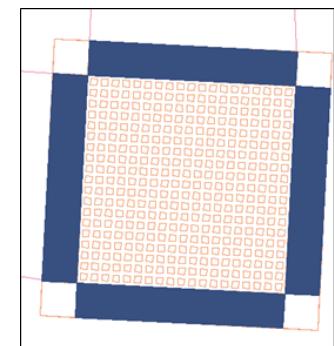
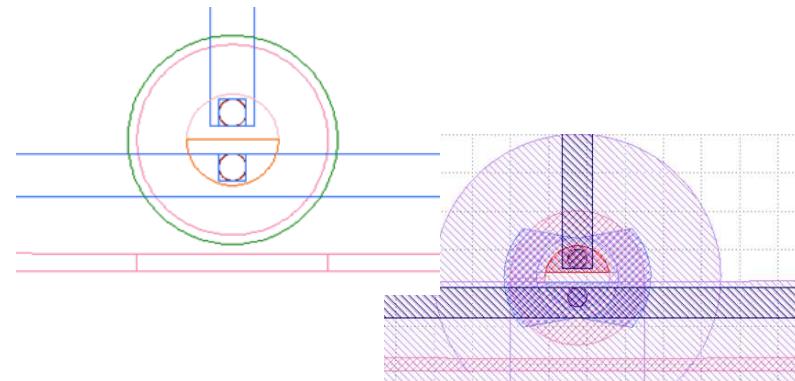


Figure 6-1 Illustration of Si cut layer 1 design rules



# Design Tools and Schedule

- Design tools and features
  - Phoenix Optodesigner pdk
  - Design guide with dimensions, layer definitions
  - Working with Lumerical to implement compact models (in progress)
- Preliminary Schedule
  - October 2017 (full run)
  - April 2017 (Silicon Only)
  - October 2018 (full run)
- Target sequential deliveries after tape out:
  - Passive (2 months)
  - Active Silicon only (4 months)
  - Active Silicon and Germanium (8 months)
- 100 mm minimum area per funding source



- Phoenix Optodesigner library devices
  - Passive waveguides
  - Grating and edge coupling
  - Polarization beam splitters
    - In-plane and grating coupled
  - SiN to Si transitions and crossings
  - Directional, Adiabatic, and MMI couplers
  - Standard or adiabatic ring filters
  - Mode filters
  - Mach-Zehnder modulators
    - Thermal, EO, traveling wave
  - Micro-disk modulators
  - Disk modulator and ring filter silicon thermal tuning elements
  - Germanium detectors
  - ...