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High Aspect Ratio X-Ray Gratings Enabled by Pt ALD

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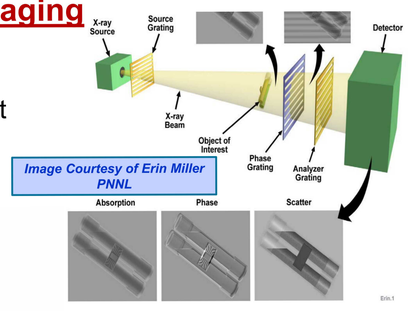
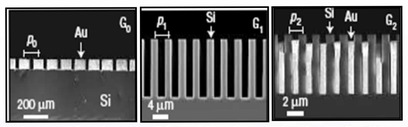
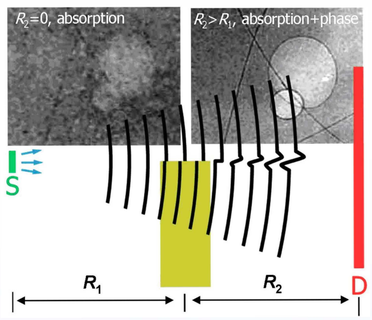
The combination of Atomic Layer Deposition (ALD) conformal coating of conductive seed layers and Electro-Chemical Deposition (ECD) offers unique capabilities for new device creation. These technologies have been combined to enable deep micro-structured transmission gratings used as optical elements in X-ray phase contrast imaging (PCI). Utilizing mold construction methods such as UV lithography and Deep Reactive Ion Etching (DRIE), single micron features with >26:1 aspect ratios have been fabricated in silicon wafers. These high aspect ratio silicon support structures were utilized as molds for a tailored pulse plating deposition of gold to create the x-ray gratings over large areas, 100 cm^2. Electrochemical deposition techniques require conductive supports which were created by uniformly depositing Pt on the silicon by ALD with precursors of (Trimethyl)methylcyclopentadienylplatinum and oxygen.

X-Ray Phase Contrast Imaging

- **Source Grating**: Creates an array of individually coherent but mutually incoherent sources
- **Phase Grating**: Creates zero and π phase shifts to form an interference pattern
- **Analyzer Grating**: Modulates interference signal on detector (local fringe position→single intensity variation recorded by detector







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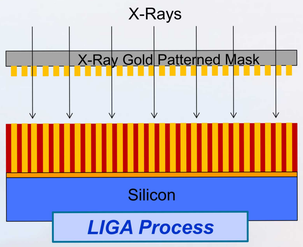
Benefits of XPCI

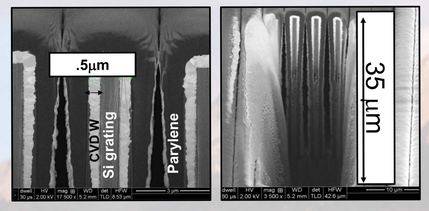
- Eliminates need for high flux synchrotron
- Higher resolution imaging ability
- Simplified optical arrangement
- Wide Area Imaging

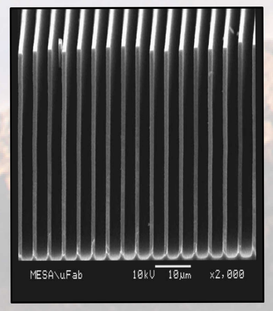
Greater than 25:1 Aspect Ratio Gratings Needed to Enable XPCI



- LIGA → resist swelling and structural instability.
- CVD Tungsten → high stress (requiring parylene compensation) and non-conformal coatings.
- DRIE Si can achieve > 50:1 Aspect Ratios and have high structural stability

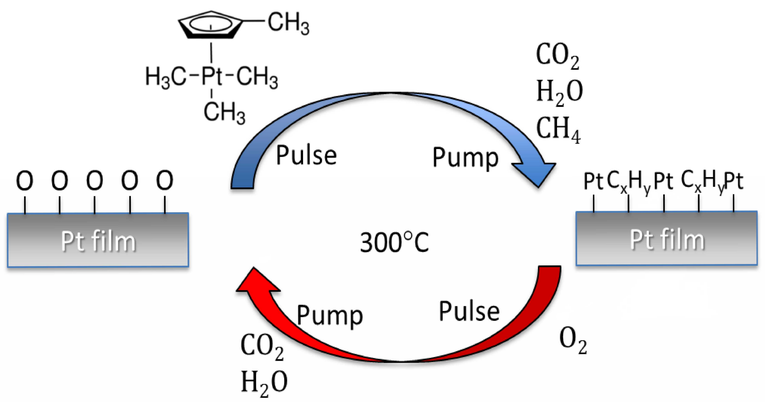
CVD Tungsten with Parylene Coating



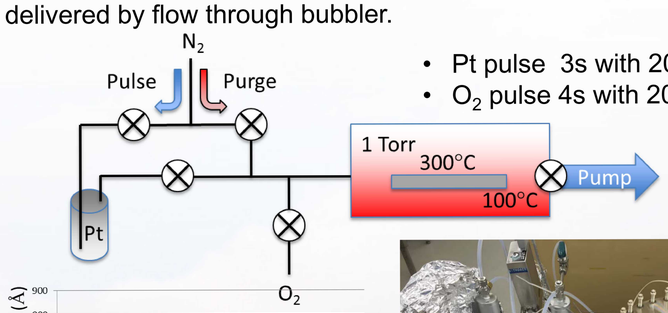


50 micron deep trenches

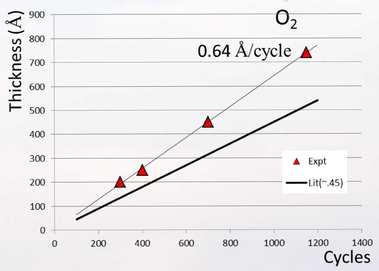
ALD Deposition of Pt Seed Layer

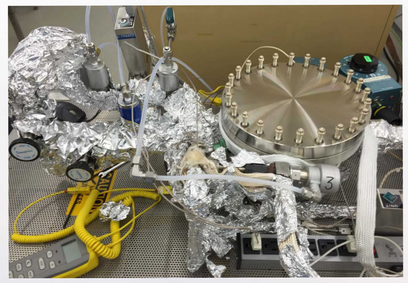


Thermal ALD was processed in a custom built flow reactor with warm walls and hot wafer stage. Pt precursor was heated to 75°C and delivered by flow through bubbler.

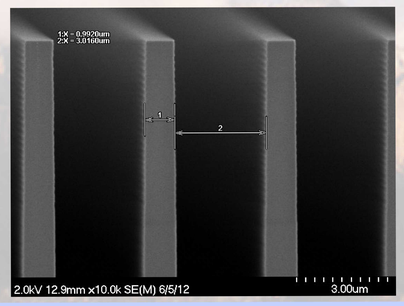


- Pt pulse 3s with 20s purge
- O_2 pulse 4s with 20s purge

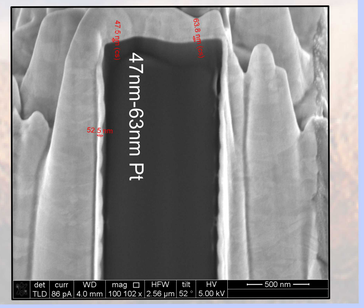




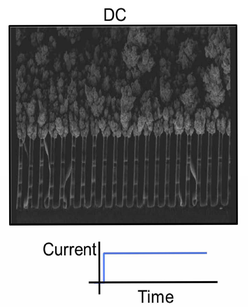
DRIE Si scaffold

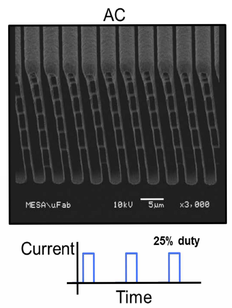


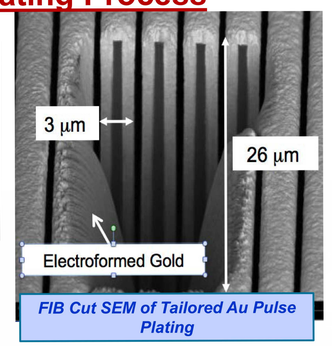
Plated Au on 50nm ALD Pt



Optimization of the Au Electroplating Process

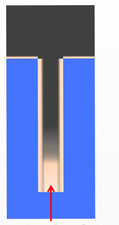






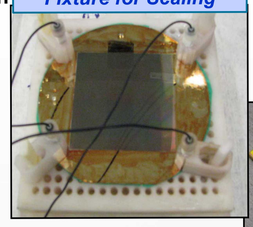
FIB Cut SEM of Tailored Au Pulse Plating

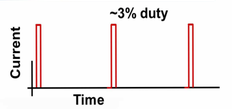
■ Max (bulk) Ion Concentration



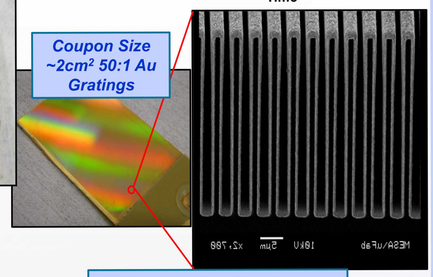
Severely depleted region

Multi-Point Contact Fixture for Scaling



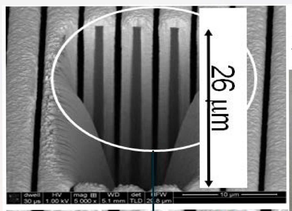


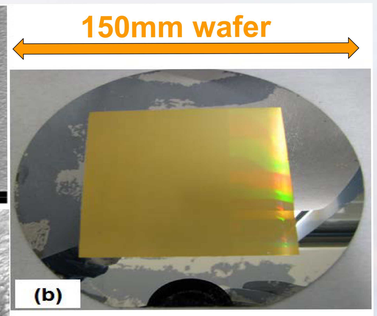
Coupon Size ~2cm² 50:1 Au Gratings



Full Wafer Gratings Plating

Realized 100cm² Grating Area
ALD conformal seed layer; Vibrating sample fixture; Pulse electroplating





100mm Long x 1μm wide Au gratings
100,000:1 Length:Width Ratio!

(a) 26:1 aspect ratio DRIE silicon trenches, ALD Pt seedlayer, and 1.2 micron of gold ECD; (b) large area PCI grating, 100 cm^2

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