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Very large scale integrated optical interconnects: Coherent optical control systems

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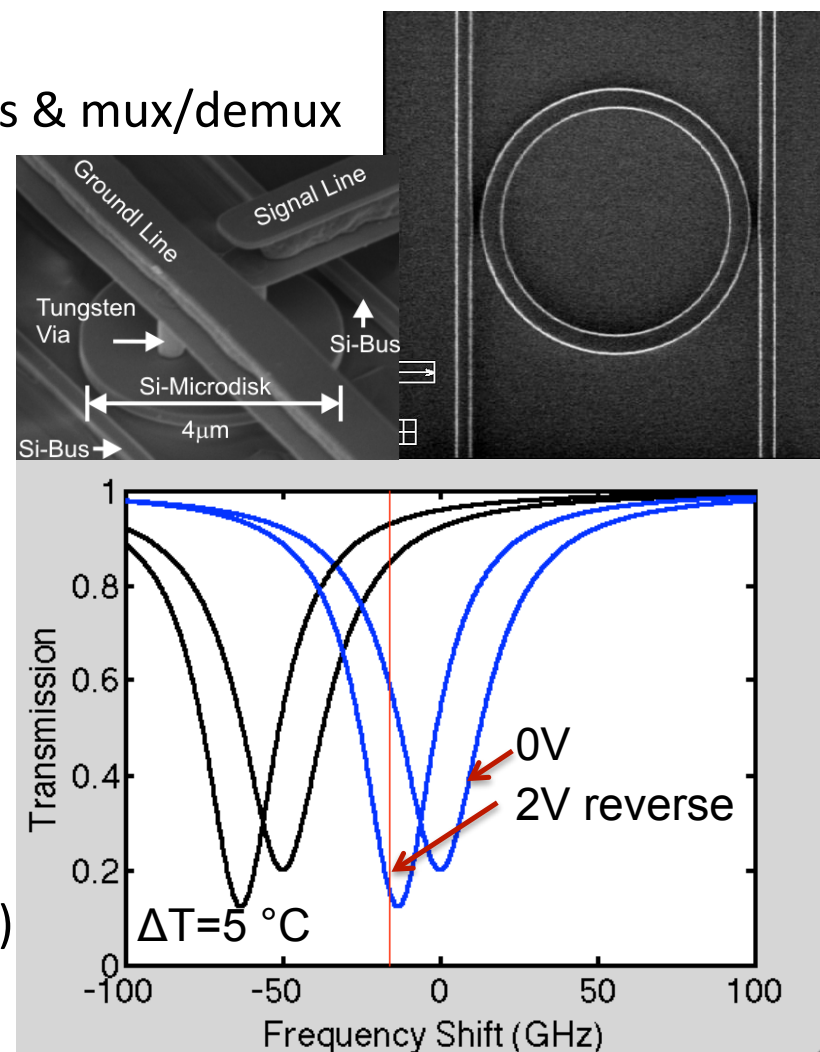
2014 IEEE AVFOP



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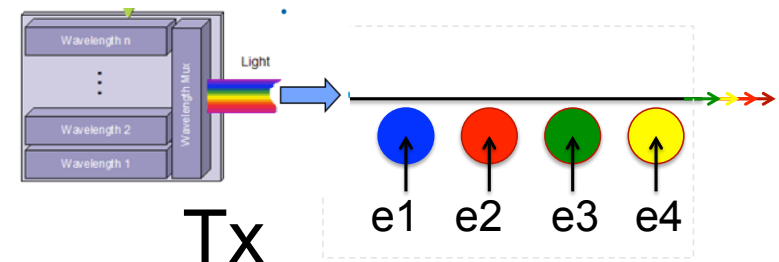
Resonant silicon micro-photonics

- Why resonant silicon photonics?
 - Small size (<4 μm dia.)
 - Resonant frequency $\rightarrow$ DWDM modulators & mux/demux
- Benefits
 - Low energy ($\rightarrow$ 1 fJ/bit)
 - High bandwidth density ($\rightarrow$ 1 Tb/s/line)
- Resonant Variations
 - Manufacturing Variations
 - Temperature Variations
 - Optical Power (1s density)
 - Aging?
- Requirements:
 - Resolution: ± 0.25 $^{\circ}\text{C}$ (1 dB Laser penalty)
 - Range: 0 – 85 $^{\circ}\text{C}$ (depending)

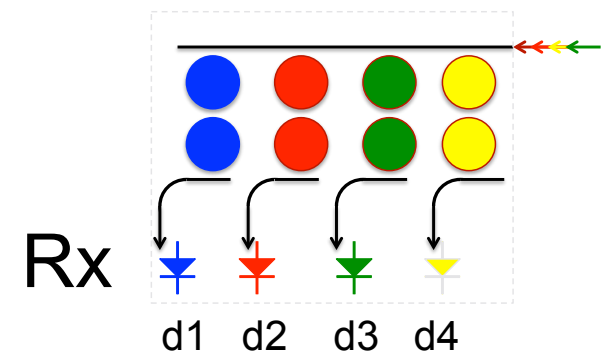


Approaches to short reach optical interconnects → 400 Gb/s to 1 Tb/s

- Most current approaches use parallel fibers at 100 Gb/s and above
 - Higher cost for fiber
 - Lower density
- Some CWDM solutions 4 x 25 Gb/s @ 100 Gb/s



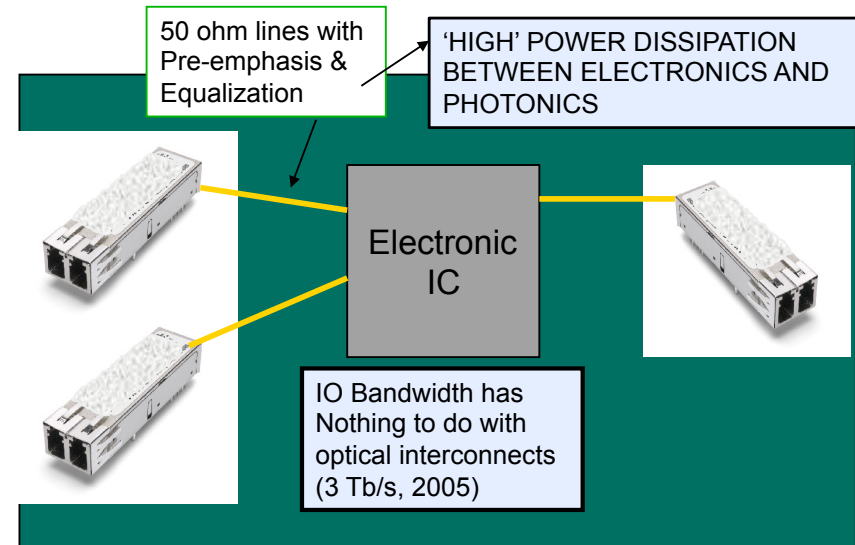
- **Dense wavelength division multiplexing (DWDM)**
 - Highest density solution
 - Need resonant wavelength stability in silicon micro-rings



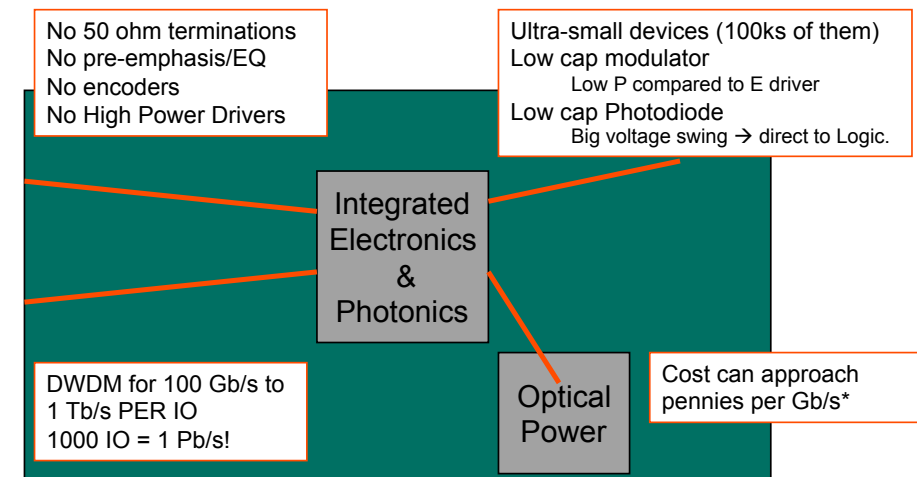
Optical Interconnects

- Evolutionary (Modules)
 - GbE and 10GbE Products
 - 100 GbE modules soon w/ VCSELs and Si Photonics
 - TbE modules on the horizon

- Revolutionary (3DI)
 - Higher bandwidth density
 - **DWDM is required!!**
 - Drastic *potential* power reduction
 - No 50 Ω lines, pre-emphasis or equalization
 - Receiver has high transimpedance, few gain stages
 - Shared CDR (less delay variation and jitter)



OPTICS FOR DISTANCE



OPTICS FOR LOW POWER, HIGH BANDWIDTH DENSITY, COST, SIZE, WEIGHT, DISTANCE

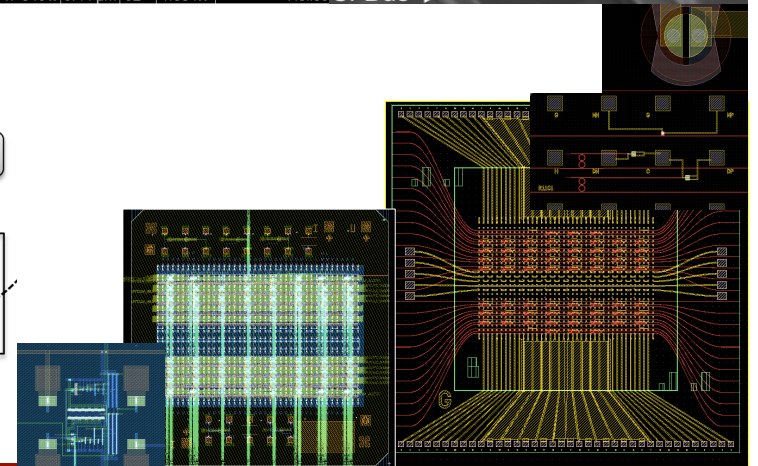
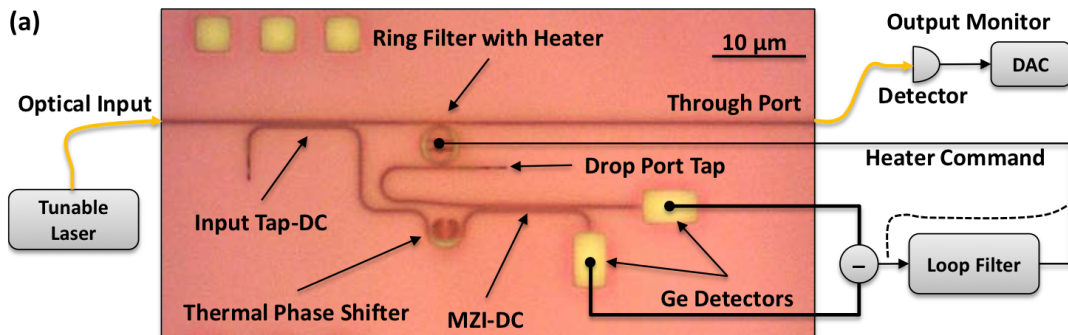
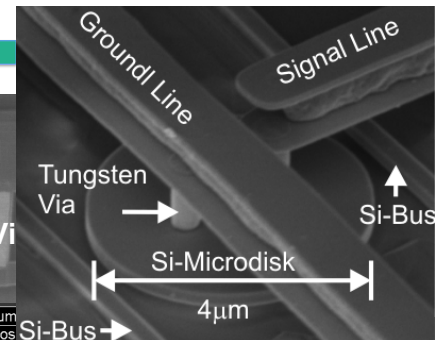
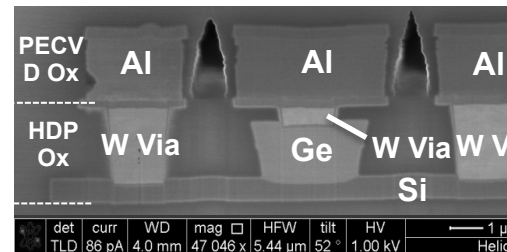
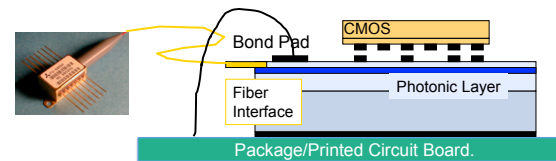
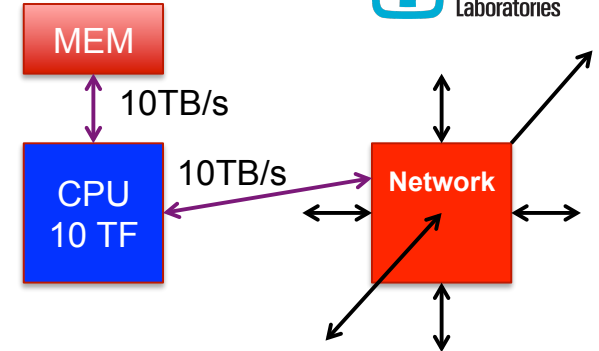
A new approach to high performance computing

- **Instead of ... Evolutionary architecture approach:**

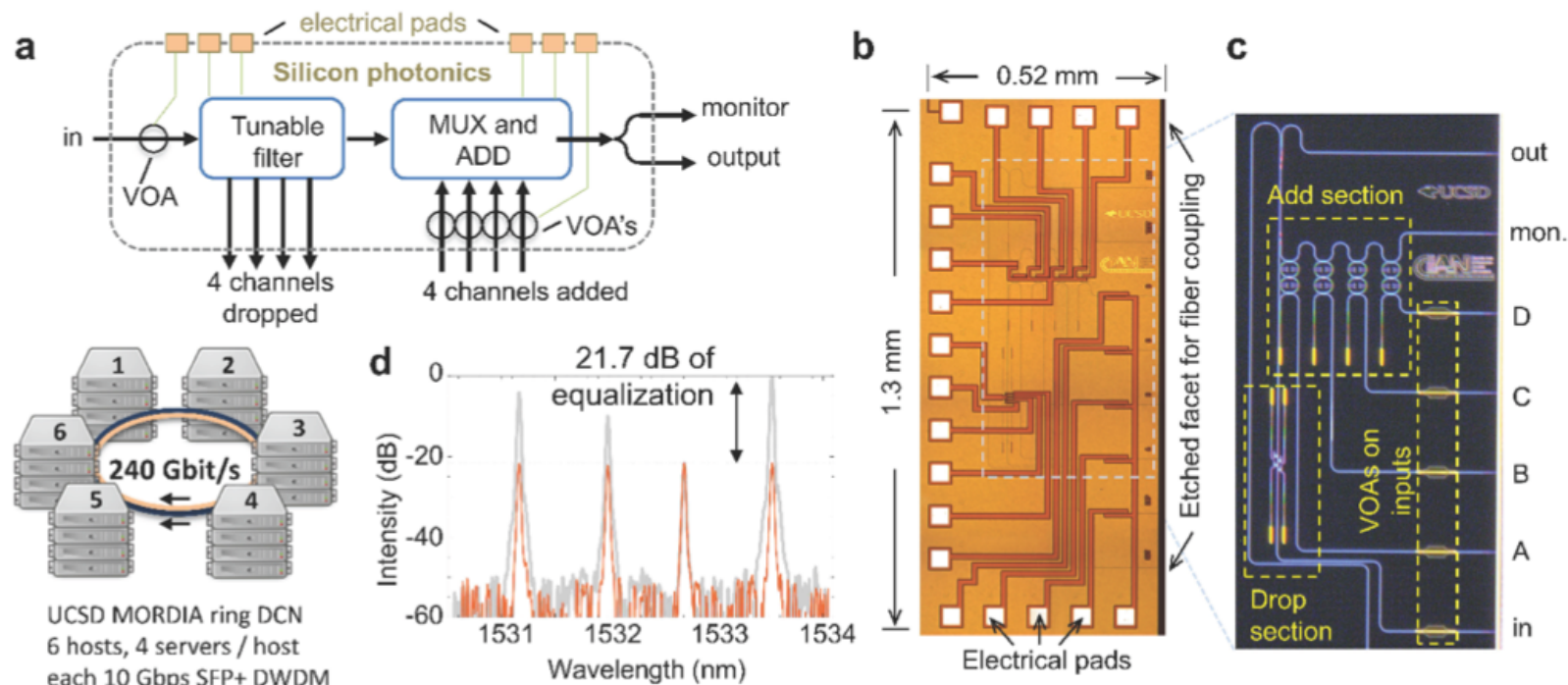
- Design around limited (network and memory) interconnect bandwidth ($\ll 1$ bit per second/flop)

- **Pursue ... Revolutionary approach:**

- Small silicon micro-photonic devices intimately integrated with network and processor ICs
 - Chip-scale 100s Tbps IO
 - <100 femtojoule/bit $\rightarrow <10$ sW IO



DWDM Networks for data centers

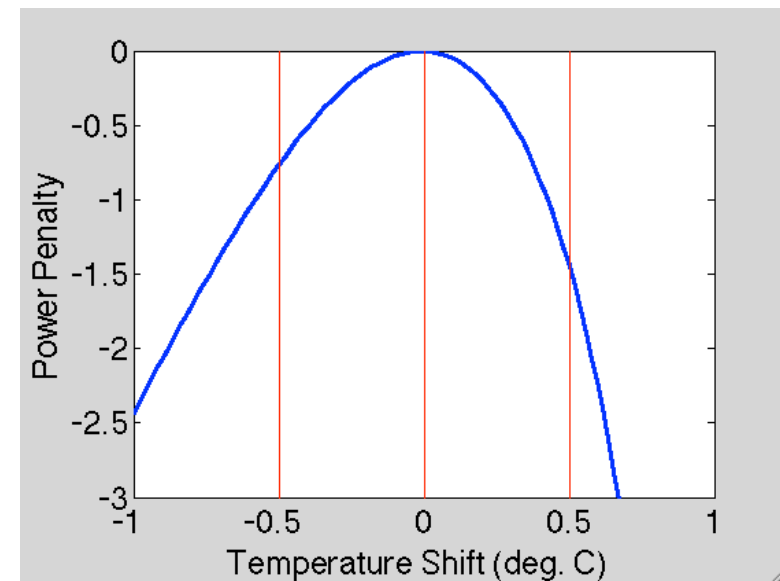
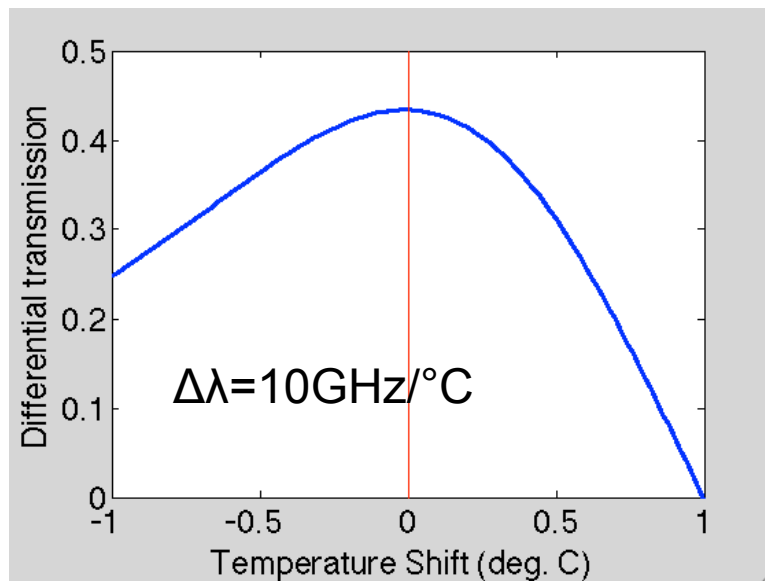
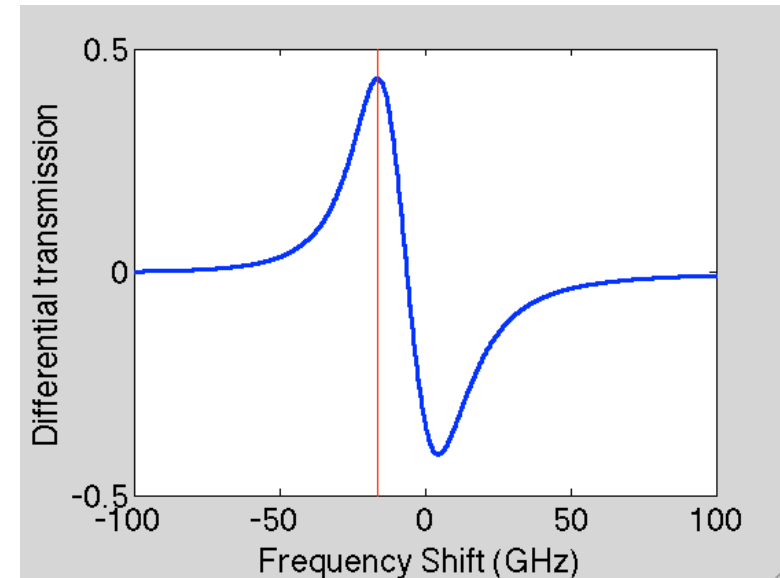
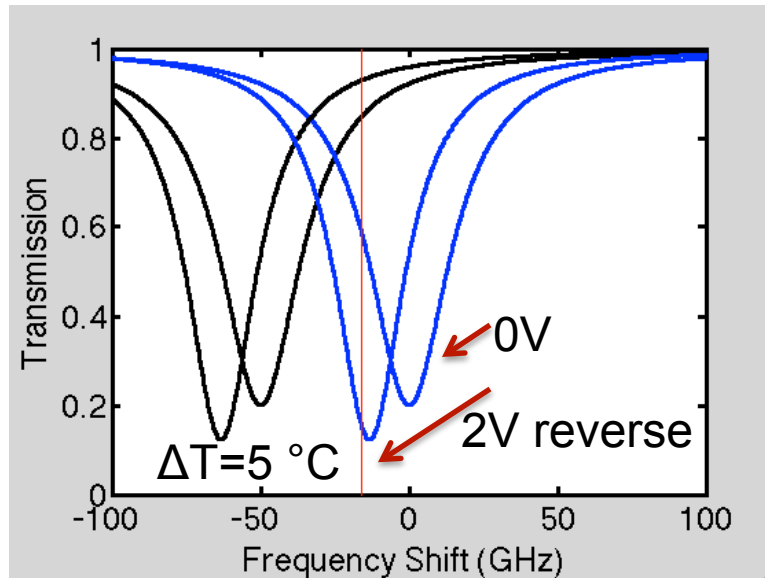


Ryan Aguinaldo et. al., 2014 IEEE IPC Post-deadline paper
(UCSD & Sandia collaboration)

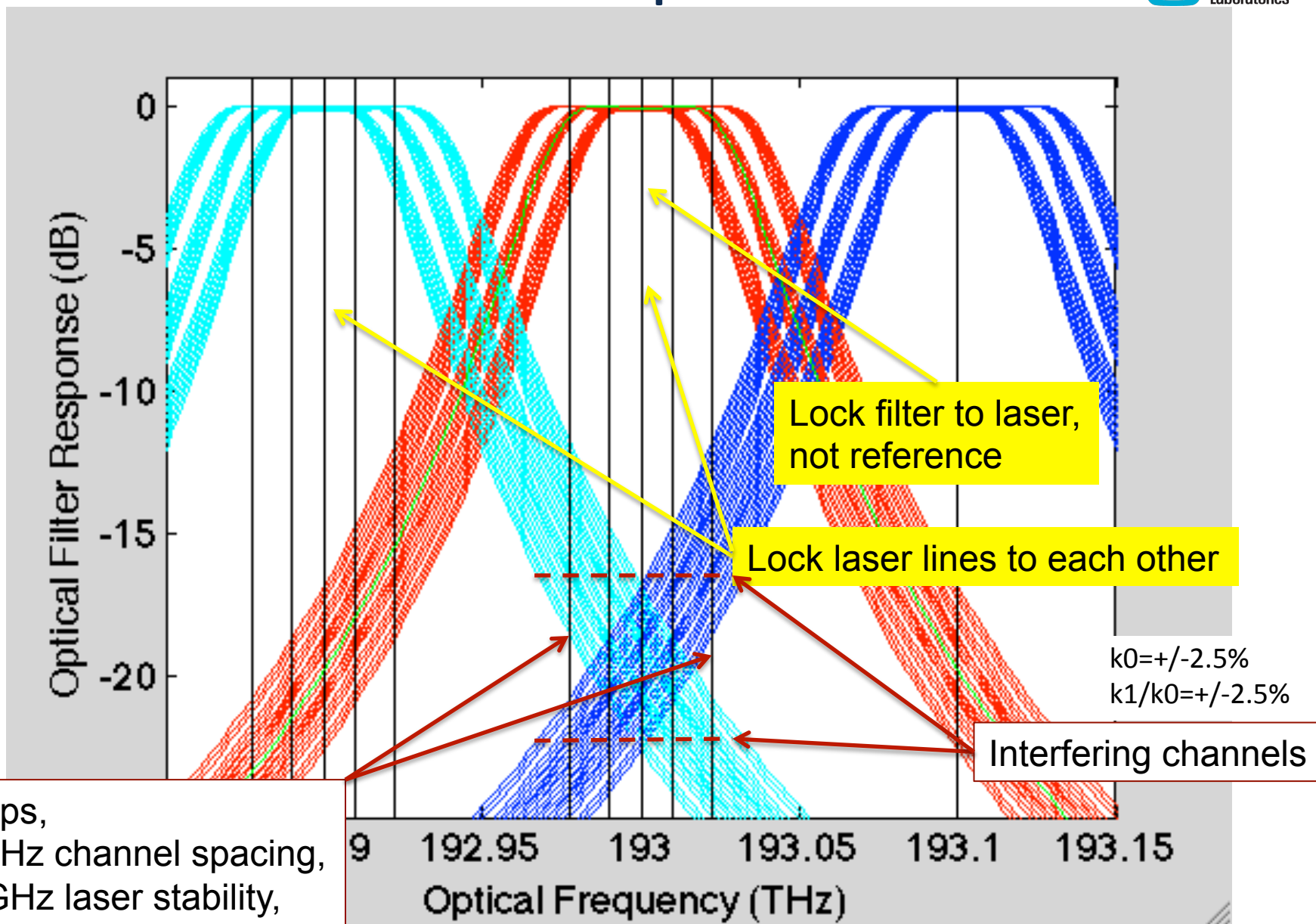
- DWDM networks lead to lower SWaP-c and enhanced functionality compared to multiple fiber networks

Requirements for wavelength locking

Effect of temperature on loss budget

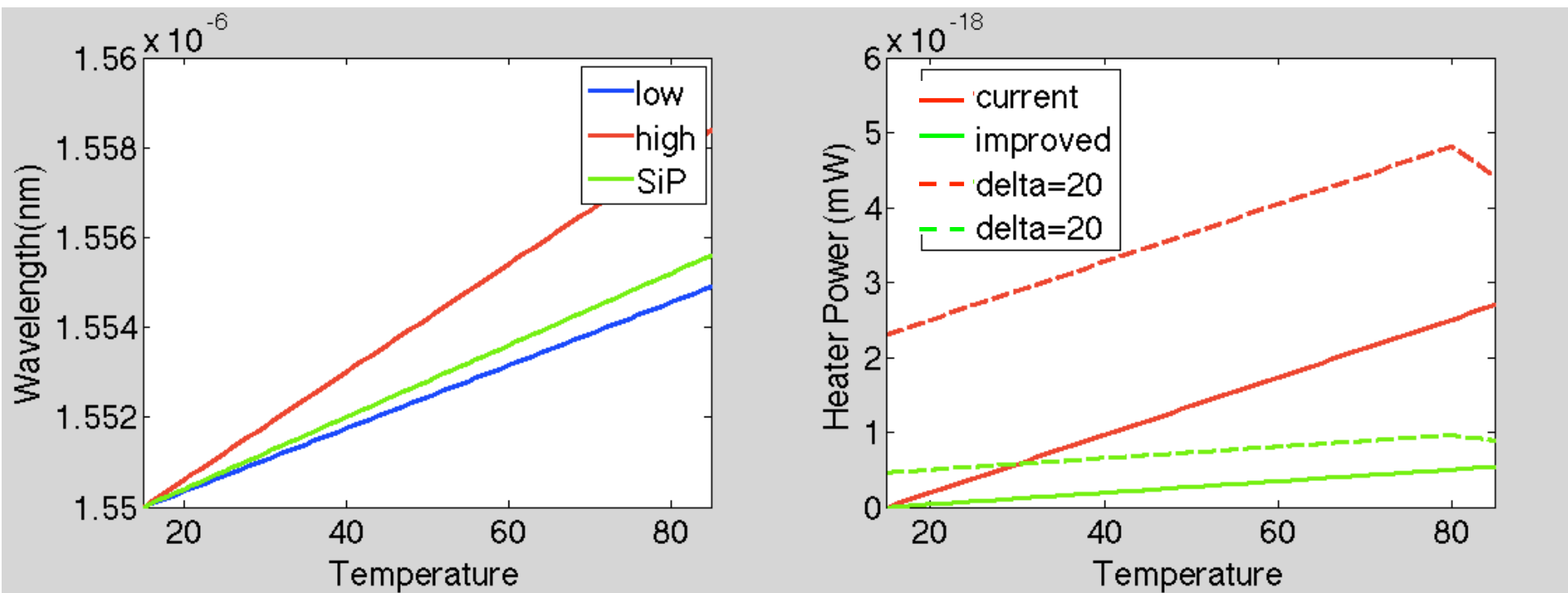


Filter allowable temperature drift.



λ Stability: Differential temperature differences

- Should we let the laser wavelength drift with temperature?
 - Range requirements 0 – 85 °C
 - CWDM lasers (up to 10% efficient (0.7 – 1.2 nm/ °C) SiP ~ 0.8 nm/°C)
 - Lock laser to resonator (Oracle 2.5% - 5% efficient)

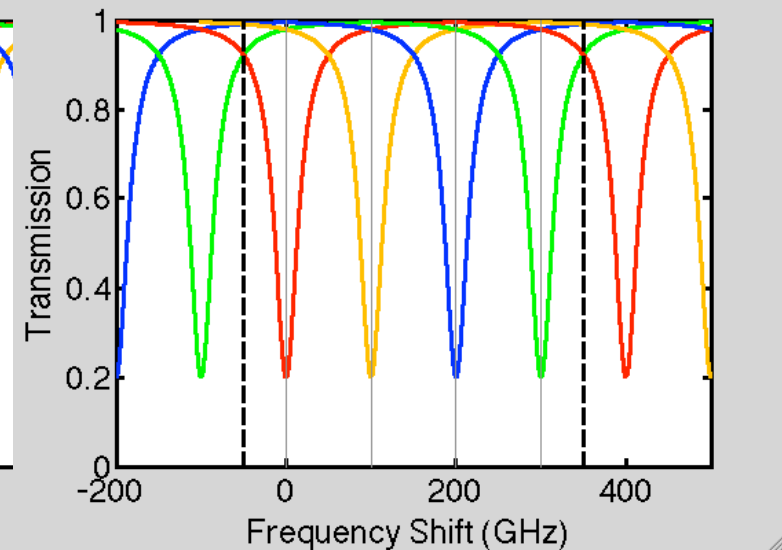
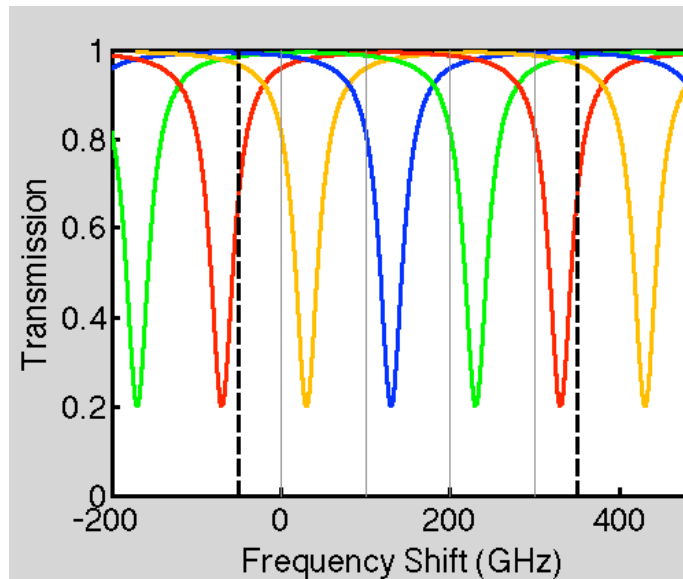
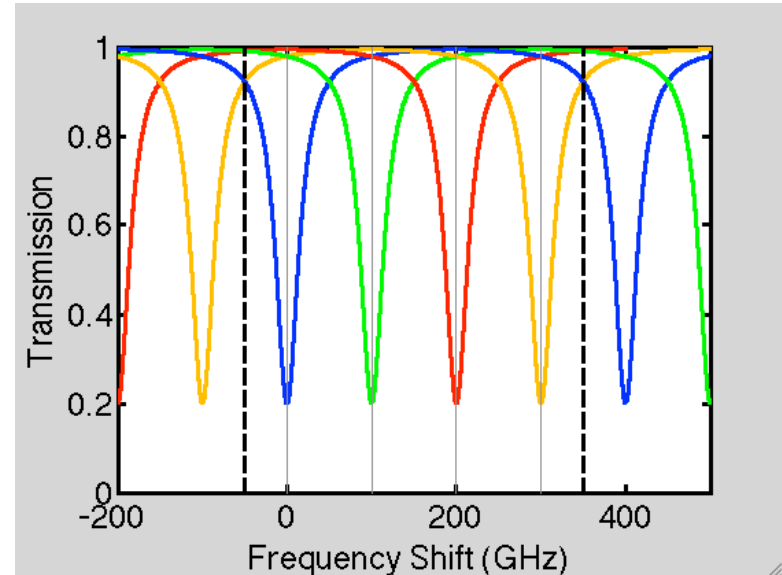


Cyclical Channels

Example: $4 \times 100\text{GHz}$ channel spacing

- a) Designed alignment
- b) 13°C heating – 130 GHz shift
- c) 7°C controlled heating to 200 GHz shift

Maximum heating = channel spacing / df/dT :
 $100\text{GHz}/10\text{GHz}/^\circ\text{C} = 10^\circ\text{C}$



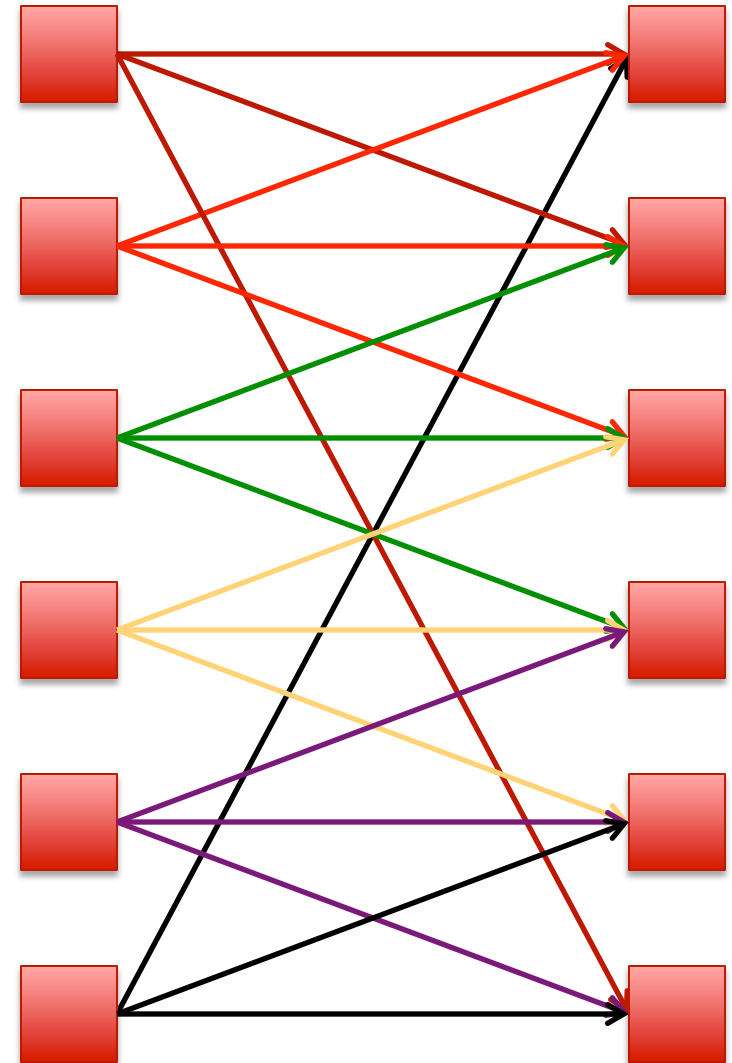
N. Binkert et al.,
ISCA 2011;

M. Gorgas et. al.,
IEEE CICC, 2011

A. Krishnamoorthy et. al.,
IEEE Photonics J., 2011

Circuit for DWDM channel alignment

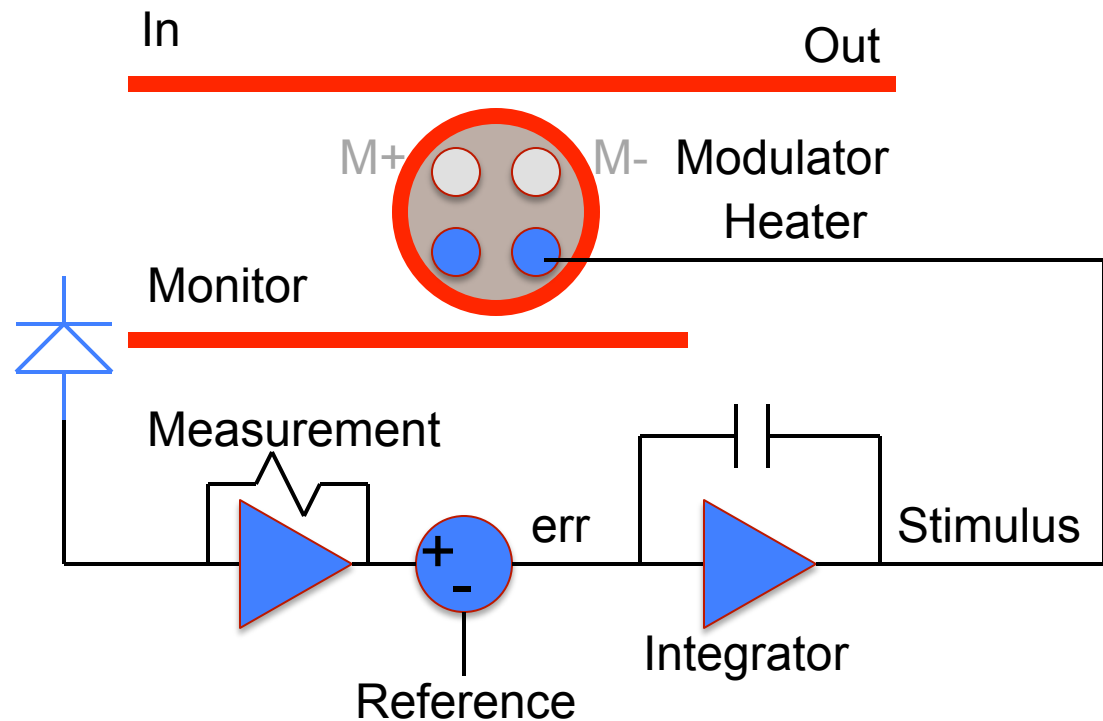
- MOSIS: Ring Oscillator 1.21 nW/MHz/gate $\rightarrow$ 0.3 fJ/bit (45 nm)
- Inverter, $I = 0.25$ fJ/bit (1 fF/1V)
- Logic Gate, $L = 0.5$ fJ/bit (2 fF/1V)
- Mux, $M = (S_c - 1) * L$; $S_c = S \uparrow$ power of 2
- Register, $R = 10 * L = 5$ fJ/bit
- Buffer fan-out, $F = S * I$
- Back of envelope example: $N=40$, $S=6$
 - 2N registers (number of channels)
 - $80 * 5 \text{ fJ/bit} = 400 \text{ fJ/'word'}$
 - Fan out of S
 - $40 * 6 * 0.25 \text{ fJ/bit} = 60 \text{ fJ/'word'}$
 - N S:1 multiplexers
 - $40 * (7) * 0.5 \text{ fJ/bit} = 140 \text{ fJ/'word'}$
 - Sum = 600 fJ/'word' = **15 fJ/bit**
 - SLOW circuitry
 - Control of the shifter
 - Extra laser channel



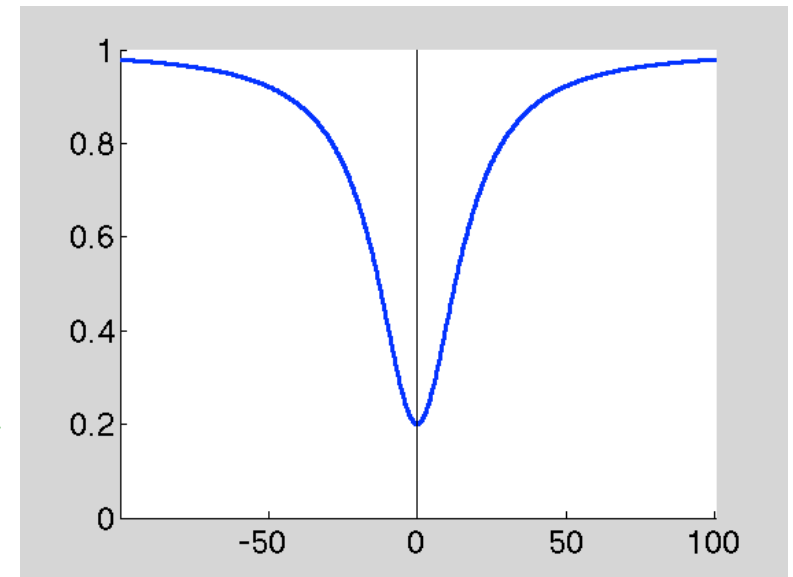
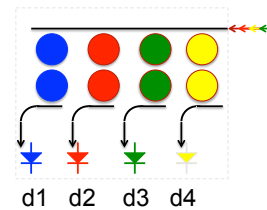
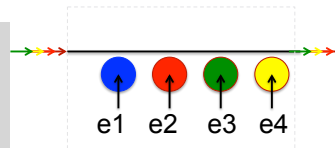
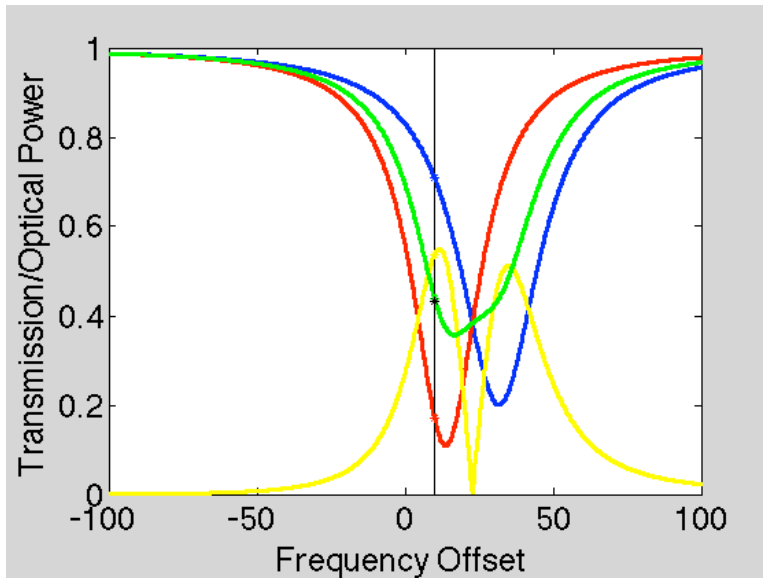
Resonant Wavelength Closed Loop Control

■ Control Loop

- Measurement
 - Temperature
 - Power (shown)
 - Phase (BHD, PDH)
 - Bit errors
- Integration (PI Loop)
- Stimulus
 - Integral Heater (shown)
 - Forward bias (heater/carriers)
 - Reverse bias (carriers)



Resonant Wavelength Locking



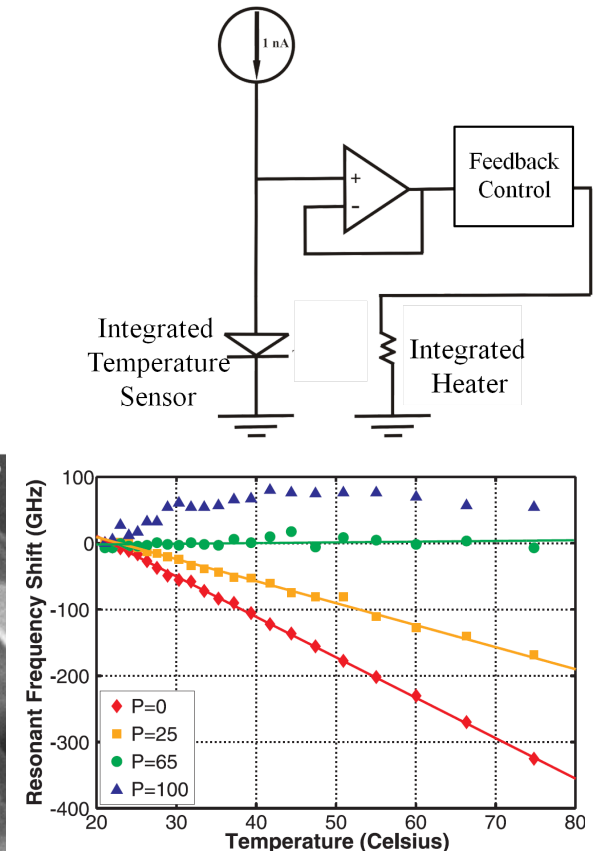
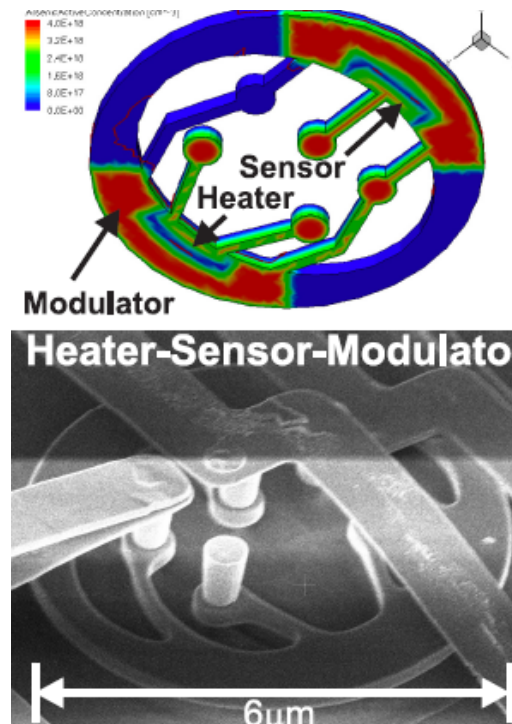
■ Lock on side of resonance

■ Lock at minimum power

Previous Methods

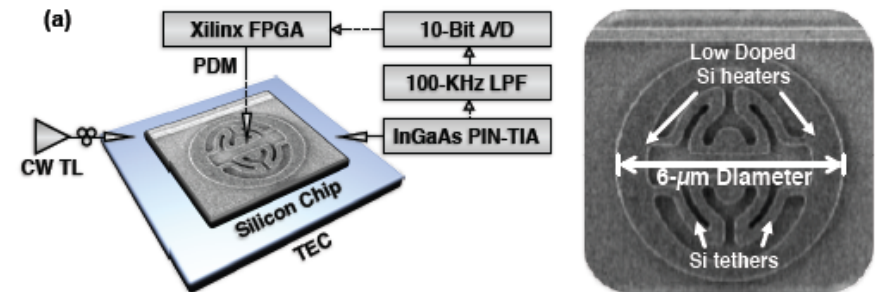
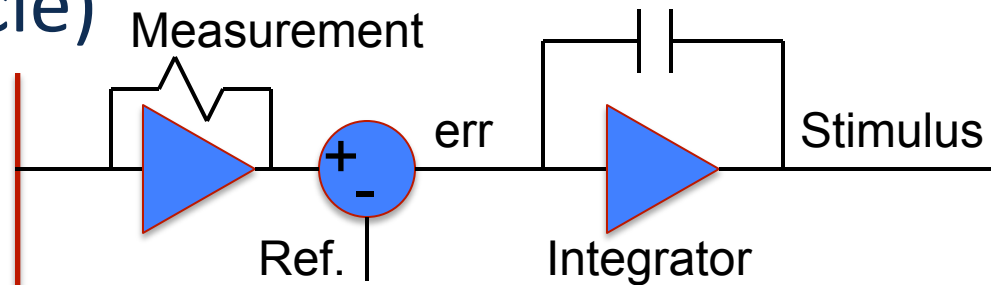
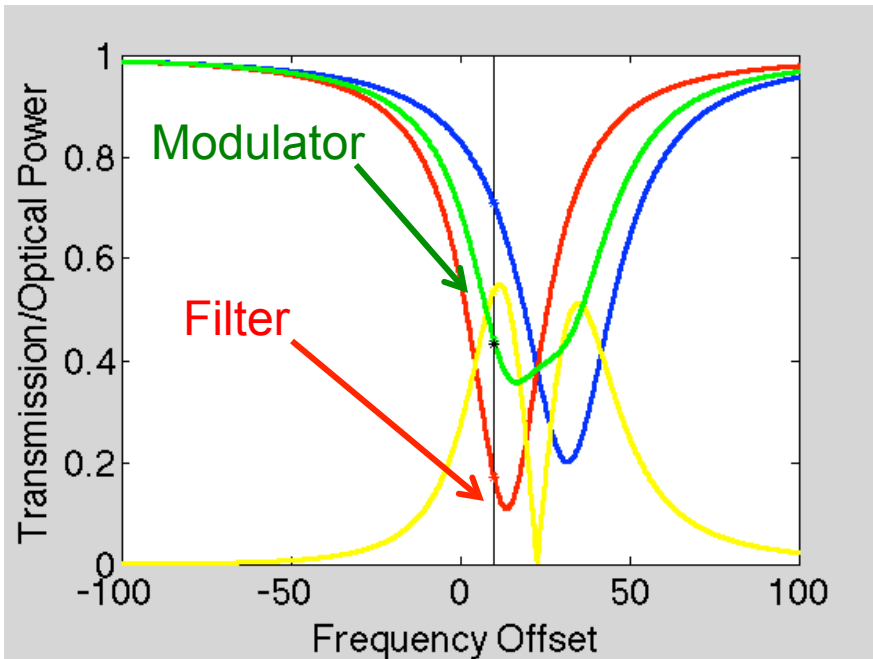
Temperature Sensor (Sandia)

- First attempt at resonant wavelength control
- Integral temperature sensors (diode)
- Sensor not independent of background temperature
- More complex device
- Not measuring other wavelength shifting affects
- Simple electronics (PI loop with $P=k$, $I=0$)

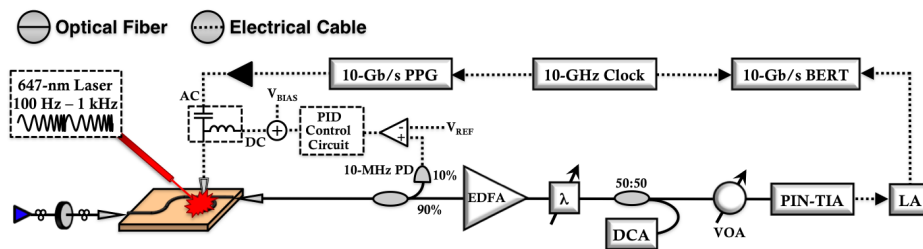


C. T. DeRose, et. al., CLEO 2011

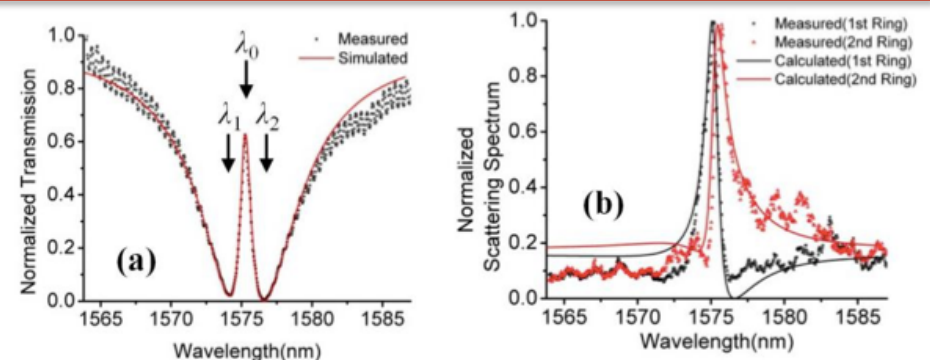
Locking using Power Sensors (MIT, Columbia, Rice, Oracle)



Resonator with heater, without sensor
(Timurdogan et. al., CLEO 2012)



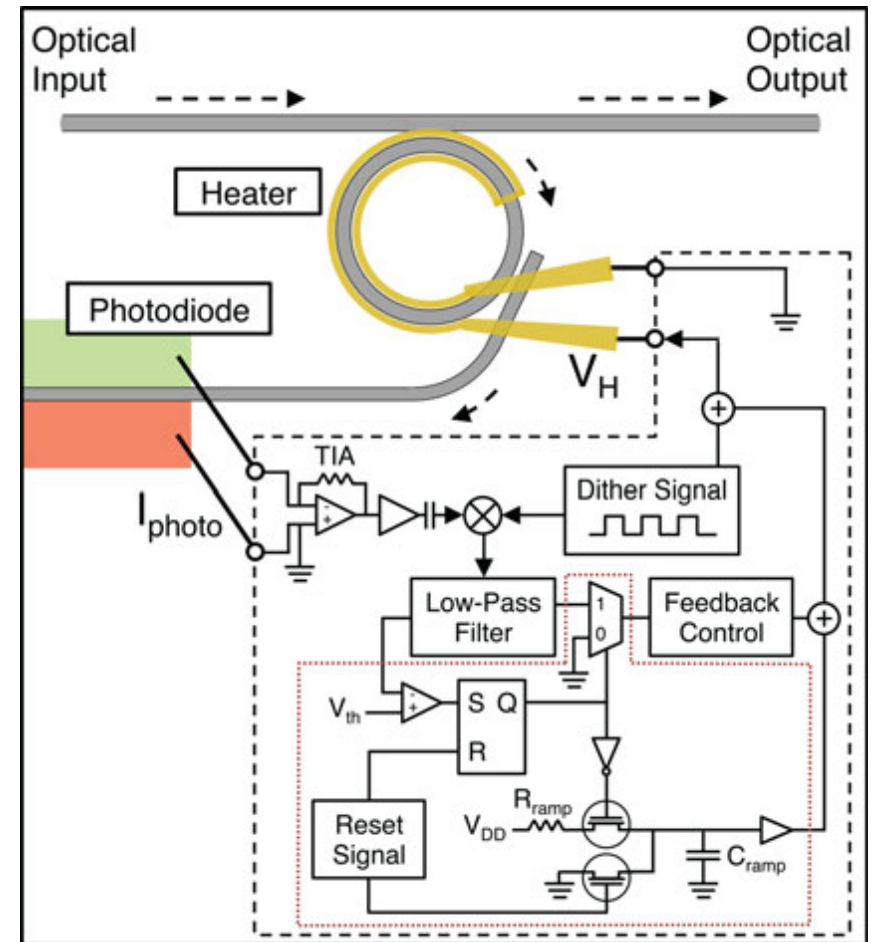
Modulator with bias induced temperature change (Padmaraju, OFC 2012)



Scattering from a dual-ring modulator
(Qui et. al. Opt. Exp., 2011)

Locking using a dither signal (Columbia)

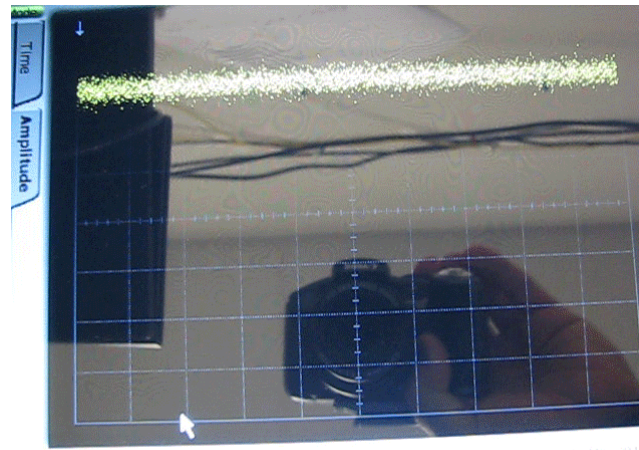
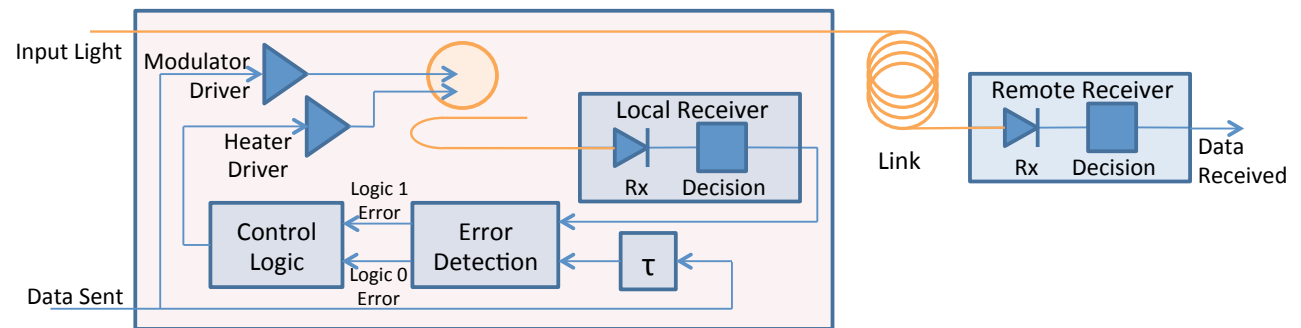
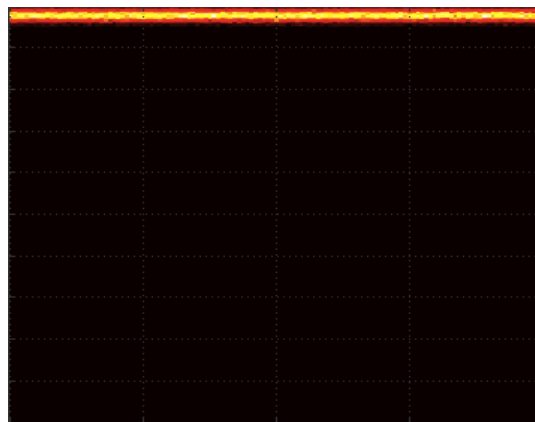
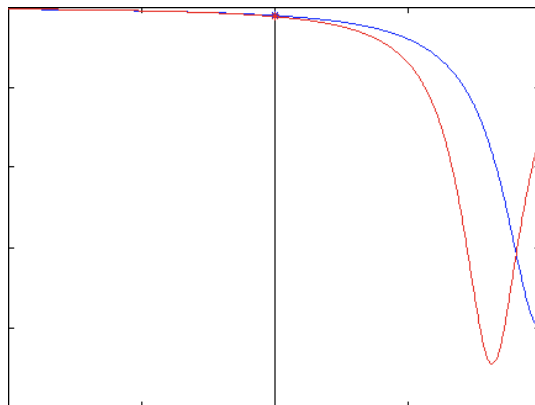
- Creates a signal that is anti-symmetric (lock at zero)
- More complex electrically
- Simple optically
- Some small degradation in the optical performance with dither
- Best for filter locking



K. Padmaraju, et. al. JLT 32 (3) (2014)

Modulator wavelength stabilization using bit errors (Sandia)

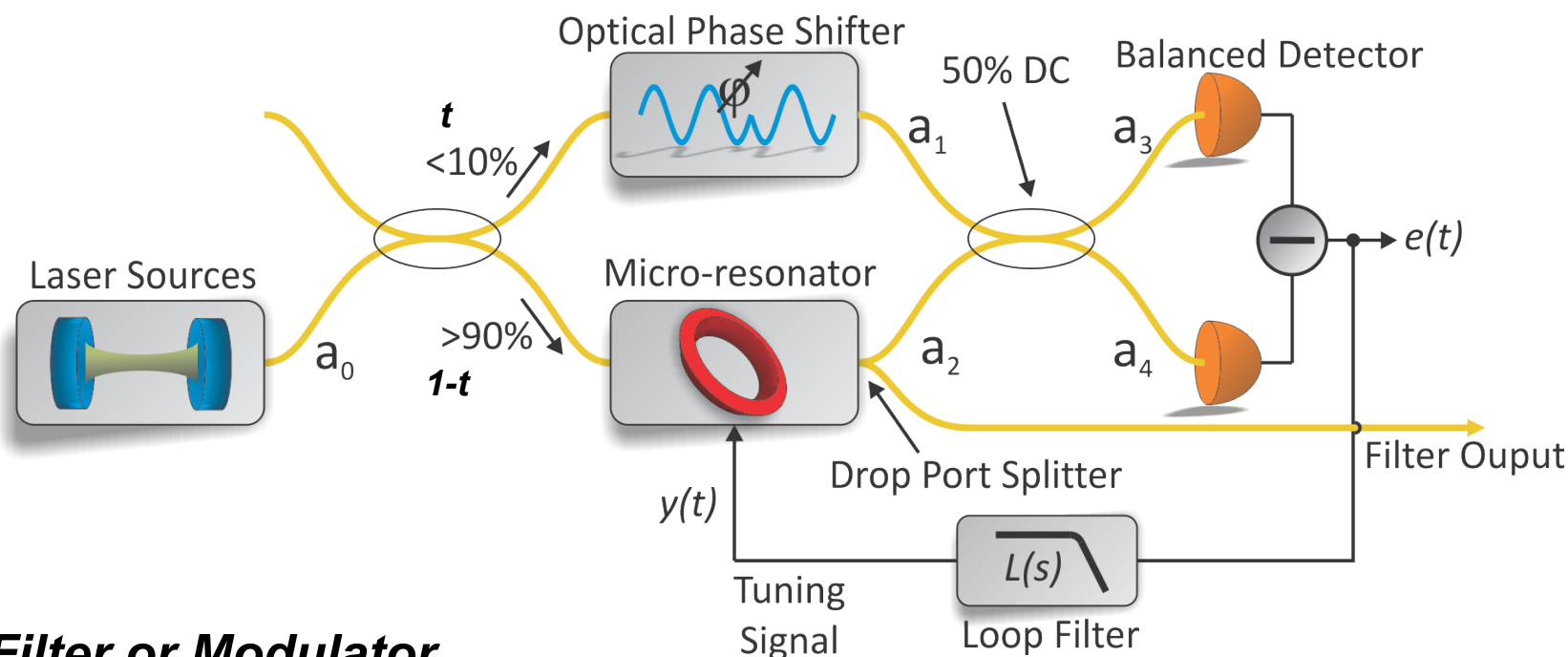
- Direct measurement of the bit errors
- Requires high speed circuitry
- Most compact solution (no low pass filtering)



W. A. Zortman et. al.,
IEEE Micro (2012)

Balanced Homodyne Detection

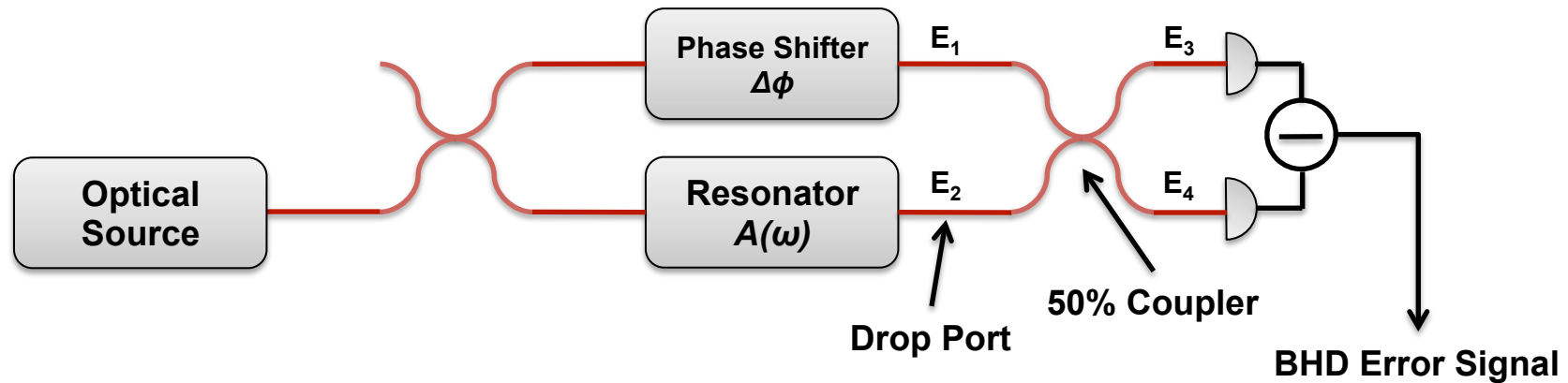
Balanced Homodyne Detection



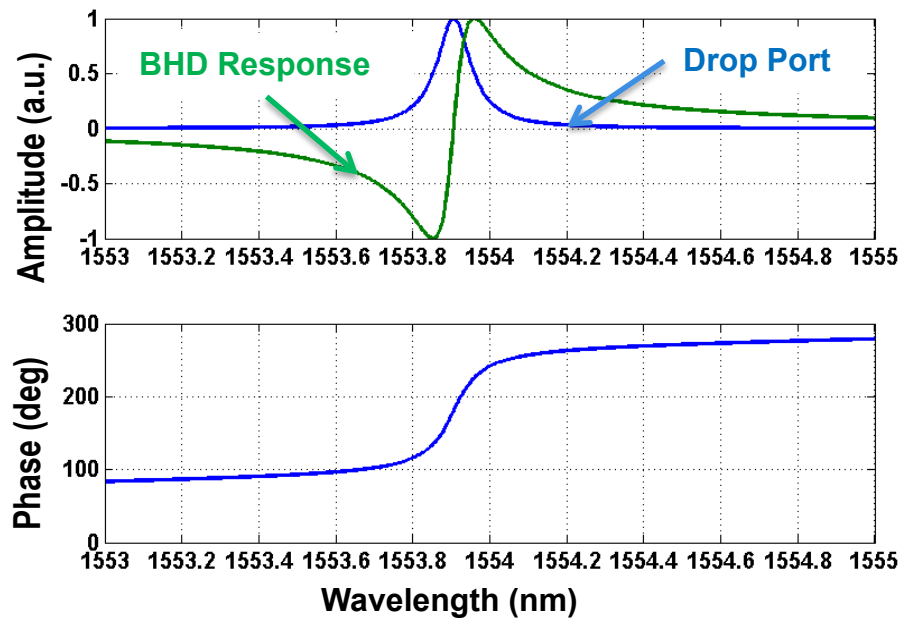
- **Filter or Modulator**
- **Lock to zero:** No calibration or reference level needed for locking
- **Amplitude insensitive:** Locking point not influenced by optical intensity
- **Precision locking:** Resonator is not disturbed
- **Minimum circuit complexity:** Power and area consumption of control electronics is minimized

J.A. Cox, A.L. Lentine, D.C. Trotter and A.L. Starbuck, "Control of integrated micro-resonator wavelength via balanced homodyne locking," *Opt. Express* Vol. 22(9) (2014)

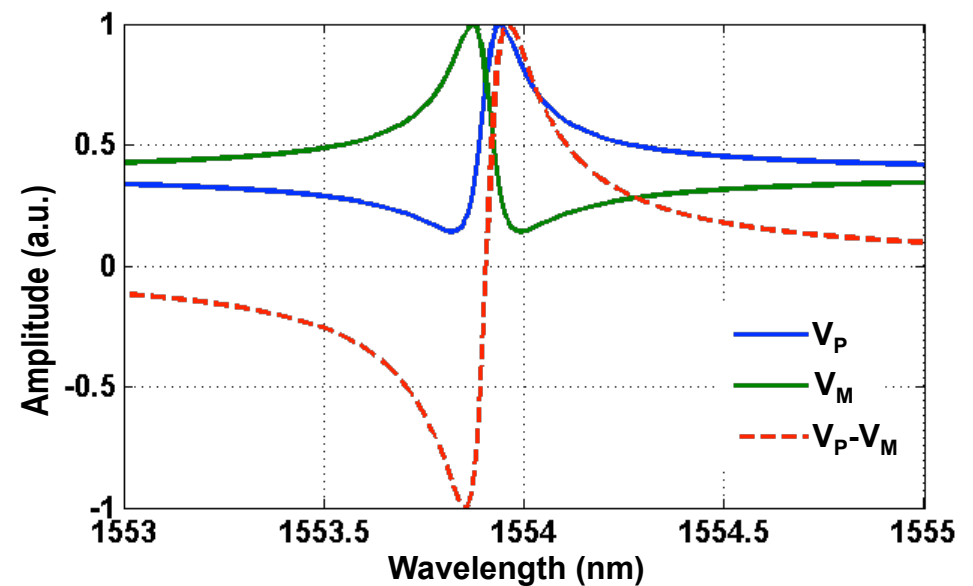
BHD Transfer Function



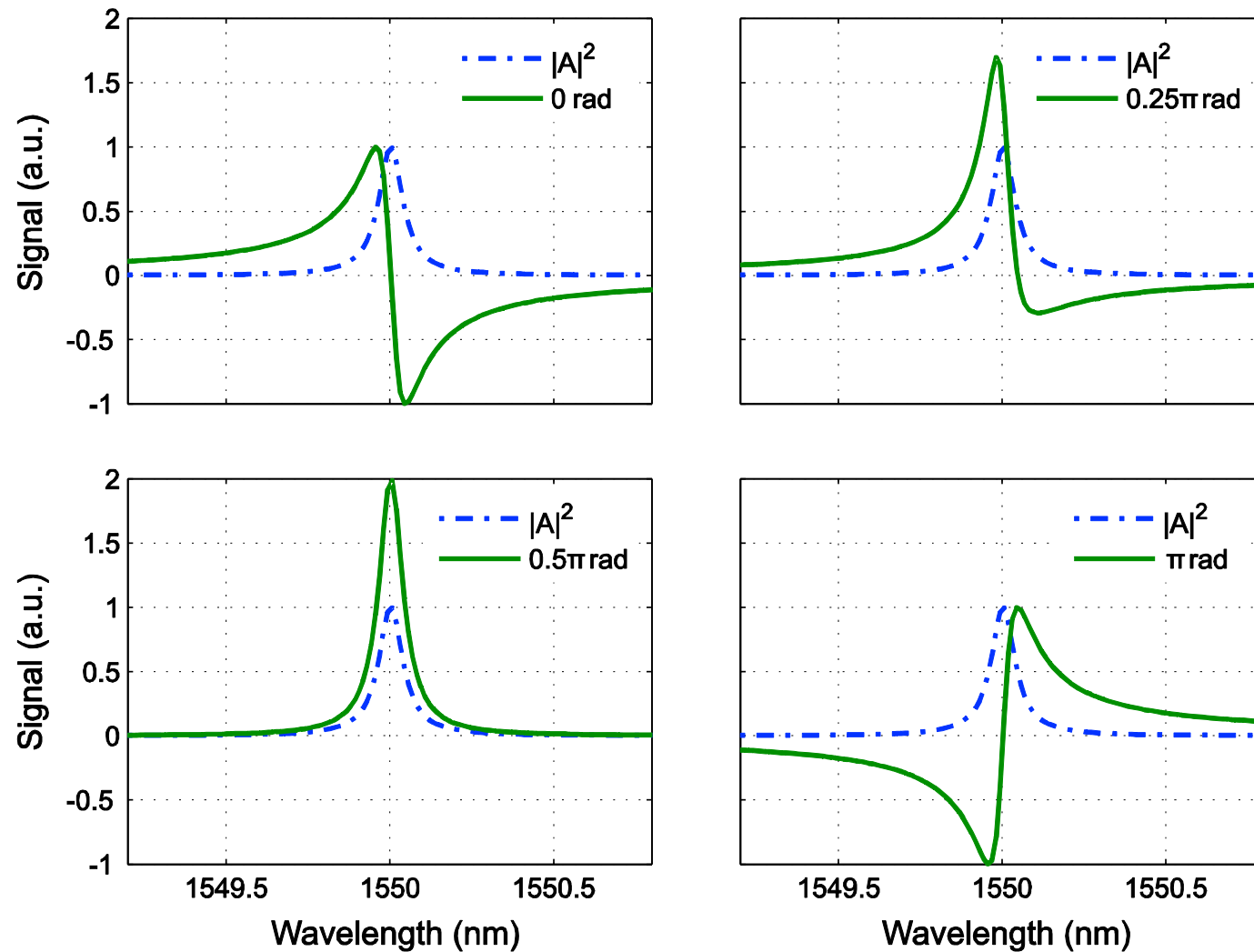
Ideal Response of 1st Order BHD



Positive and Negative Photodetector Signals

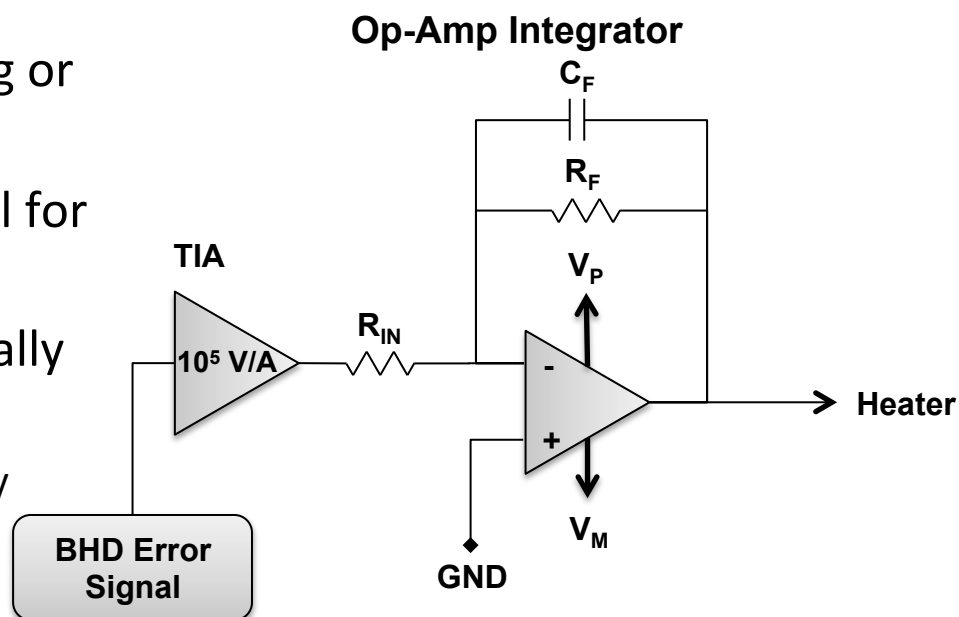
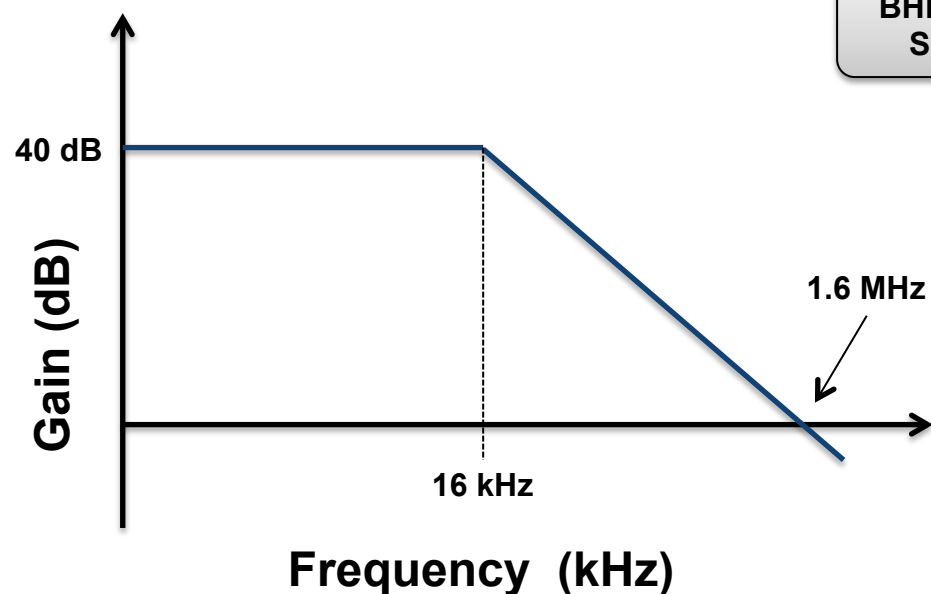


Effect of Phase Imbalance



Control Loop

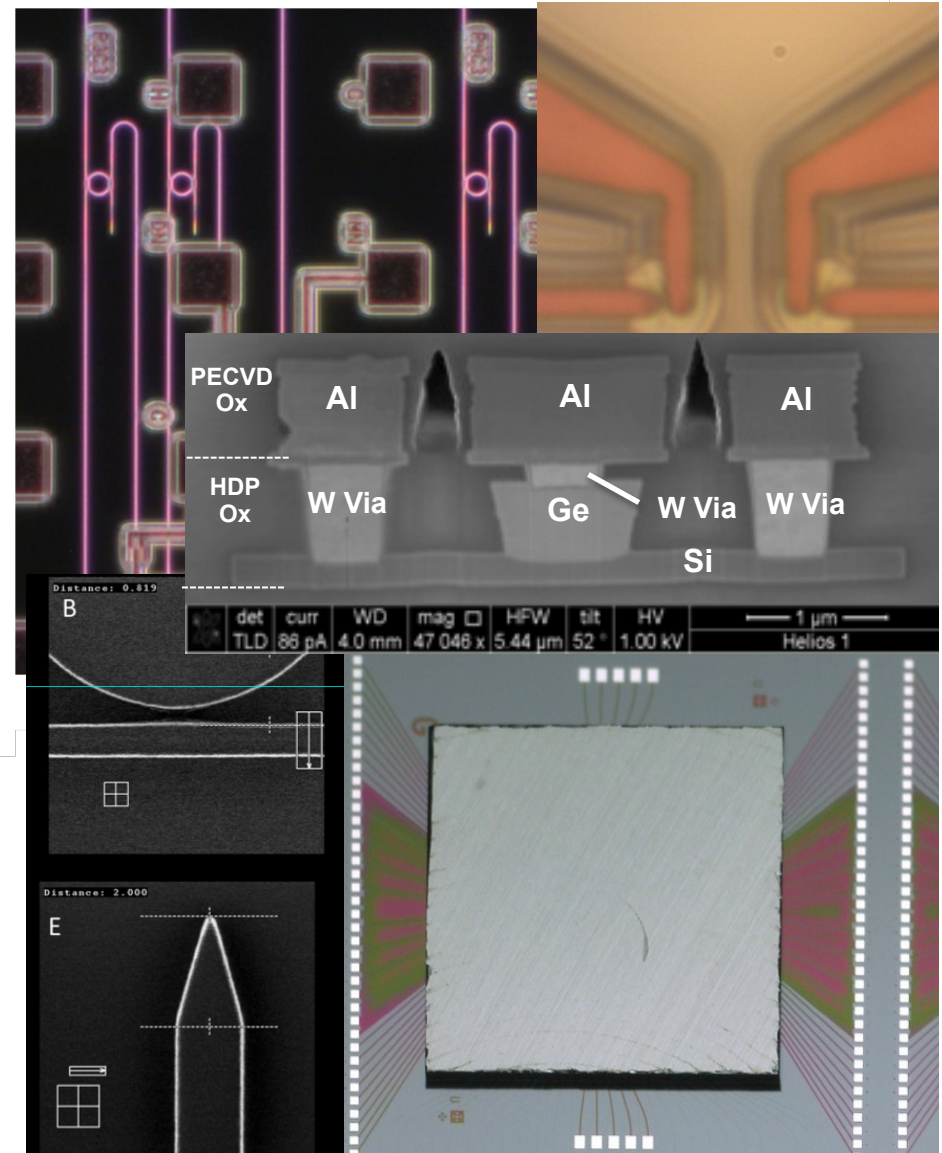
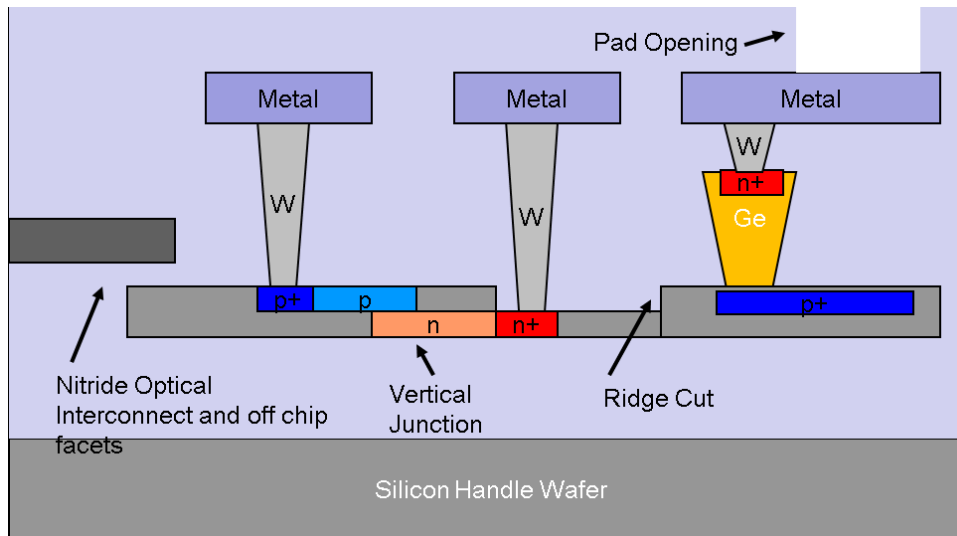
- Simplest possible circuit for analog or digital implementation on-chip
- Smallest component values critical for analog design on ASIC
- Dual voltage operation automatically provides inverted feedback
 - Loop stable regardless of BHD polarity



Element	Value
C_F	10 pF
R_F	1 M Ω
R_{IN}	10 k Ω

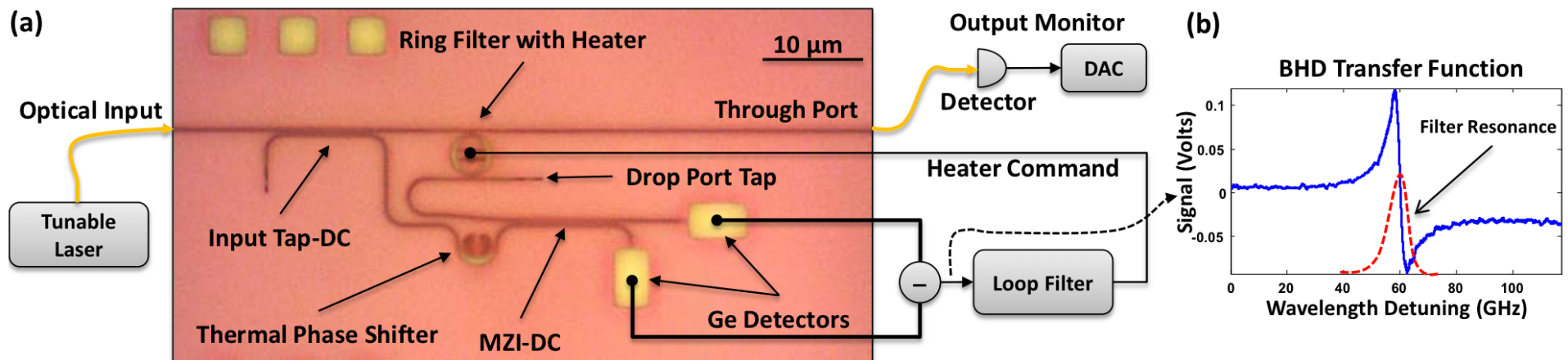
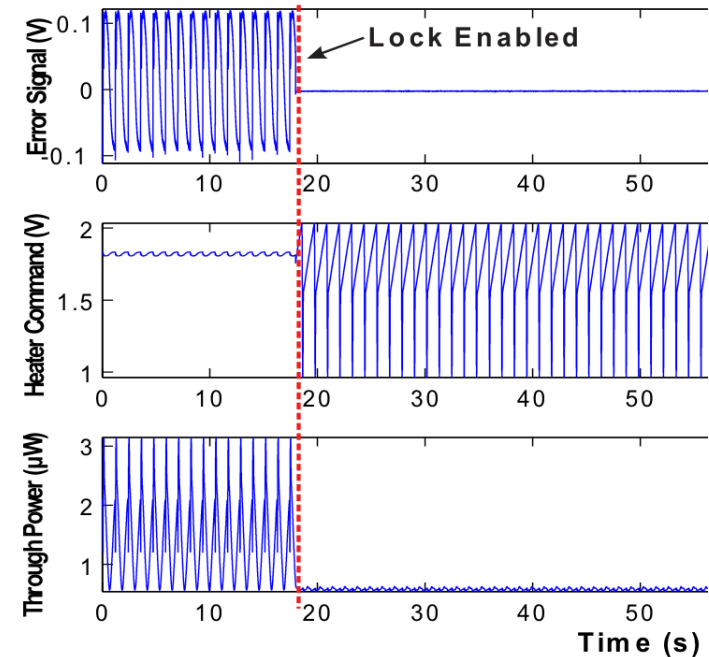
Sandia's Silicon Photonics Process

- Low energy modulators
- Fast (45 GHz) detectors
- Compact switch elements
- Wavelength tunable devices
- Si, Si ridge, SiN guides



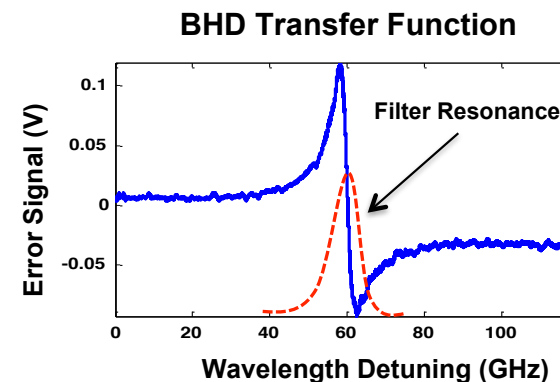
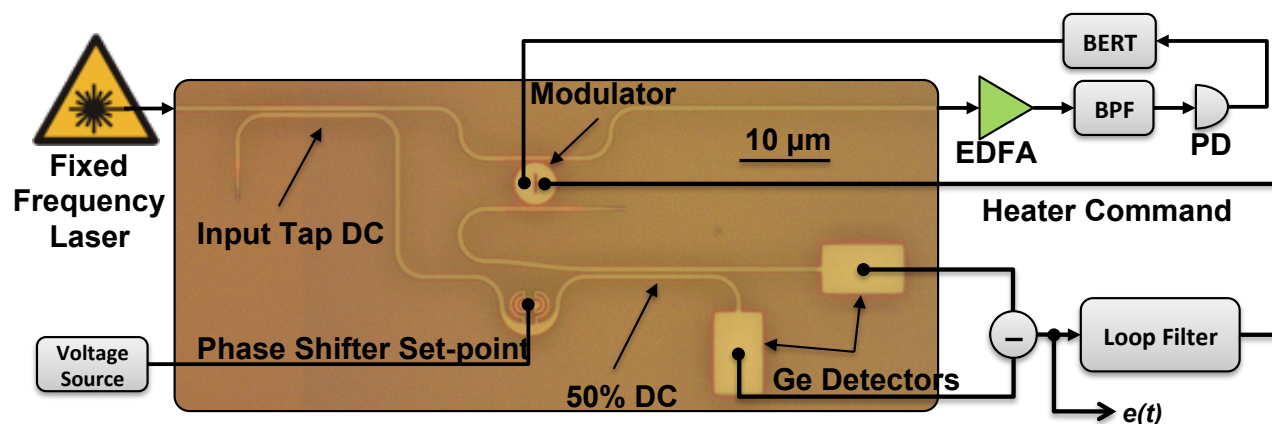
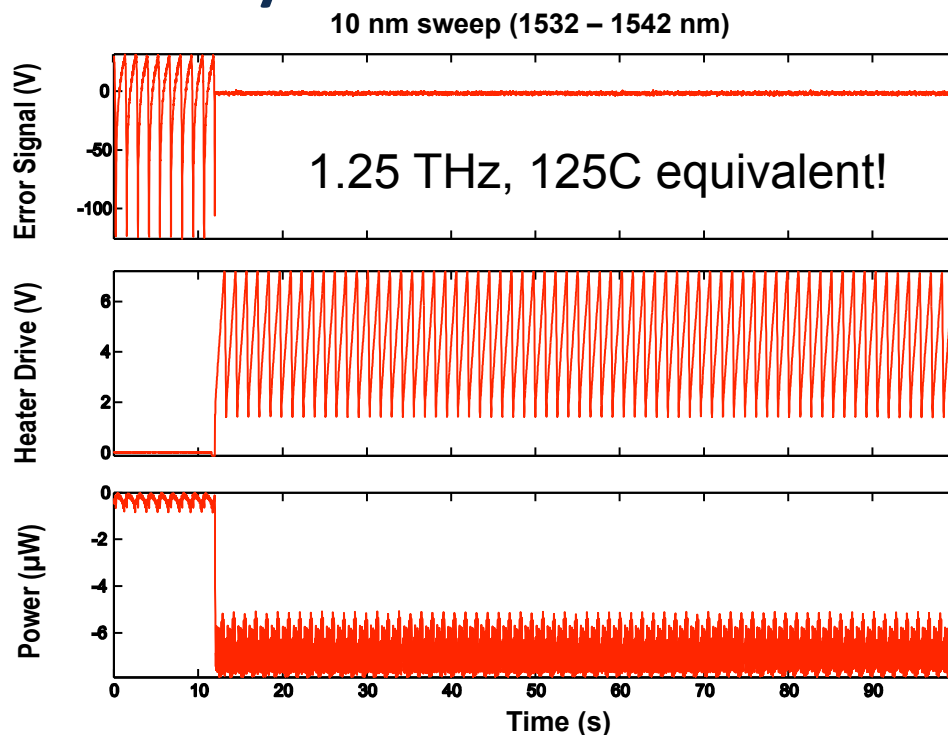
Resonant locking of a DWDM filter

- Problem: locking on minimum power level does not lend itself to a simple control loop
- Solution: Homodyne detection with balanced detection gives optimal locking solution

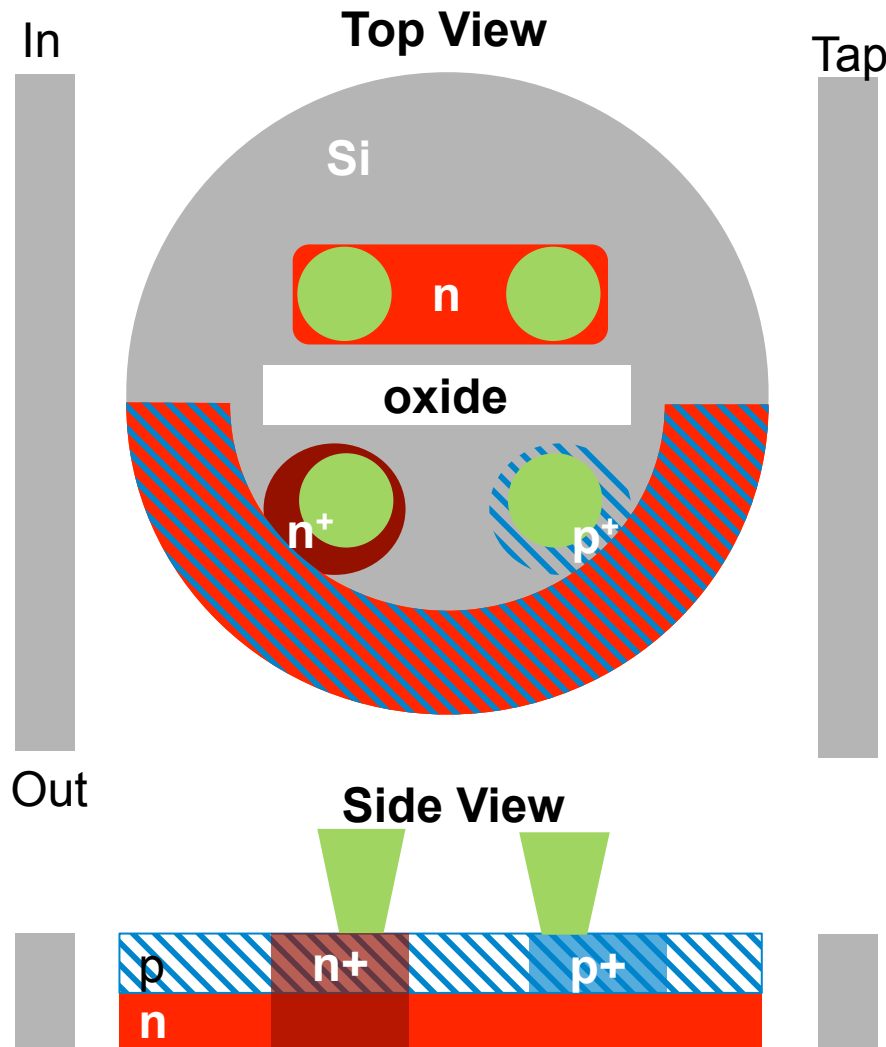


Modulator Stabilization System

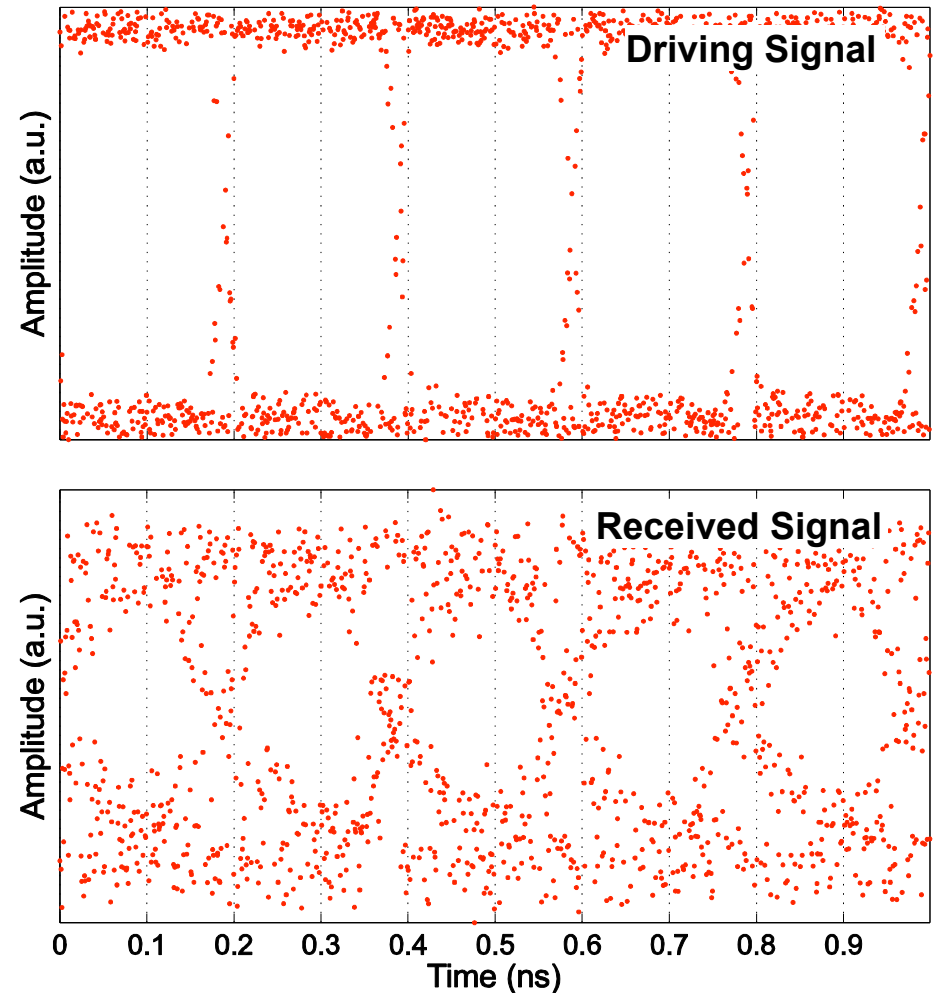
- **Lock to zero:** No calibration or reference level needed for locking
- **Amplitude insensitive:** Locking point not influenced by optical intensity
- **Precision locking:** Resonator is not disturbed
- **Minimum circuit complexity:** Power and area consumption of control electronics is minimized



Modulator Design and Performance



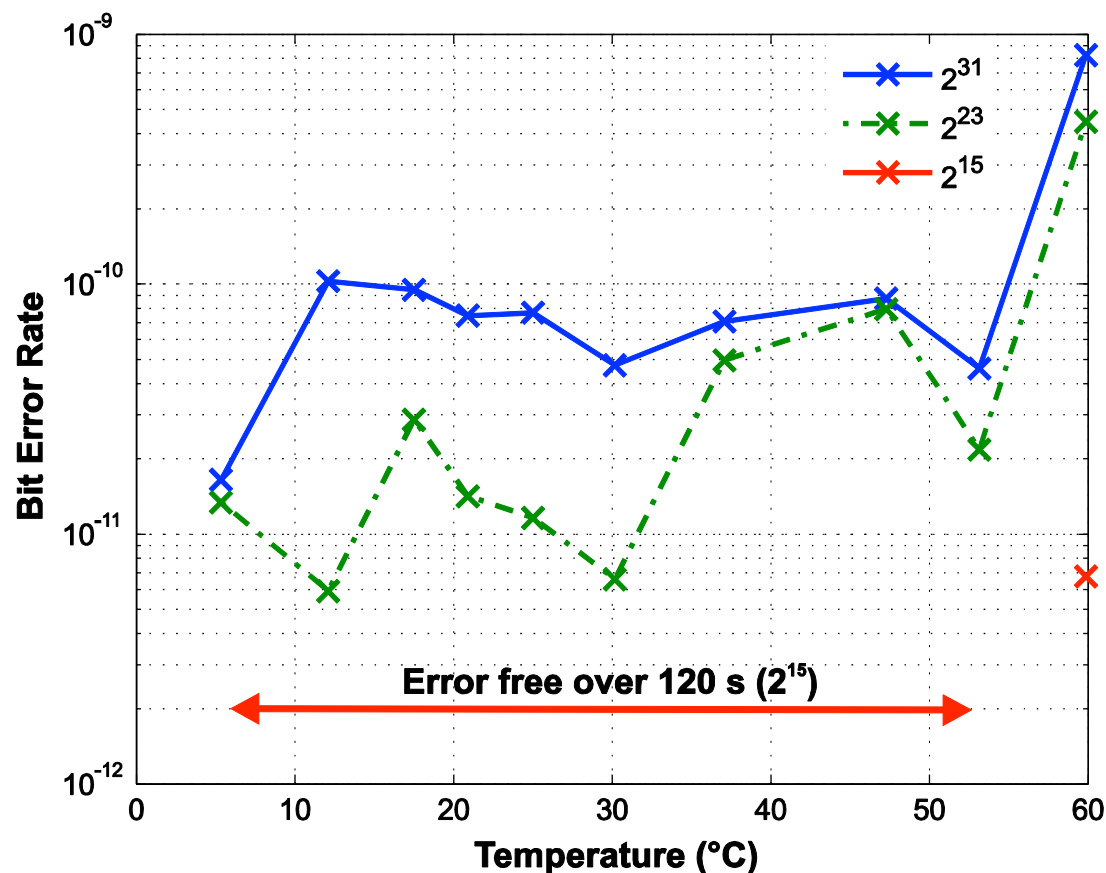
5 Gbit/s Modulation



W. Zortman, A. Lentine, D. Trotter, and M. Watts, "Integrated CMOS Compatible Low Power 10Gbps Silicon Photonic Heater Modulator," in *Optical Fiber Communication Conference, OW41.5*. (2012)

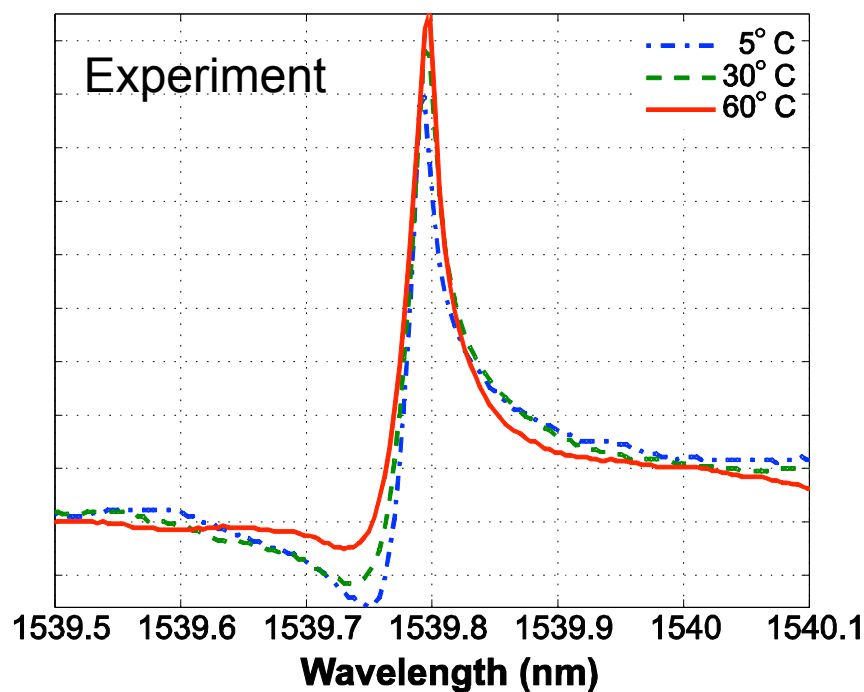
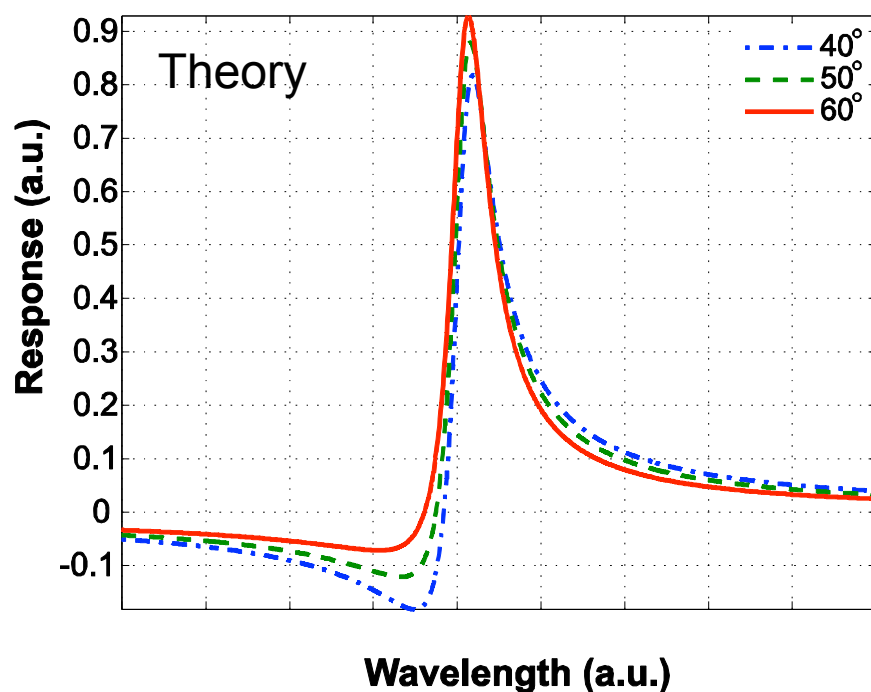
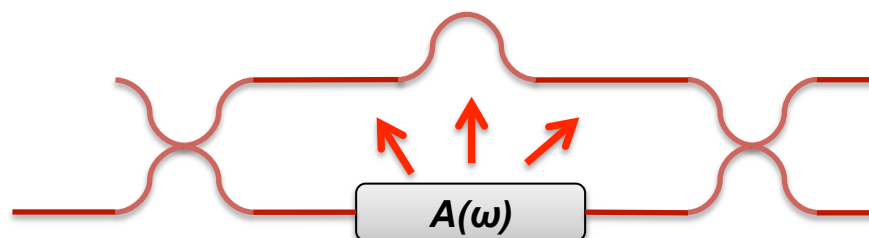
Error Rate vs. Temperature

- 5 GHz modulation applied
- Modulator locked, and phase shifter adjusted **once** for lowest BER.
- **Wavelength held constant. Chip temperature varied from 5—60° C while locked.**
- Error free from 5—55° C (2^{15} -1 bits)
- Error rate rises at 60° C due to thermal phase imbalance in interferometer



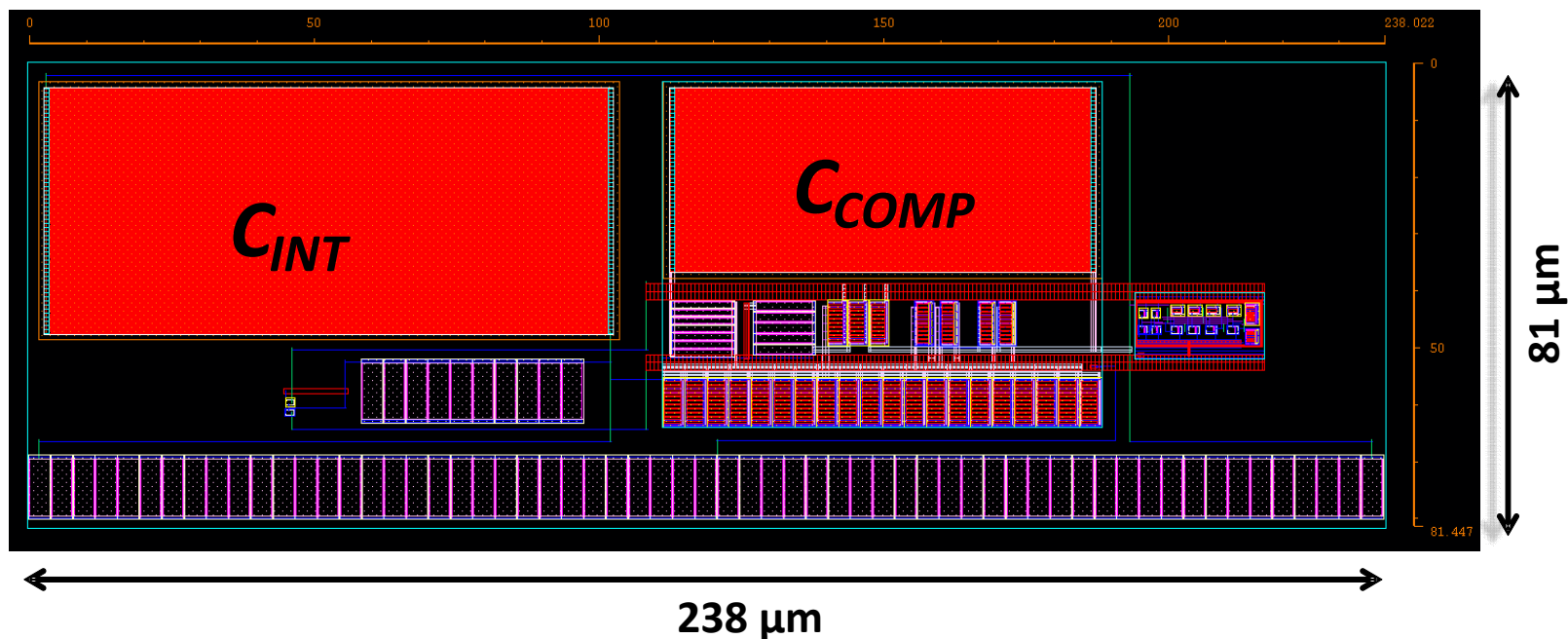
Design Considerations

- **Hypothesis:** Path length imbalance and thermal gradients from modulator heater cause shift in locking point
- **Test:** Vary chip temperature while tuning heater to hold resonant wavelength constant



CMOS ASIC Design (currently in fab)

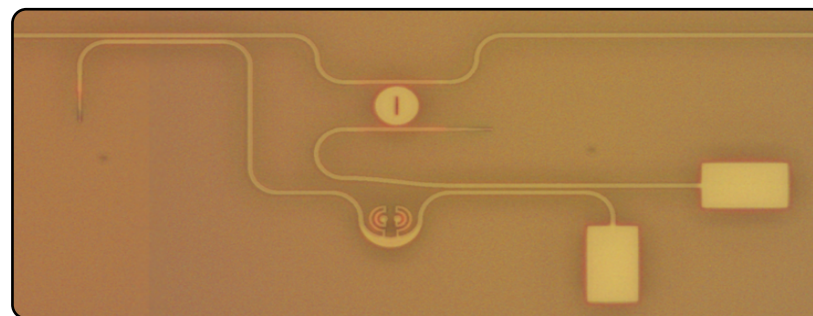
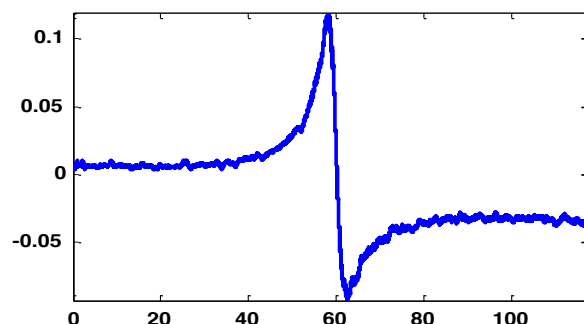
- **IBM 45 nm CMOS** ASIC designed at Sandia
- **Power consumption:** 1.07 mW (steady-state); 0.27 mW (TIA) and 0.8 mW (integrator) (30 – 100 fJ/bit @ 30Gbps-10Gbps) [1]
- **Heater time constant** → large integrator resistor and capacitor in loop filter
- **Heater driver:** Class-B “push-pull”
- **Inverter** implemented with analog switch network



[1] recent result by X. Zheng (OpX 2014) 200 μW , 2600 μm^2 for ‘power meter’ control

Summary

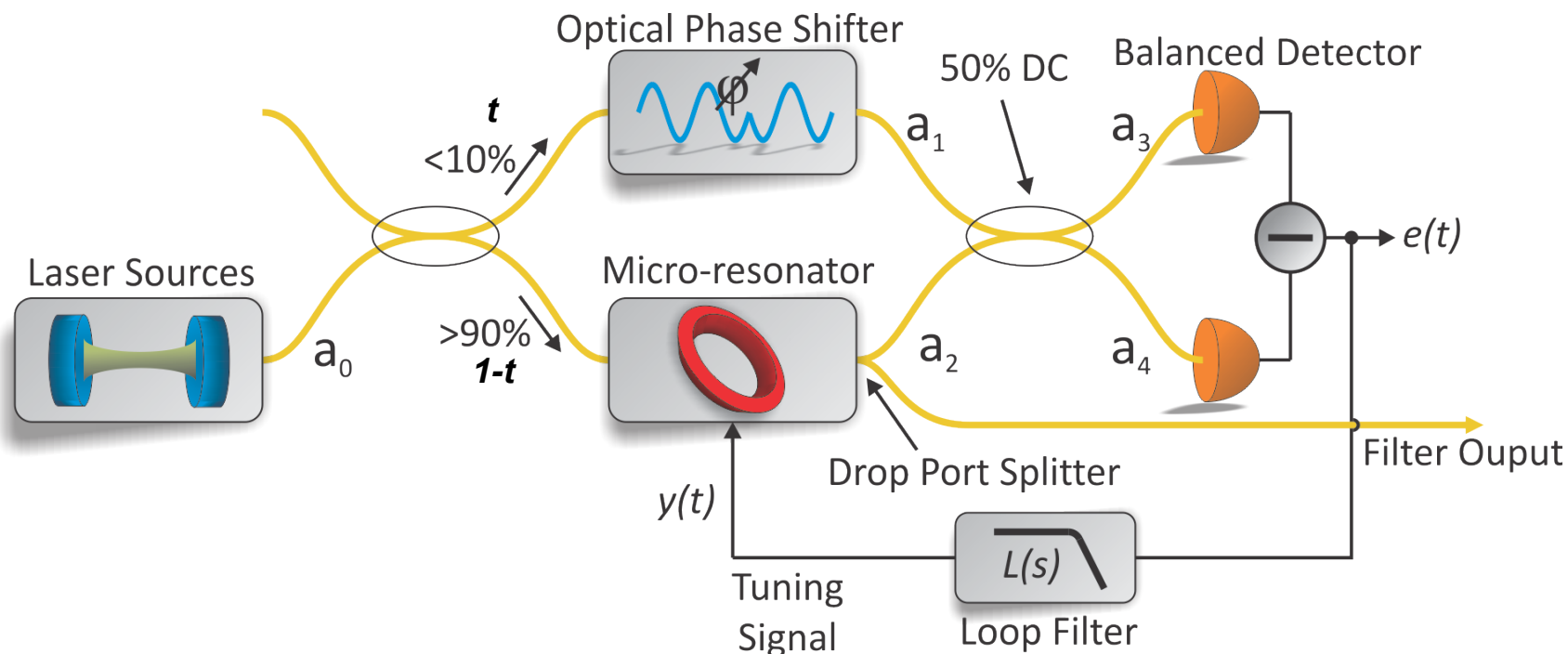
- BHD provides a scalable, robust method for resonant modulator and filter wavelength stabilization
- Advantages
 - Suitable for DWDM networks
 - Insensitive to laser intensity noise
 - Arbitrary locking reference not required (lock to zero)
 - Simple control circuitry for dense on-chip integration
 - Precision locking for other micro-resonators application



J.A. Cox, A.L. Lentine, D.C. Trotter and A.L. Starbuck, "Control of integrated micro-resonator wavelength via balanced homodyne locking," *Opt. Express* Vol. 22(9) (2014)

Backup Slides

Balanced Homodyne Detection



BHD Transfer Function

$$Y(\beta) = -\alpha G a_0^2 |K|^4 \frac{a_m n}{Z_0} \sqrt{t - t^2} \left(\frac{e^{i\phi}}{K^2} \frac{e^{-i2\pi R\beta}}{e^{-i4\pi R\beta} + |K|^2 - 1} + \frac{e^{-i\phi}}{K^2} \frac{e^{i2\pi R\beta}}{e^{i4\pi R\beta} + |K|^2 - 1} \right)$$

What is Silicon Photonics?

- Active and Passive Photonics on/in Silicon

- Passive:

- Waveguides, spectral filters, splitters, polarizers, polarization rotators, gratings, isolators*

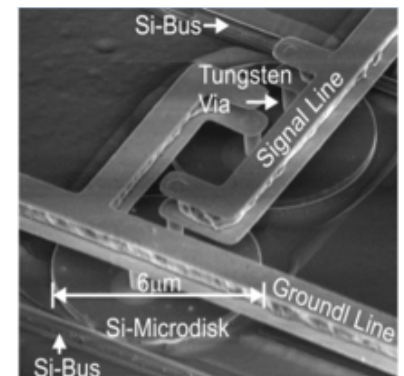
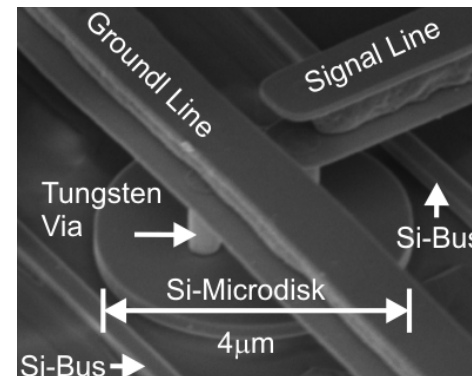
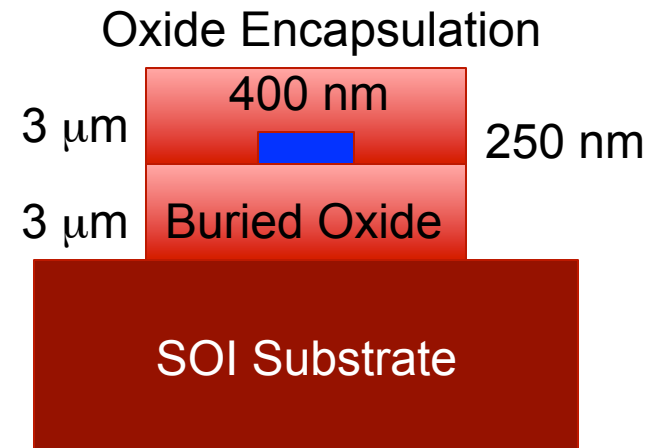
- Active

- Modulators(EO), switches, detectors (OE, Ge), lasers*

- Thermal Shift of index
- Electro-refraction
- Electro-absorption (SiGe)

- Most applications require intimate integration with CMOS Electronics

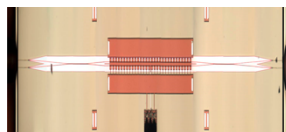
- Heterogeneous integration
 - Flip-chip bonding, Wafer bonding, etc.
- Monolithic integration



* Heterogeneous integration

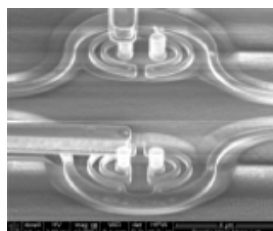
2 x 2 silicon photonics switches

- Fast ($< 100\text{ps}$)
- Broadband
- $1\text{pJ}/\text{switching event}$
- No static power
- 1 mm size



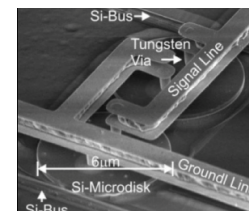
MZ – free carrier effect

- Slow (10 us)
- Broadband
- $\sim 15\text{ mW}/2\pi$
- Static power in one state
- $< 10\text{ um}$ size + coupler



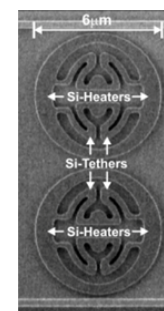
MZ – thermo-optic

- Fast ($< 100\text{ps}$)
- Wavelength selective*
- $1\text{fJ}/\text{switching event}$
- No static power
- $< 10\text{ um}$ size



Ring – free carrier effect

- Slow (10 us)
- Wavelength selective
- $\sim 4\text{ uW}/\text{GHz}$ (200uW)
- Static power in one state
- $< 10\text{ um}$ size



Ring – thermo-optic

*Can also switch all channels at once if free spectral range = channel spacing