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Fabrication of multi-device layer, planarized SNS Ta_xN Josephson junctions

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Traditional superconducting electronics employ a planarized multilayer fabrication process, consisting of a single device layer with multiple metallization layers. Typical fabrication protocols restrict processes such as dielectric deposition temperatures after the junction layer has been formed due to potential barrier breakdown resulting in junction failure. This temperature restriction can impact the quality of silicon dioxide layers for chemical mechanical polishing and in high frequency applications.

In this work, we explore a planarized multilayer niobium process for investigating properties of Ta_xN barrier Josephson junctions. By controlling processes which permit the Mott-Cabrera based oxidation of Nb, a processing module which deposits, patterns and planarizes a combined in-situ metallization stack of routing metal and junction layer can be repeated to create multiple routing layers and multiple junction layers at the wafer scale. This work will describe the fabrication details and impacts upon wafer level yield as measured by room temperature electrical measurements, wafer curvature, ellipsometry and cryogenic electrical measurements. Impacts upon the superconducting Nb films during the fabrication processes such as photoresist strip will be discussed as will the planarization process. The critical currents and barrier resistances of of self-shunted Nb-Ta_xN-Nb junctions with diameters ranging from 2 to 10 microns will be presented.

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