SAND2014-18821PE

ERD Emerging Memory Assessment Workshop Update

Workshop Objectives

- Evaluate emerging memory technologies
  - How does it work? What are the key advantages? What are the most suitable applications?
  - What is the state-of-the-art?
  - What are the major challenges and possible solutions?
  - What should industry and academia focus on?
- Identify promising candidates
  - Survey of workshop participants

Workshop Format

- Advocate presentations (30 min)
- Friendly critic presentations (20 min)
- Discussions (20 min)

- All the presentations have been made available (with authors' permission):

https://backup.filesanywhere.com/fs/v.aspx?v=8c716a8759646fbeac6b

- ERD is working on the report of the workshop

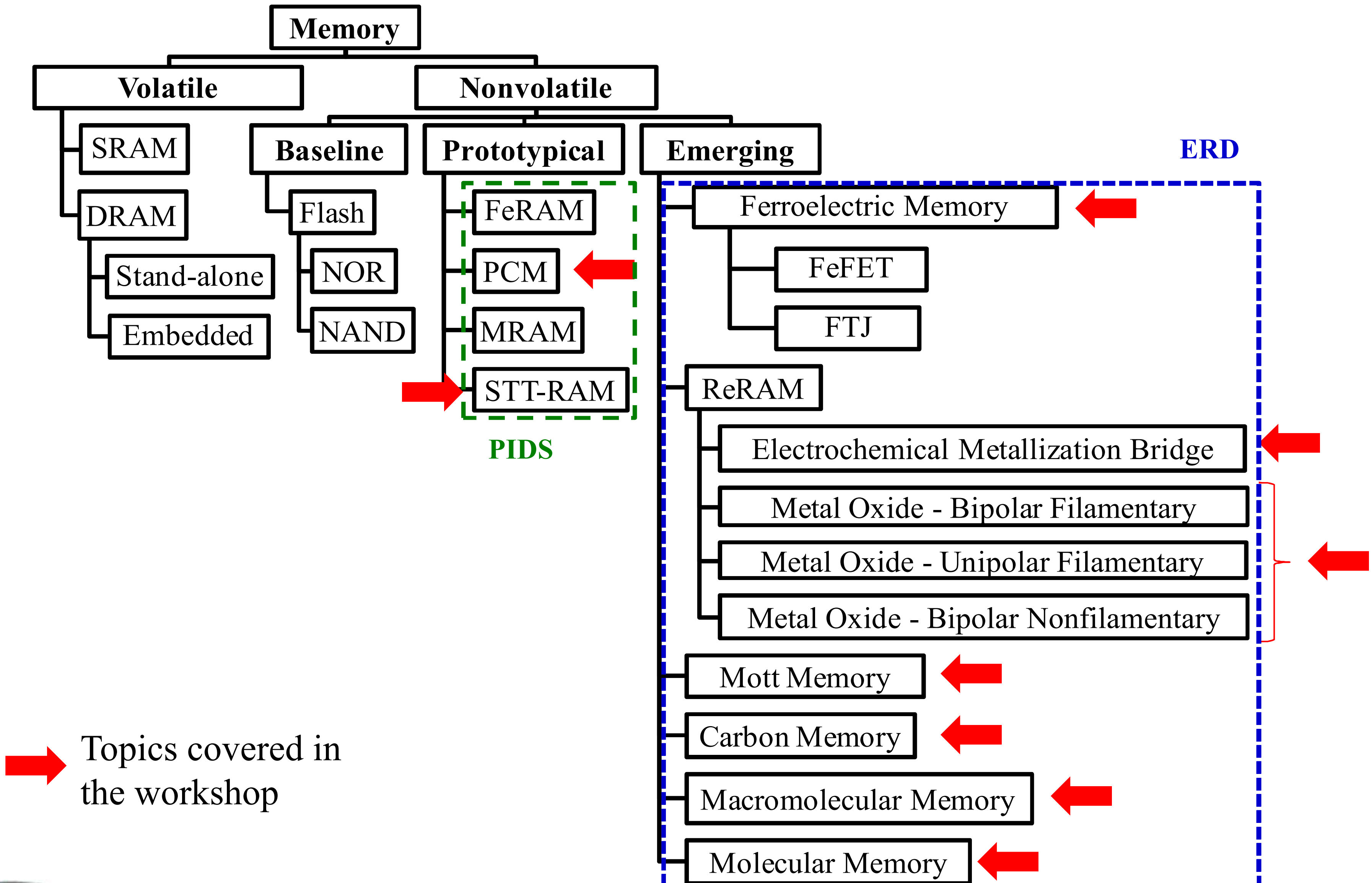
Agenda – Day 1 (Aug. 25, Monday)

Time	Topic	Presenter
11:00am	Registration	
11:30am – 11:50am	Introduction	ERD
11:50am – 1:00pm	***Lunch talk "Potential and Challenges of RRAM"***	***Simon Wong / Stanford U.***
1:00pm – 1:30pm	PCM advocate presentation	Hsiang-Lan Lung / Macronix
1:30pm - 1:50pm	PCM friendly critic presentation	Geoff Burr / IBM
1:50pm – 2:10pm	PCM discussion	Erik DeBenedictis / Sandia
2:10pm – 2:40pm	STTRAM/MeRAM advocate presentation	Min Tai / IMEC
2:40pm – 3:00pm	STTRAM/MeRAM friendly critic presentation	Kelly Baker / Freescale
3:00pm – 3:20pm	STTRAM/MeRAM discussion	An Chen / GF
3:20pm – 3:40pm	***Break***	
3:40pm – 4:20pm	Emerging Ferroelectric Memory advocate presentation	Johannes Muller / Fraunhofer CNT; T.P. Ma / Yale U.
4:20pm – 4:50pm	Emerging Ferroelectric Memory organized discussion	Matt Marinella / Sandia
4:50pm – 5:20pm	Carbon-based Memory advocate presentation	Franz Kreupl / TU Muenchen
5:20pm – 5:40pm	Carbon-based Memory friendly critic presentation	Wabe Koelmans / IBM
5:40pm – 6:00pm	Carbon-based Memory discussion	Mike Garner / Stanford
8:00pm – 9:00pm	Evening discussion	

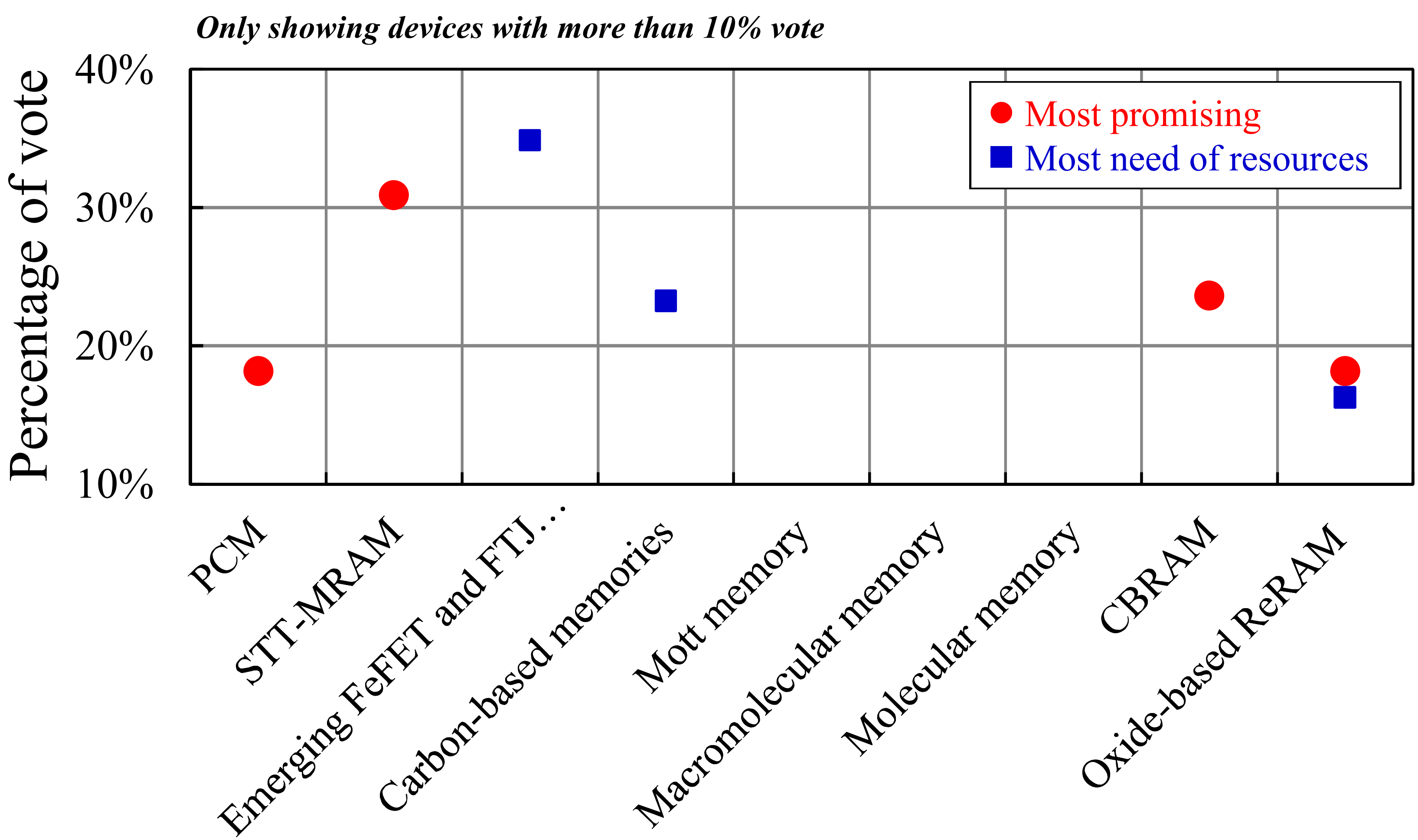
Agenda – Day 2 (Aug. 26, Tuesday)

Time	**Topic**	**Presenter**
8:00am	Breakfast	
8:30am – 8:35am	Introduction	ERD
8:35am – 9:20am	**Keynote**	**Gilbert V. Herrera / Sandia**
9:20am – 9:50am	Mott Memory advocate presentation	Xia Hong / U. Nebraska
9:50am – 10:20am	Mott Memory organized discussion	Zoran Krivokapic / GF
10:20am – 10:40am	***Break***	
10:40am – 11:10am	Macromolecular Memory advocate presentation	Stefan Meskers / TU Eindhoven
11:10am – 11:30am	Macromolecular Memory friendly critic presentation	Victor Zhirnov / SRC
11:30am – 11:50am	Macromolecular Memory discussion	Jim Hutchby / SRC
11:50am – 1:00pm	***Lunch talk "Perspective of spintronics – energy scaling and its integration with CMOS"***	***Kang Wang / UCLA***
1:00pm – 1:30pm	Molecular memory: organized discussion	Matt Marinella / Sandia
1:30pm – 2:00pm	CBRAM advocate presentation	Jun Sumino / Sony
2:00pm – 2:20pm	CBRAM friendly critic presentation	Stan Williams / HP
2:20pm – 2:50pm	CBRAM discussion	Mark Kellam / Rambus
2:50pm – 3:10pm	***Break***	
3:10pm – 3:55pm	Oxide-based RRAM advocate presentation	Malgorzata Jurczak / IMEC
3:55pm – 4:20pm	Oxide-based RRAM friendly critic presentation	Seung Kang / Qualcomm
4:20pm – 4:50pm	Oxide-based RRAM discussion	Matt Marinella / Sandia
4:50pm – 6:00pm	Emerging memory priority selection; summary	All
6:00pm	Meeting adjourn	

ERD Memory Entry & Workshop Topics



Survey Result



Most Promising Devices

STT-RAM

Advantages:	Challenges:
• The closet to working memory (SRAM, DRAM) performance, better than any other emerging memories • Well-understood device physics and material engineering • Significant progress in device parameters and processing in the past 5 years	• Although excellent performance is shown on devices, repeatability and manufacturability needs to be confirmed • Cost/bit is a major issue; lack of MLC and 3D strategy • Limited demonstration of high temp data • Variability control is critical

Key observations:

- R&D focus has shifted from in-plane to perpendicular. Perpendicular MTJ has demonstrated the following characteristics:
- Nearly "infinite" endurance for switching voltage below 650mV
- Sub-5ns read and write operation in a 8Mb test chip between -25°C and 125°C
- Thermal stability after 400°C 90min annealing, ready for BEOL CMOS process
- Switching V/I reduced to <450mV/60µA at error rate below 10^{-7} for 37nm MTJs
- Scalability down to 15nm demonstrated
- MeRAM looks exciting for reduced energy writes and endurance, but much work is needed to demonstrate useful operating window

Phase Change Memory

Advantages:

- Very mature (large-scale demos & products)
- Industry consensus on material GeSbTe or GST
- Large resistance contrast analog states for MLC (& neuromorphic computing)
- Offers much better endurance than Flash
- Shown to be highly scalable (still works at ultra-small F) and Back-End-Of-the-Line compatible
- Can be very fast (depending on material & doping)

Challenges:

- RESET step to high resistance requires melting -> power-hungry, thermal crosstalk? To keep switching power down -> sub-lithographic feature and high-current Access Device To fill small feature -> ALD or CVD -> difficult now to replace GST with a better material Variability in small features broadens resistance distributions
- 10-year retention at elevated temperatures can be an issue recrystallization
- Device characteristics change over time due to elemental segregation -> device failure
- MLC strongly affected by relaxation of amorphous phase -> resistance drift

Key observations:

- The tradeoffs that bedevil PCM are almost all amenable to engineering – many of its problems could potentially be finessed with new invention.
- Unlike most of the other emerging NVMs, there don’t appear to be any fundamental “physics” showstoppers for PCM…

CBRAM

Advantages:	Challenges:
• High scalability, <10nm; high density possible with $4F^2$ crossbar • High endurance • Low voltage; low switching energy • CMOS BEOL compatible process • Wide res range; MLC possible • Recent results show improved high temperature retention	• Historically poor retention • New materials may be required • Retention-switching speed trade-off • Need select device Variability • Device to device • Random telegraph noise

Key observations:

- Significant progress in recent years
- Numerous demonstrations of test macros have been demonstrated in the past two years, including Sony/Micron (presenter at workshop)
- Retention is historically problematic, but has been improved with new materials
- Low density commercial product available

Oxide-based ReRAM

Advantages:	Challenges:
• High scalability, <10nm; high density possible with $4F^2$ crossbar • High endurance, good retention • Fast read and write; low switching energy • CMOS compatible materials & process • Resistive crossbar compatible; can be layered • Numerous test chip demos (up to 32Gbit)	• Product-level limitations • Need lower current, ~1 uA range Variability • Device to device • Cycle to cycle • Random telegraph noise • Forming process – want forming free • Details of mechanism under debate

Key observations:

- Focus of talk (an most work) is on bipolar, although unipolar and nonfilamentary are included in ERD
- Large increase in interest in the past two years; significant progress has been made
- Variability is a key problem
- Low density commercial product available (Panasonic)

Most In Need of Resources

Emerging Ferroelectric Memory

Advantages:	Challenges:
FeFET • High endurance possible • Doped HfO is highly CMOS compatible • Fast switching speed and low sw energy • Scalable FTJ – (combines adv. FeFET w RRAM) • Low switching energy • Bit is scalable and crosspoint array compatible (FET not required)	FeFET • Retention historically poor; can only optimize for endurance/retention • Discovery of FE-HfO:x relatively recent; some controversy in mechanism FTJ • Immature technology – memory properties not well understood

Key observations:
FeFET • Promising new results have turned research focus from traditional materials (eg PZT) to doped HfO. This has created a renewed interest in FeFET • HfO process demonstrated with slightly modified HKMG CMOS flow • Possible to optimize for endurance or retention (difficult to get both) FTJ (less focus in presentation) • Interesting technology to watch, could combine advantages of RRAM with FeFET, but currently immature. Could make use of FE-HfO.

Carbon-based Memories

Advantages: (depend on memory type)	Challenges:
• High endurance (Nantero) • Good retention; high temperature operation possible (Nantero) • Scalable "to single atomic bond dimensions" • Resistive crossbar compatible – high density	• Contact resistance • Variability (similar or worse than ReRAM) • High switching voltage for certain types

Key observations:

- This category is not well understood. Many mechanisms and materials could be incl
- Speaker suggested two different mechanism – possible method of categorization
    1. low mass density: break-junction by local evaporation of carbon and plumbing by field emission
    2. high mass density: conversion of a-C ↔ sp2-bonds
- Decision: categorize by material or mechanism
- Carbon nanotubes, graphene, a-C
- Speaker does not consider carbon memory if metal is diffused through – should we adopt this?

“Other” Emerging Memories

Mott Memory

Advantages:	Challenges:
• Scalability (in theory) below 1nm • Sub-ns switching time • Tunable carrier density and band gap • Significant memory effect at moderate electric field, i.e., low-power operation • Variety of control factors for metal-insulator transition: carrier density, T, E, strain, and optical excitation	• Require growth techniques for large-scale high-quality thin film oxides; solutions exist but are not industry compatible • Precise control of material property at nanoscale with high-level of uniformity is challenging • Stoichiometry and defect control is critical

Key observations:

- It is possible to build FET-like devices with gate-modulated MIT
- Still need to find materials with sufficiently high transition temperature suitable for industry processing and applications
- MIT mechanism itself is not non-volatile; need other mechanisms (e.g., ferroelectrics) to maintain the transition condition for retention

Macromolecular Memory

Advantages:	Challenges:
• Option for flexible electronics • Compliance not needed • Solution processing; inexpensive materials (this claim was controversial)	• High programming voltage • Sensitive to oxygen • Switching dead time • Mechanisms not well understood • Endurance • Retention • Materials not CMOS compatible – difficulty surviving BEOL temperatures

Key observations:

- Category not well understood – mixed with molecular to some degree
- Mechanisms reported ften similar to ReRAM

Need better definition in 2014 roadmap

- Option 1: Combine with Macromolecular
- Option 2: Drop
- Option 3: Boneyard (Geoff)

Molecular Memory

Advantages:	Challenges:
• Ultimate scalability, information stored in single molecule	• Lack of device demonstration • Experiments very difficult – contact tends to obscure molecule results • Poor demonstrated endurance and retention • Progress on true single molecule switching very limited

Key observations:
• Category not well understood – mixed with macromolecular to some degree • Many historic demonstrations of interest turned out to be parasitic/contact effects, possibly ionic switching • Single molecule conduction should be in pA range (Victor)

Summary

- Those promising has not changed
  - PCRAM
  - STT-MRAM
  - Oxide ReRAM
- "In need of resources" gave new results:
  - Oxide ReRAM (also most promising)
  - Emerging Ferrorelectric Memories
  - Carbon Memories
- Splitting CBRAM and MO-ReRAM was worthwhile – they ranked differently
- Should we create a bone-yard?

Acknowledgements

- Sandia National Laboratories - Julie Phillips, CTO
- Sandia National Laboratories – Gil Herrera, Director, MESA
- Sandia staff: Valerie Valdez, Denise LaPorte, Christina Pidanick, Virginia Lujan
- All the invited speakers
- ERD organizing committee