SAND2014-17866PE

Exceptional service in the national interest

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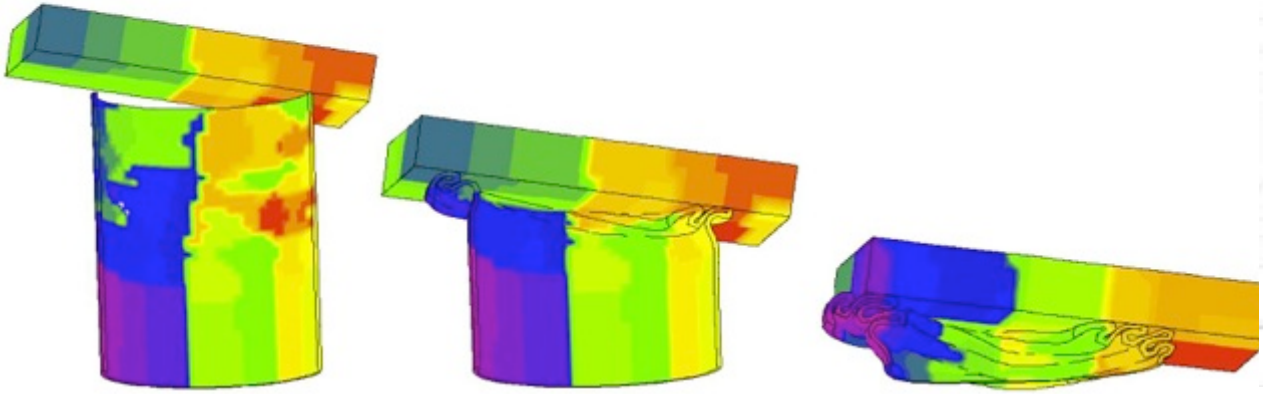
Finite Element Model (FEM) of a Crushed Can

Courtesy of Sandia CSRI



Si Photonics for Exascale Computing

Paul Davids, Anthony Lentine, Chris DeRose, Jonathan Cox, Andrew Pomerene, Andrew Starbuck, Doug Trotter.

U.S. DEPARTMENT OF ENERGY | NNSA

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CMOS interconnect scaling

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As CMOS technology node scales

- More smaller transistors and more logic operations
- Capacitance per length is constant
- Resistance per length is increasing
- ***Interconnect speed is slowing down!***
- ***Interconnect power is increasing!***

- ***Interconnect limits scaling of large ICs (e. g. CPUs)***

Need a breakthrough for global on-chip interconnections

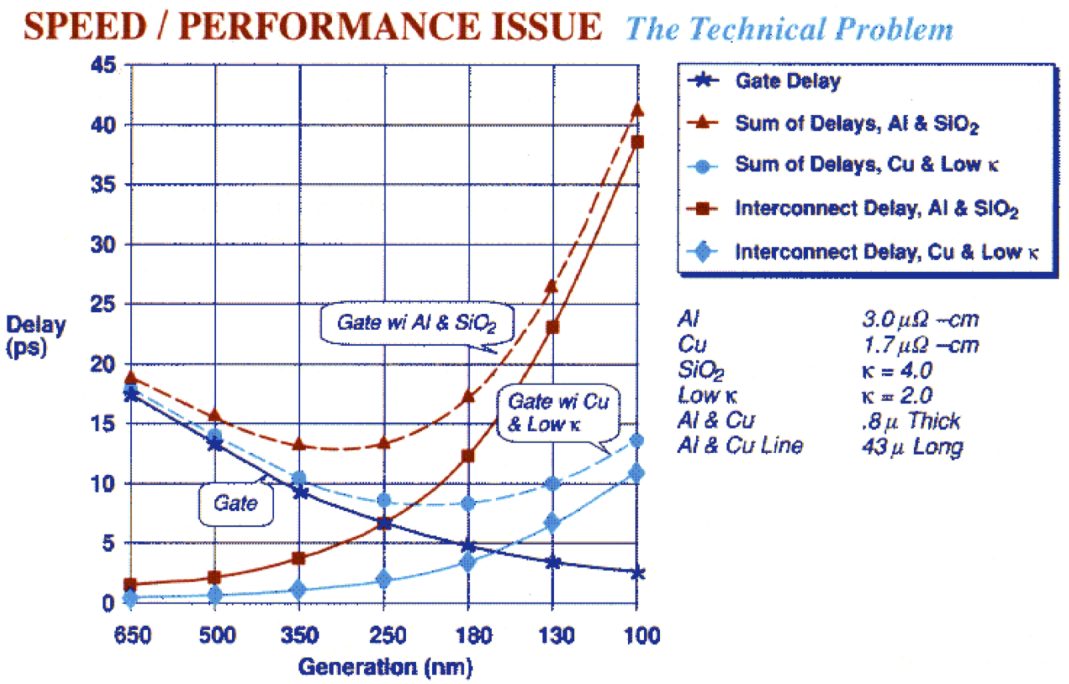
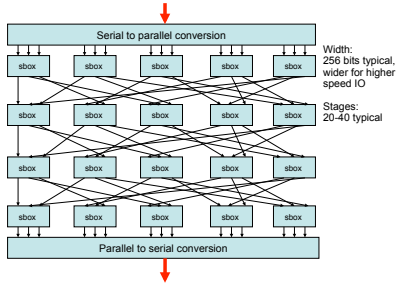


Figure 3 Calculated Gate and Interconnect Delay versus Technology Generation

Calculated gate and interconnect delay versus technology generation illustrating the dominance of interconnect delay over gate delay for aluminum metallization and silicon dioxide dielectrics as feature sizes approach 100 nm. Also shown is the decrease in interconnect delay and improved overall performance expected for copper and low κ dielectric constant insulators.

March 28, 2008

DARPA Places $44M Bet On Optical Interconnects



Trouble in River City

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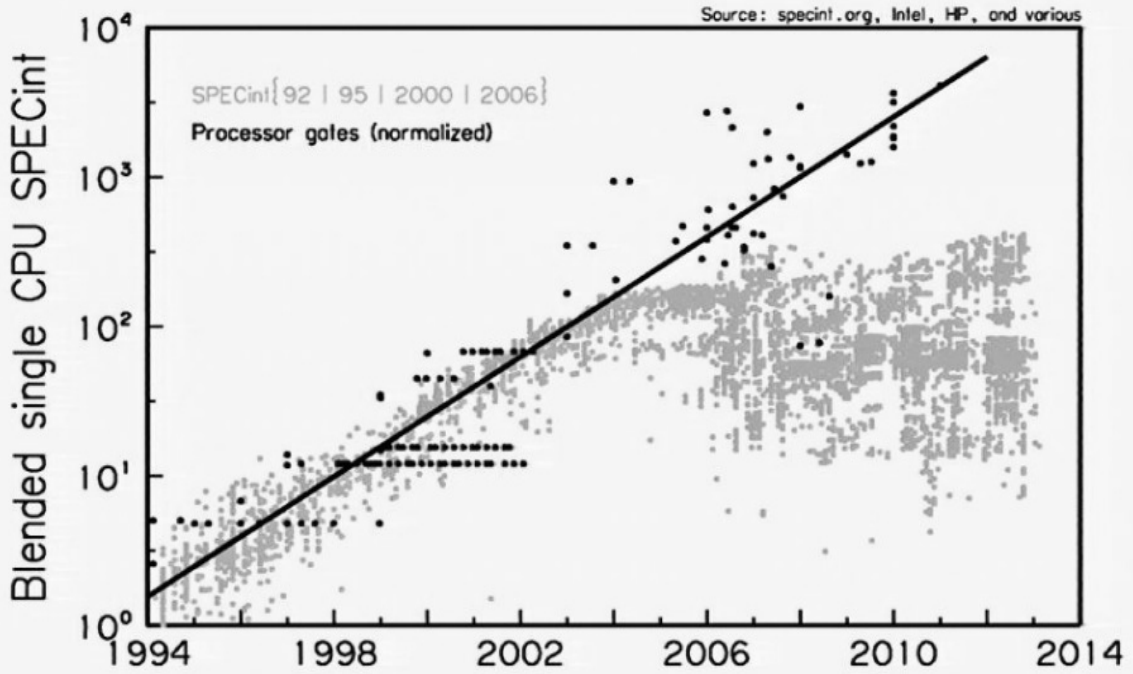
- Overlay SPECint performance data w/ growth in processor transistor count
- Increase in transistors for the past ~9 years has not given commensurate performance benefit
  - 10X increase in gates
  - 10X drop in performance



Adapted from Greg Astfalk, Hewlett Packard
Processors and Sockets, What's next?
Salishan High Speed Computing Conference, April, 2013

- Slide from Rob Leland's presentation at Sandia on 'Beyond Moore's Law'

Lack of scaling in Moore's Law is an interconnect problem

- Gate delay (transistor performance) speeds are scaling
- On-chip RC lines are not scaling
  - Capacitance is nearly constant (fringing)
  - R is increasing as line widths narrow
  - Increased repeaters for long lines
- Power = CV^2f (C dominated by interconnect)
  - V also not scaling (transistor)
- Off-chip (electrical)
  - Looming divergent capacity compared to on-chip processing capability

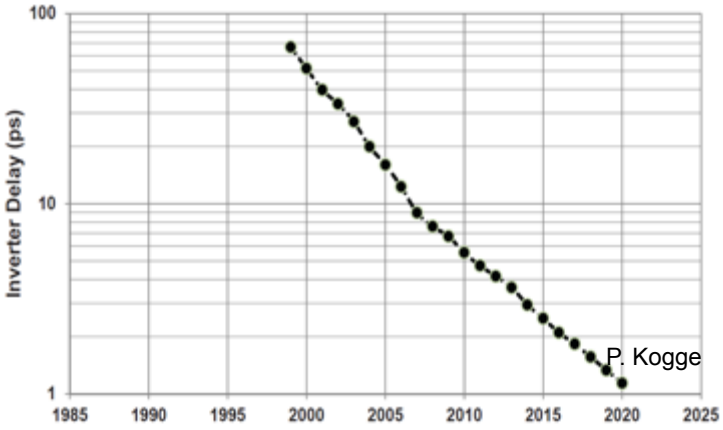
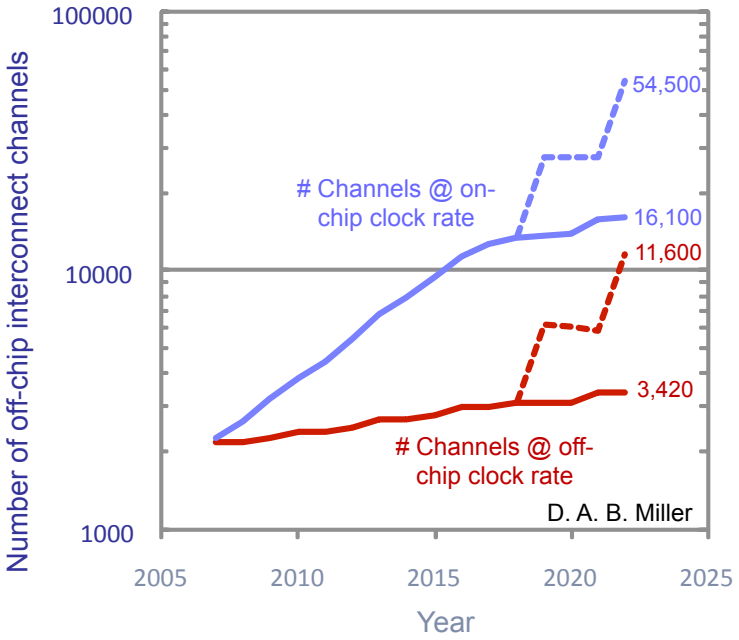
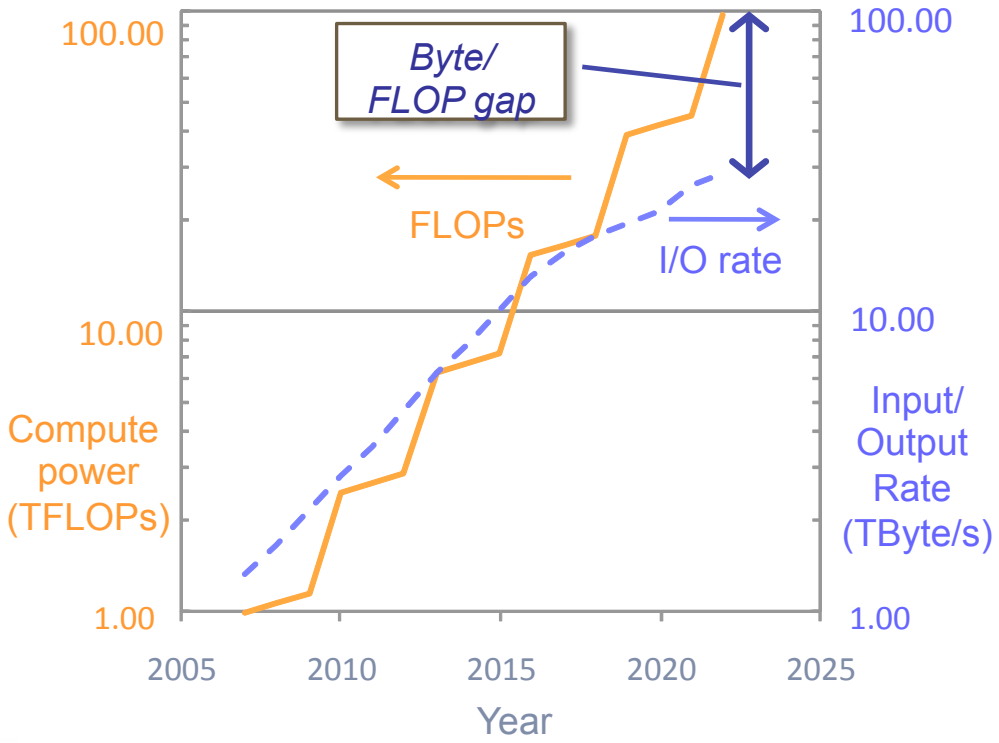
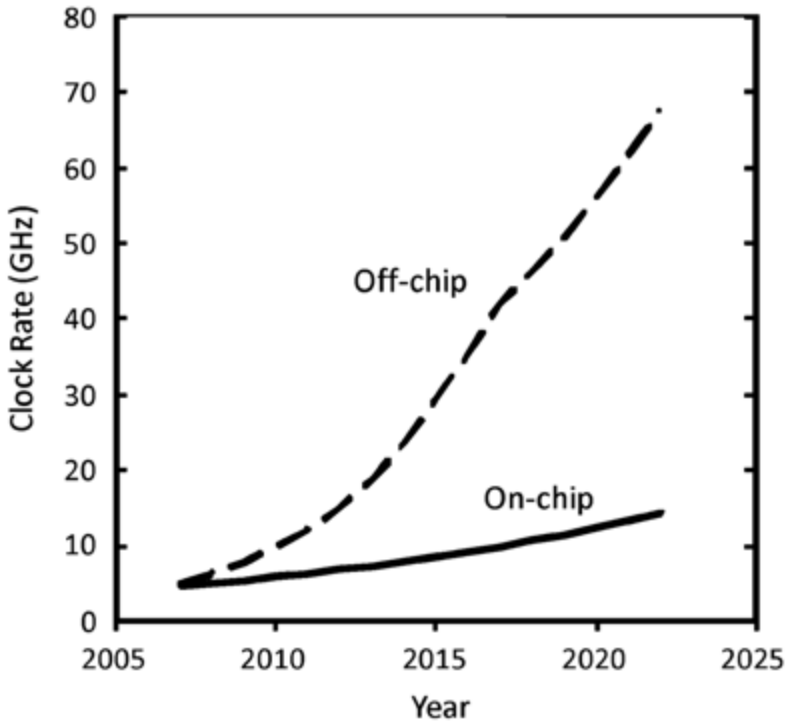


Figure 2.2: Inverter Delay as Derived from ITRS.



Why Photonics: ITRS Projected Chip Performance: Bytes/FLOP



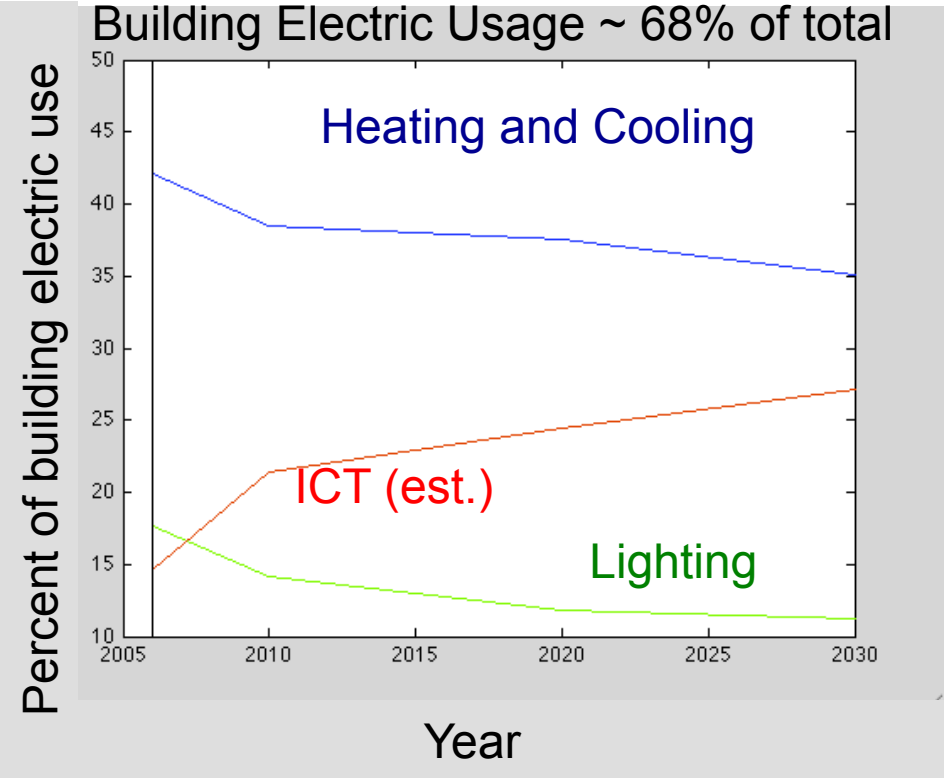


- Input / Output interconnect (I/O) rate does not keep up
- Electronics is quite high: 80 Tb/s/IC (30 Gbps) by 2015.
- Will the roadmap hold true?
- What about the power?

D. A. B. Miller, 'Device Requirements for Optical Interconnects to Silicon Chips,' Proc. IEEE 97, 1166 - 1185 (2009).

ICT Energy usage: Energy Security

- ICT consumes 10% of US Electricity (Wiki)
- ICT contributes 2.0%-2.5% of global greenhouse gas emissions, to 4% by 2020 (www.greentouch.org)
  - generation and distribution of electricity accounts for about ¼ of global greenhouse gas emissions.
- Data Centers are 2.5% and growing.
- 'Other', 'Electronics', and 'Computers' which include ICT infrastructure is growing, Heating, Cooling, and Lighting are decreasing (**2009 Buildings Energy Data Book**)

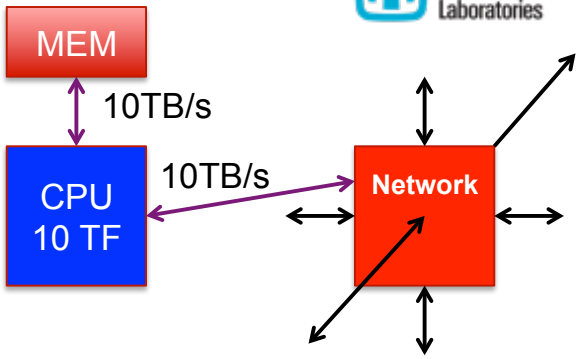


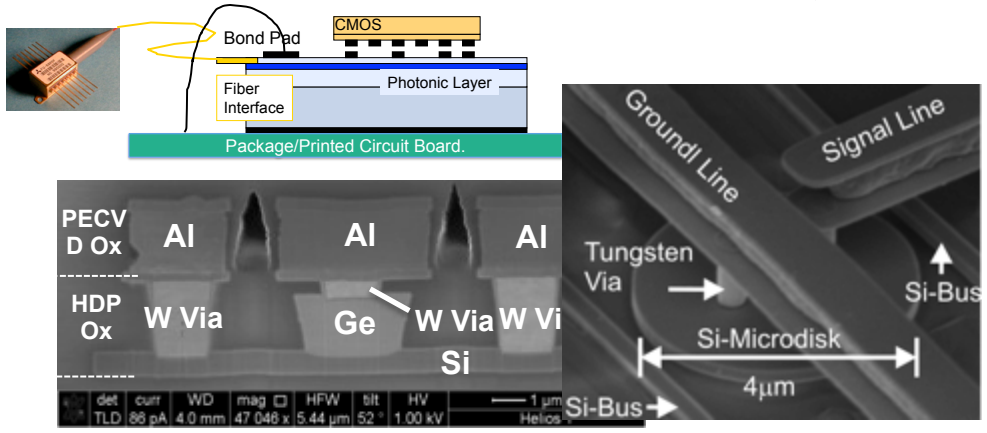
ICT (est.) = normalized to 10% of US electricity usage in 2006
Data estimated from 2009 BE data book

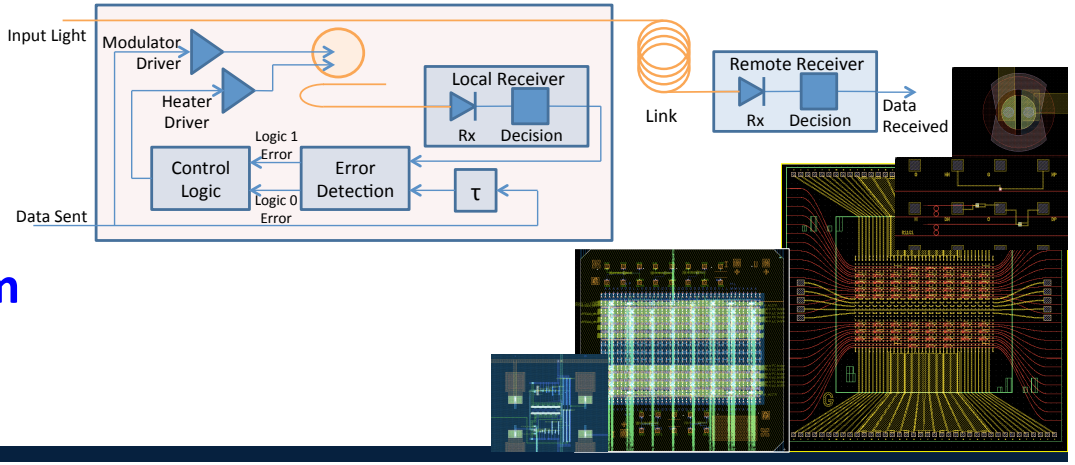
Conclusion: Large Numbers and growing!

Exascale Approach

- Instead of … Evolutionary architecture approach:
  - Design around limited (network and memory) interconnect bandwidth (<< 1 bit per second/flop)
- Pursue … Revolutionary approach:
  - Small silicon micro-photonic devices intimately integrated with network and processor ICs
  - Chip-scale 100s Tbps IO
  - <100 femtojoule/bit → <10sW IO
- Identify and solve critical technology gaps
- Identify fundamental/practical limits
- **Co-design: information to/from architecture, modeling, and simulation**







Exascale Computing Example: Local and Global Communications

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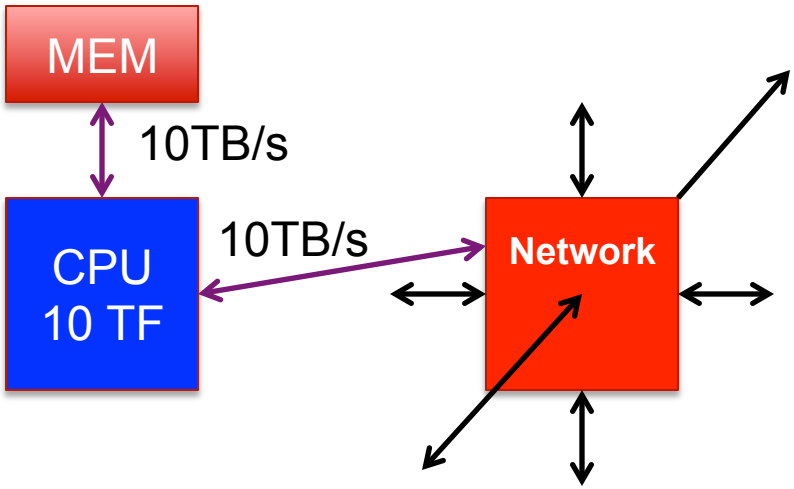
Memory Connection Requirements (approx.)

- > 10^{18} FLOPS
- > 10^{18} B/s Memory bandwidth
- < 100,000 IC →10 TF/IC → 10 TB/s (***80 Tb/s)***
- > 40k (200 x 200) connections @ 2Gb/s → 3DI
- < 2 MegaWatt (20W/IC) consumption
- < 250 fJ/bit per memory access



Network Connection Requirements (approx.)

- > 10^{18} B/s cross section bandwidth
- < 100,000 IC →10 TF/IC → 10 TB/IC (CPU)
- > 120 TB/s (960Tb/s) IO BW/IC (Network IC) (3D-mesh arch., bidirectional, 6 directions)
- > 48,000 Tx @ 10 Gb/s/Tx
- > 48,000 Rx @ 10 Gb/s/Rx
- < 5 MegaWatt (50W/IC) consumption
- < 100 fJ/bit/connection *total*

Potential Photonics Solution Requirements

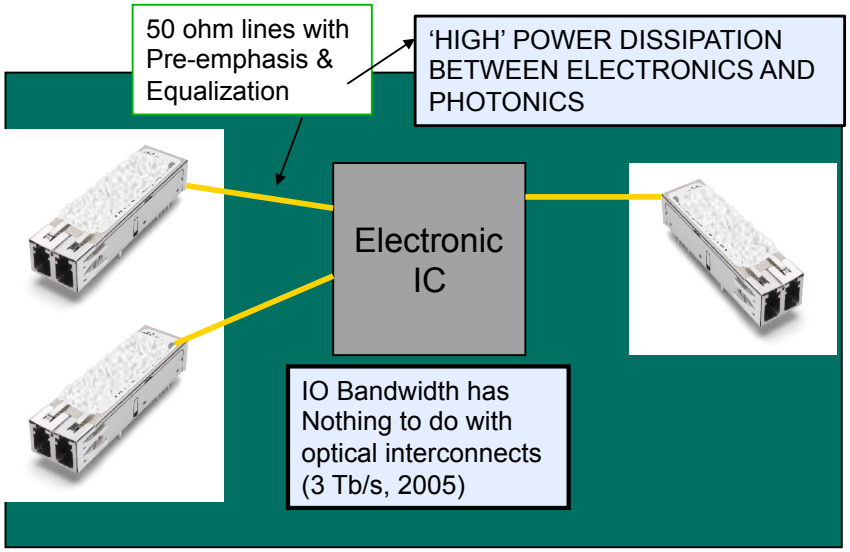
- Single Mode (Rx power requirement)
- DWDM (connection BW density)
- High reliability (48 Billion Transmitters)
  - Reverse biased devices
  - Silicon devices
- Heterogeneous Integration – no 50Ω
- Suitable for packaging with fibers, waveguides, sources, detectors, etc.

Silicon Photonics is the enabling technology

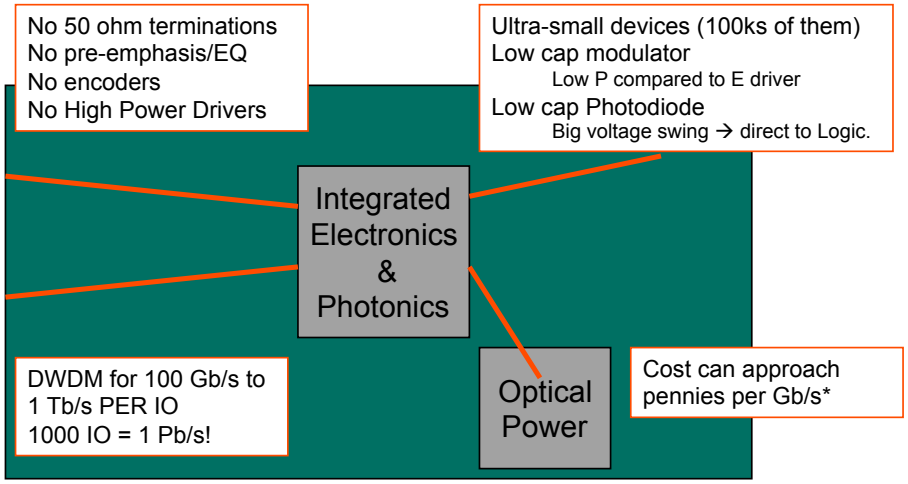
Optical Interconnects

- Evolutionary (Modules)
  - GbE and 10GbE Products
  - 100 GbE modules soon w/ VCSELs and Si Photonics
  - TbE modules on the horizon

- **Revolutionary (3DI)**
  - **Higher bandwidth density**
    - **DWDM is required!!**
  - **Drastic *potential* power reduction**
    - **No 50 Ω lines, pre-emphasis or equalization**
    - **Receiver has high transimpedance, few gain stages**
    - **Shared CDR (less delay variation and jitter)**



OPTICS FOR DISTANCE



OPTICS FOR *LOW POWER*, *HIGH BANDWIDTH DENSITY*, COST, SIZE, WEIGHT, DISTANCE

Silicon Photonics: Enabling a revolution in SWaP, function, and cost.

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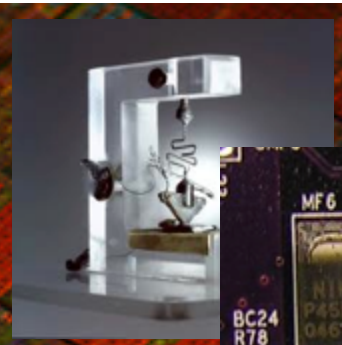
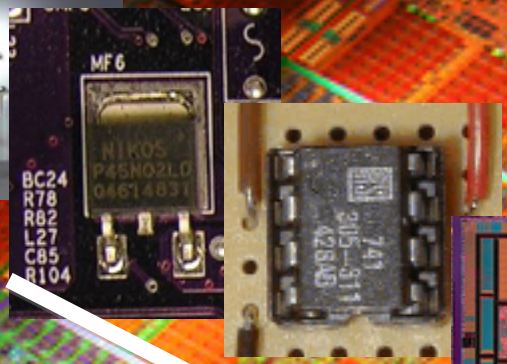
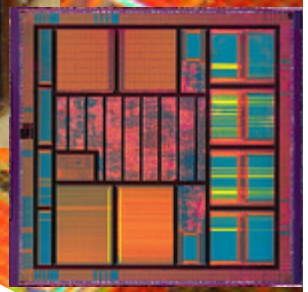
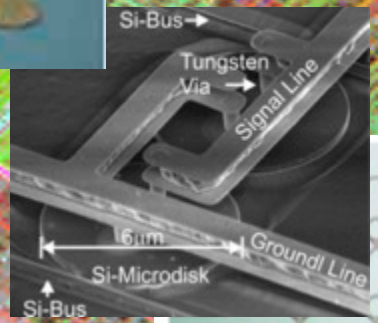
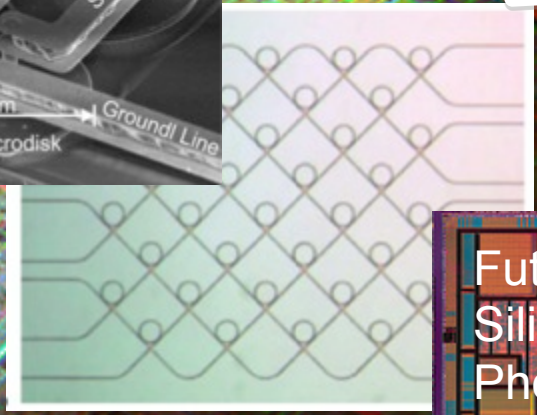
- Takes advantage of decades of progress in Si VLSI
- Most key optical devices demonstrated
- Next: Integration & Systems

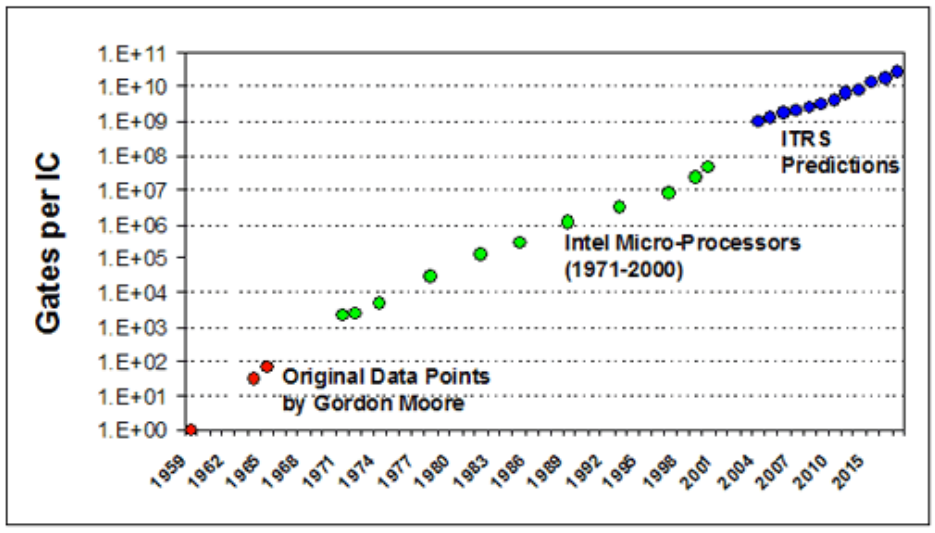






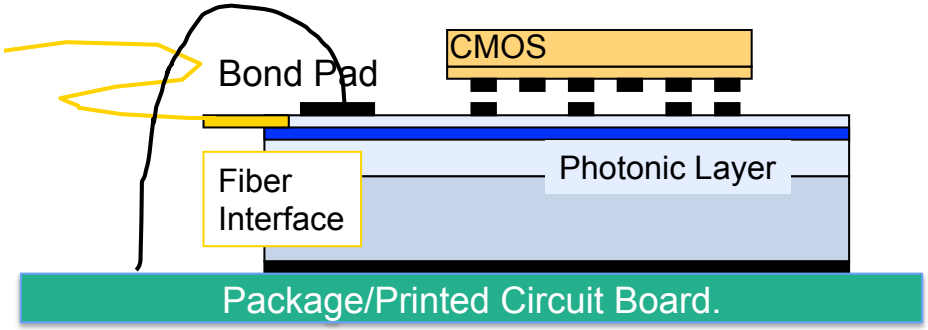


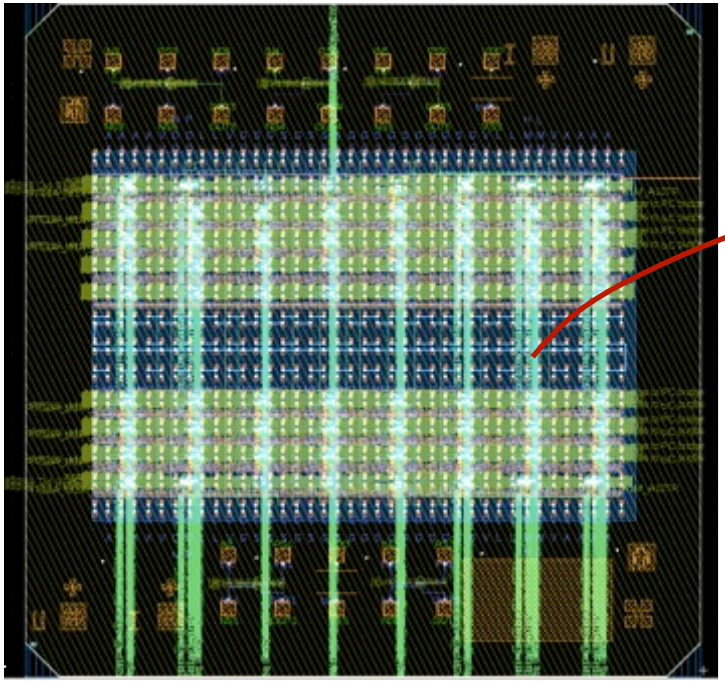


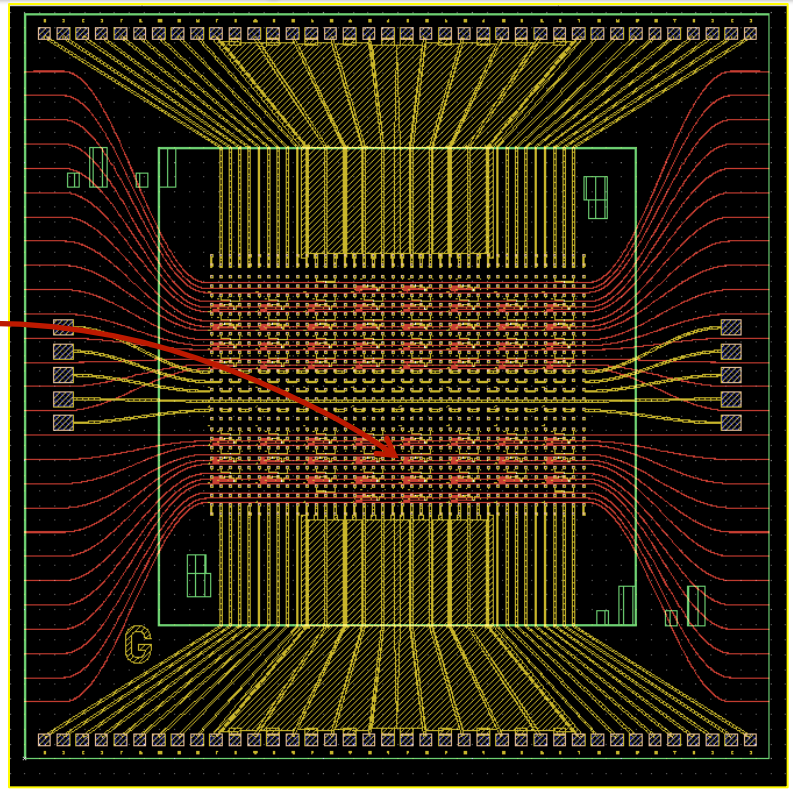


Electronic-Photonics Integration

- Heterogeneous integration
  - Independent optimization of electronics & photonics
  - Need very high yields and small size







Electronic-Photonics Integration

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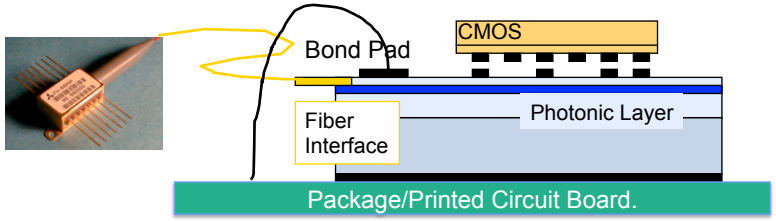
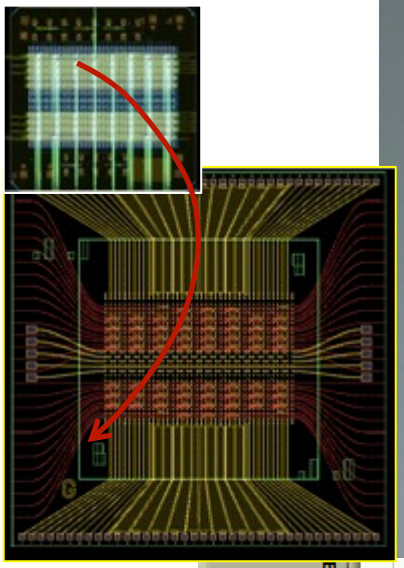
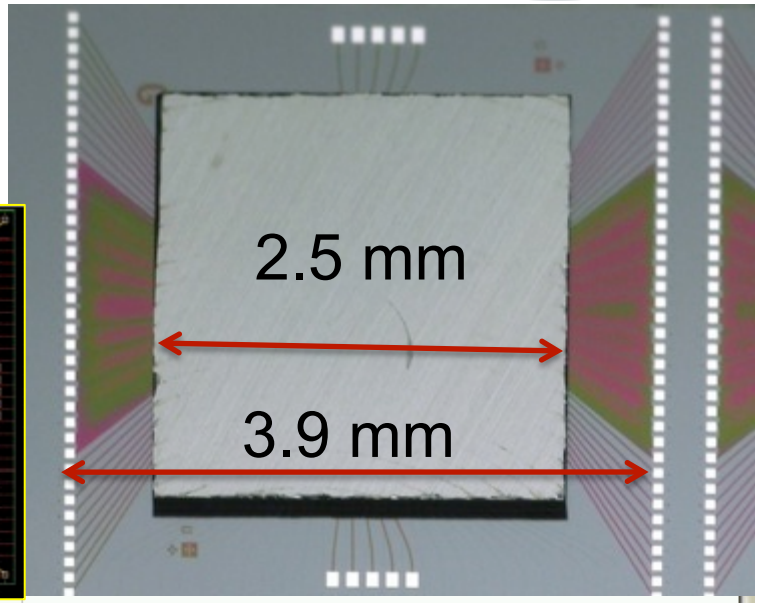
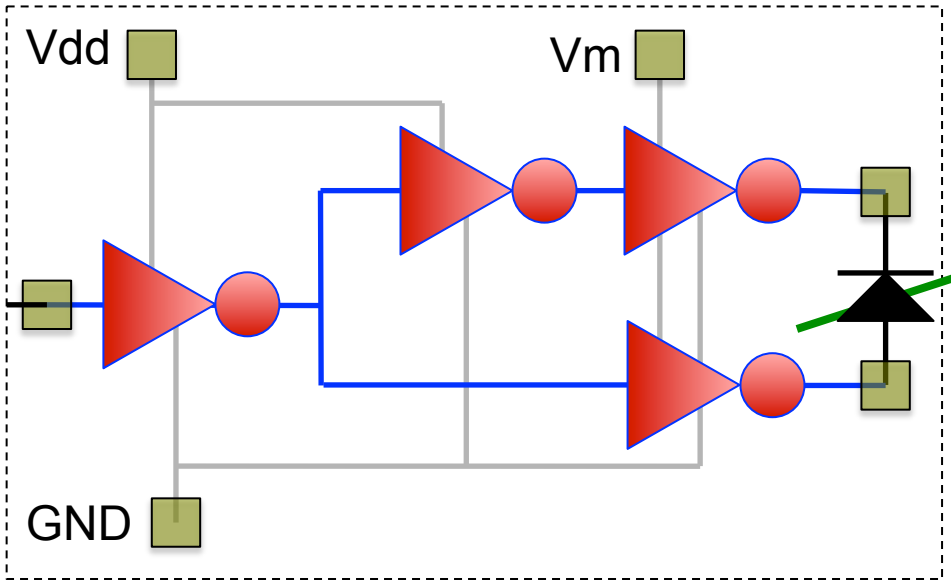
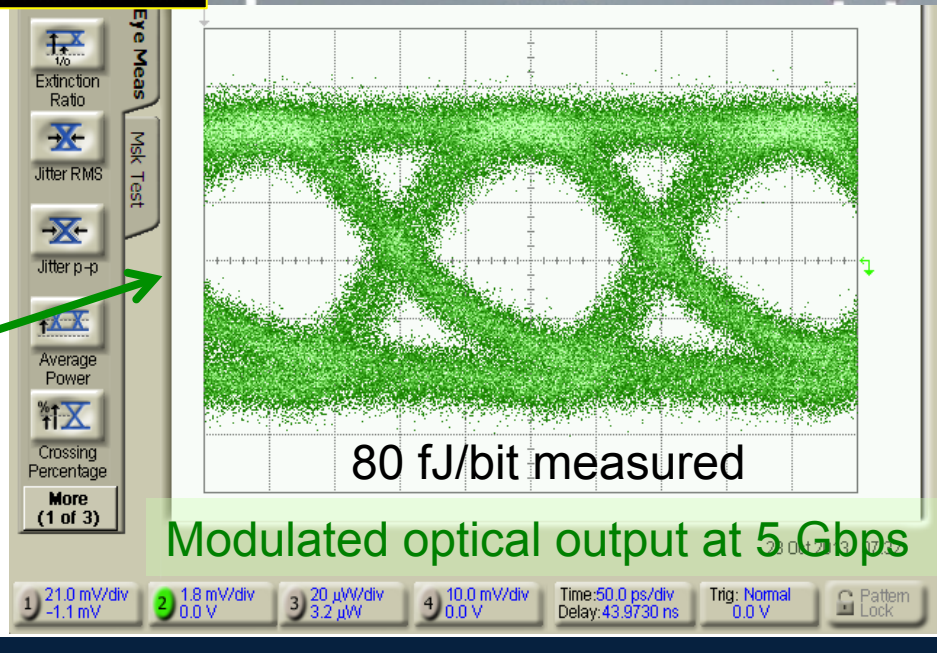






- Heterogeneous integration
  - Independent optimization of electronics & photonics
  - Challenge: Need high yields and small bond size

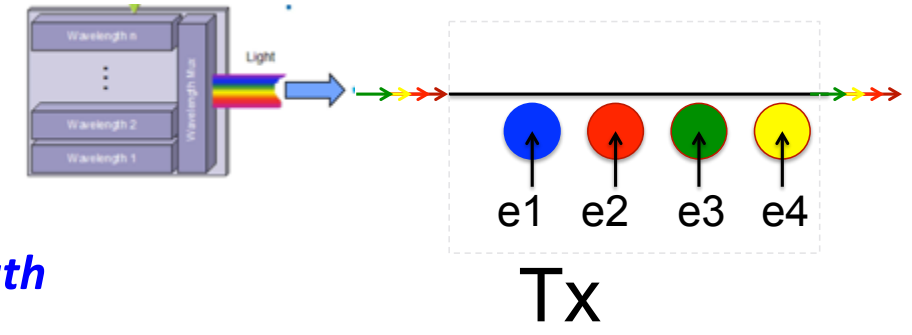


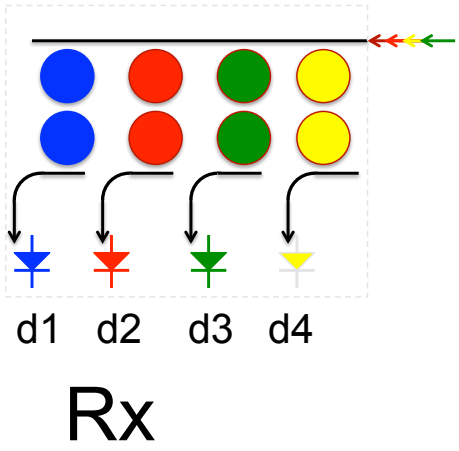


Technology Gaps

- Integration
  - ***Silicon photonics integration with state of the art CMOS with low capacitance and high yield***
  - Cost effective, reliable packaging
- Silicon Photonics
  - ***Low energy receivers***
  - ***Modulator and optical filter wavelength stability and uniformity***
  - *Fiber coupling and waveguide losses*
  - Efficient Laser source
- Interface Electronics
  - ***Efficient clock and data recovery***
  - Data TDM multiplexing (SERDES)
  - Efficient Data encoding and error correction

Focus on chip to chip interconnect





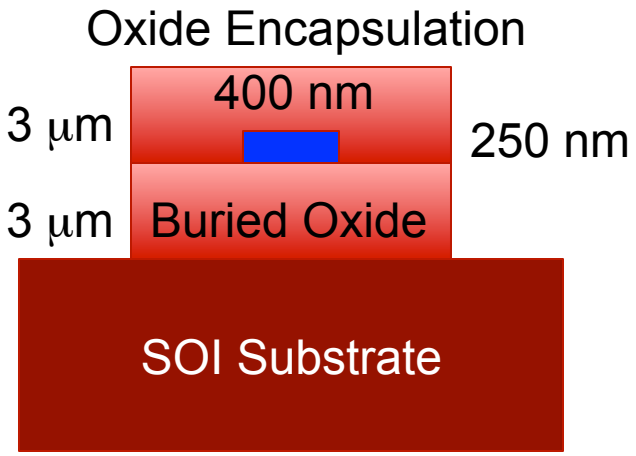
Focus of the talk

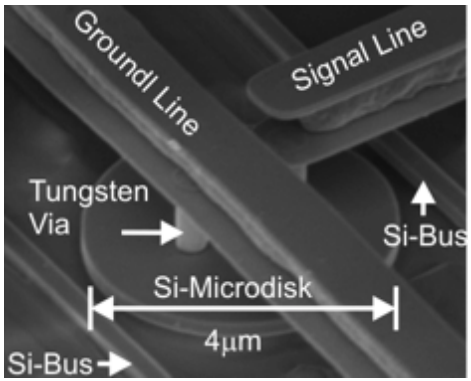
Sandia National Laboratories

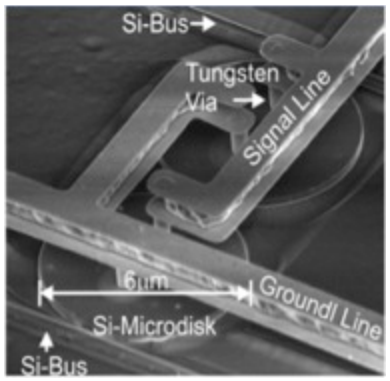
- ***Low energy receivers.***
  - ***Low capacitance detection.***
  - ***Ge on Si integrated detectors.***
- ***Modulator and optical filter wavelength stability and uniformity.***
  - ***Low energy modulators < 3 fJ/bit.***
  - ***Temperature stabilization for WDM systems.***

What is Silicon Photonics?

- Active and Passive Photonics on/in Silicon
- Passive:
  - Waveguides, spectral filters, splitters, polarizers, polarization rotators, gratings, isolators*
- Active:
  - Modulators(EO), switches, detectors (OE, Ge), lasers*
    - Thermal Shift of index
    - Electro-refraction
    - Electro-absorption (SiGe)
- Most applications require intimate integration with CMOS Electronics
  - Heterogeneous integration
    - Flip-chip bonding, Wafer bonding, etc.
  - Monolithic integration







Photos from M. R. Watts, Zortman, Trotter, Young, Lentine, Optics Express, 22, (2011)

SNL Photonics Fabrication

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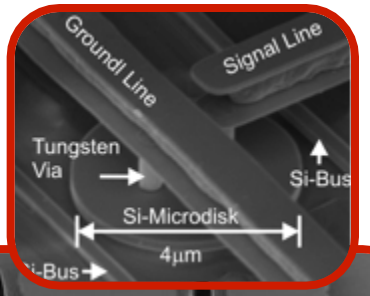
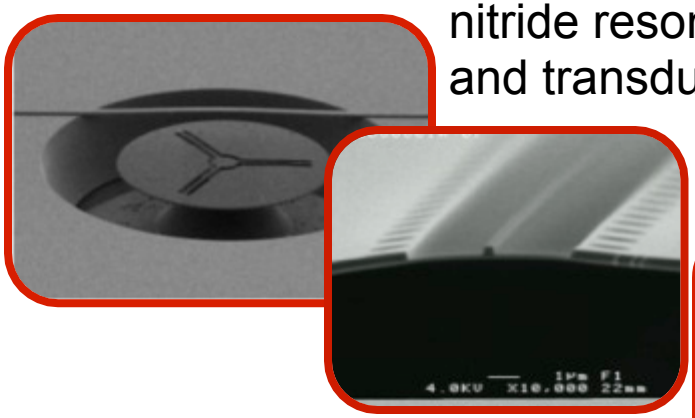
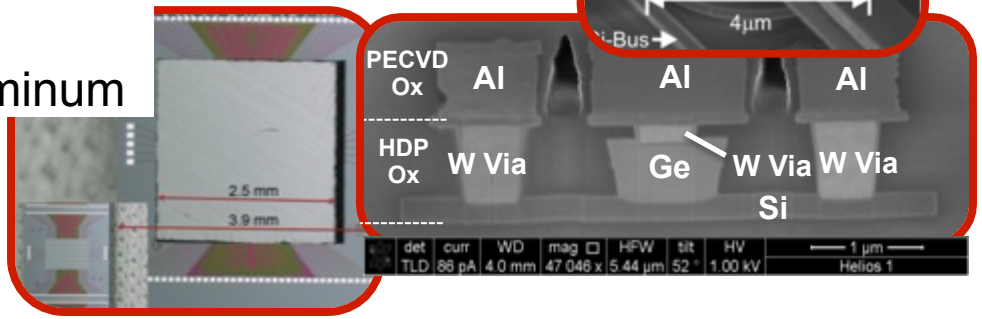
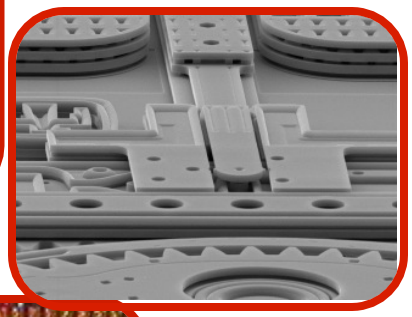
- Low-energy modulators[1], detectors[2], low-loss waveguides, SiN edge couplers, travelling wave Mach-Zehnder modulators, grating couplers, advanced CMOS flip-chip / direct CMOS integration



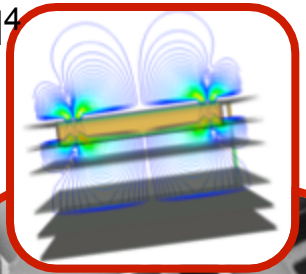
- Suspended Si/SiN resonators phononic/photonic crystals[3], aluminum nitride resonators and transducers.



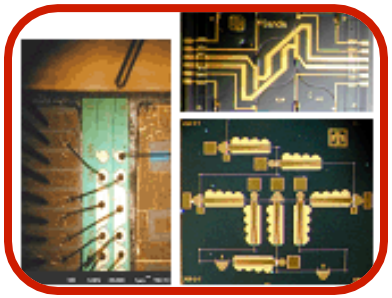


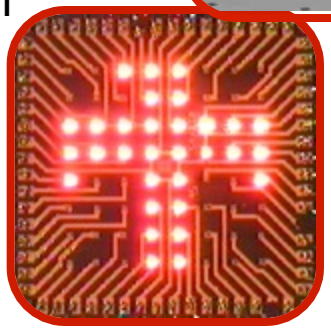


- Near to long-wave IR plasmonics and metamaterial[4] based devices.

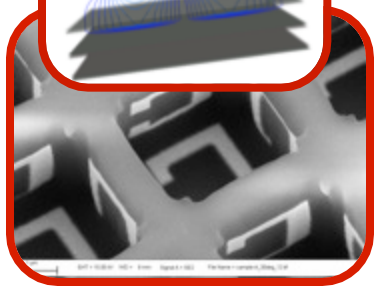


- Compound semiconductor devices and fabrication





- MEMS processing

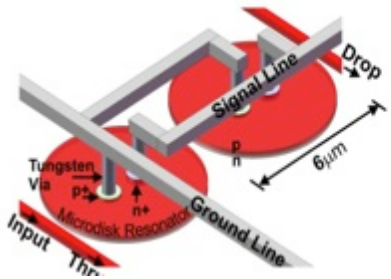


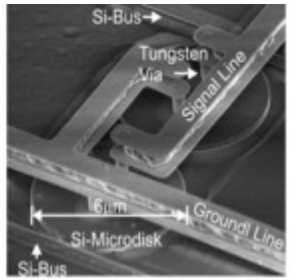
[1]M.R. Watts, et al. OPEX **19** 21989 (2011)
[2]C.T. DeRose, et al. OPEX **19** 24897 (2011)
[3]P.T. Rakich, et al. Nature Comm. **4** 1 (2013)
[4]D.B. Burckel, et al. Advanced Mat. **22** 5053 (2010)

Silicon Photonics at SNL

Sandia National Laboratories

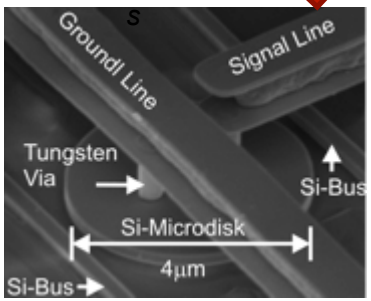
Free-carrier Effect (high-speed)

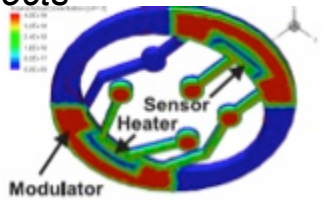


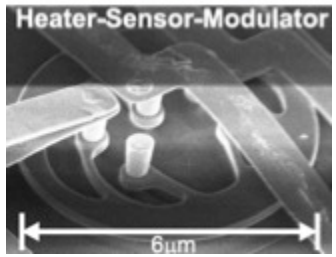


Fast Reconfigurable Interconnects

3.2fJ/bit at 12Gb/s





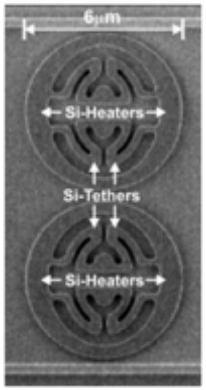


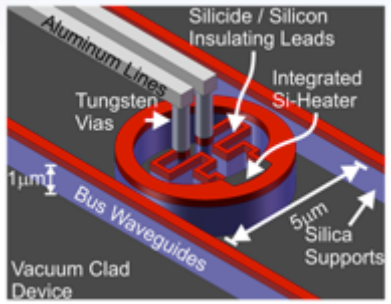
Resonant Optical Modulator/Filter

Thermally stabilized modulator

Broadband Mach-Zehnder Filter/Switch

Thermal Optic Effect (wide-band)

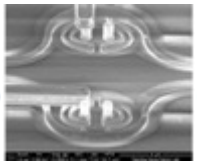




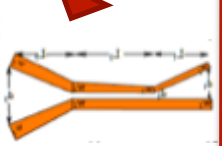
Tunable Resonant Filter

Thermo-optic Phase Shifter

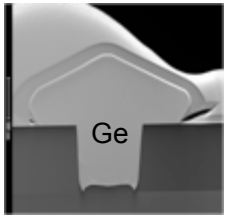
Adiabatic Splitter



Switch Arrays

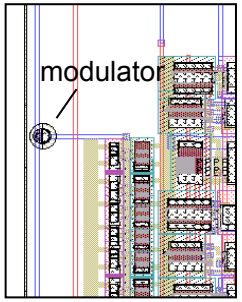


High-speed Ge Detector in

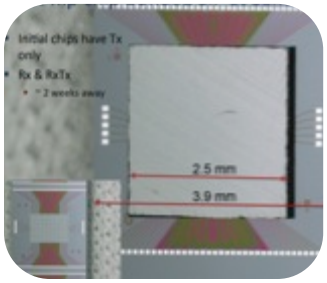


45GHz, 3nA dark current

Photonics-CMOS Integration

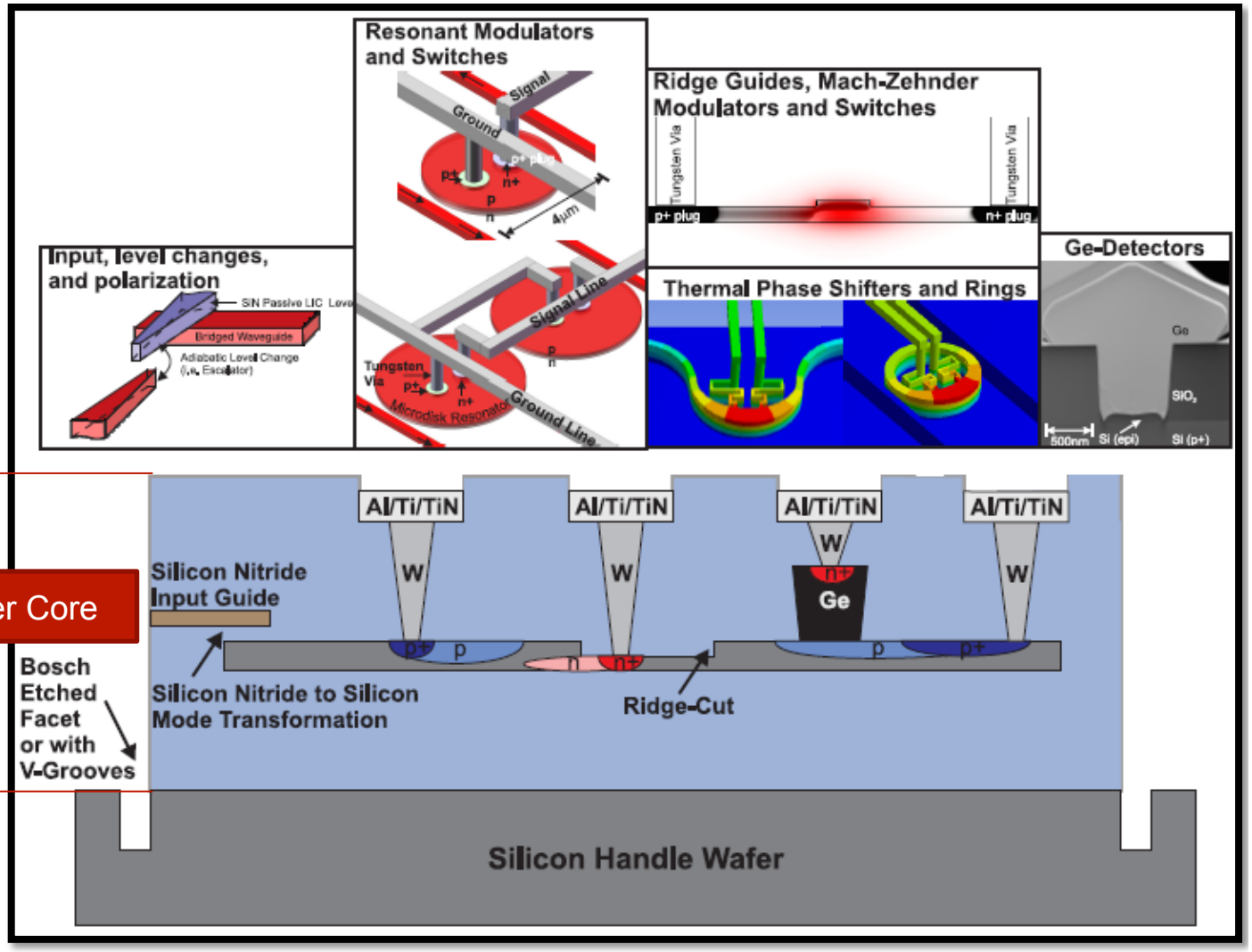


Flip-Chip Bonding



Si Photonics cross-section

Sandia National Laboratories



Off-chip laser

Fiber Core

Ge in Modern CMOS

Germanium old semiconductor technology.

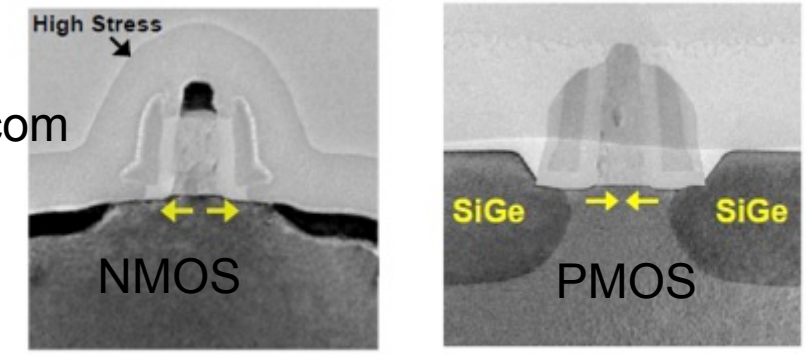
- Indirect Bandgap at 0.66 eV.
- Direct Bandgap at 0.8 eV (1550 nm) in telecom band.
- Not efficient optical emitter.

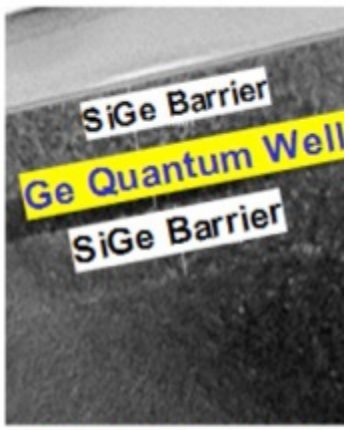
Selective epitaxial growth of Ge on Si has enabled advanced strain engineering in modern CMOS.
Fully CMOS Compatible.
High electron and hole mobilities.

Ge optoelectronics: direct bandgap at 1550nm implies good absorption.

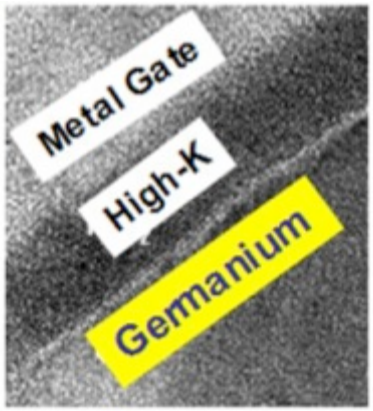
Strain engineering in CMOS

Intel 45nm





Ge Quantum-well

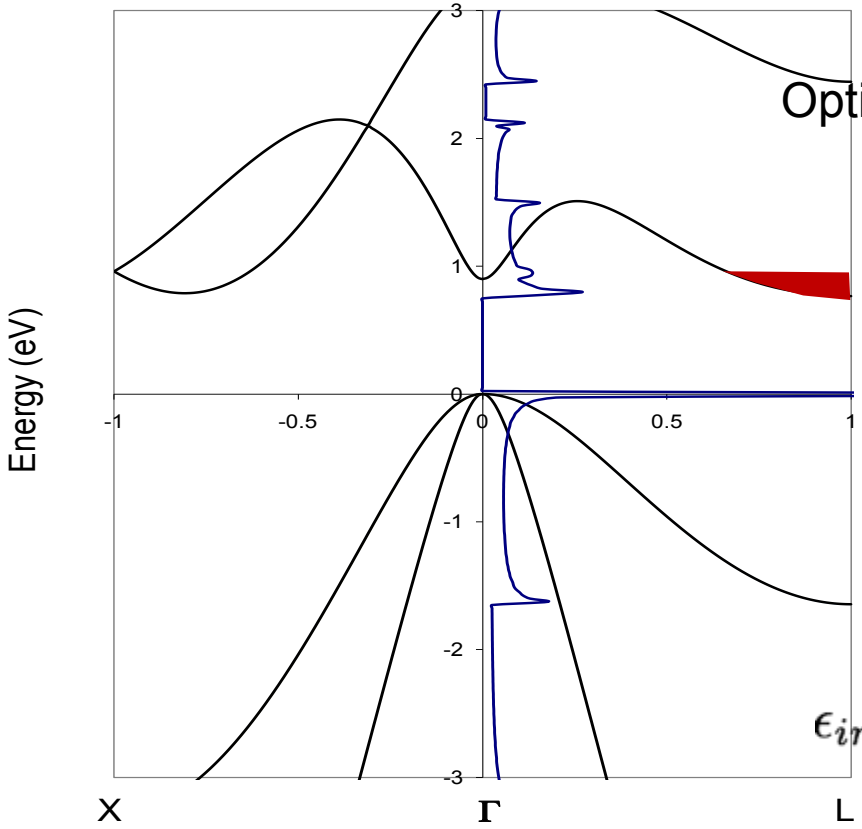


Ge MISFET Transistor

Sources: (1) ESSDERC 2008, (2) www.intel.com/silicon research/R&D pipeline

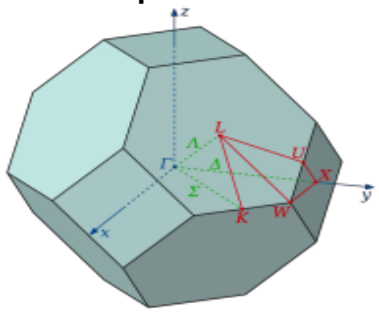
Optical Properties of Germanium

Tight binding band-structure



Can we determine validity of band-filling and strain models for PL & EL signatures?

Optical Properties of Heavily Doped Semiconductor



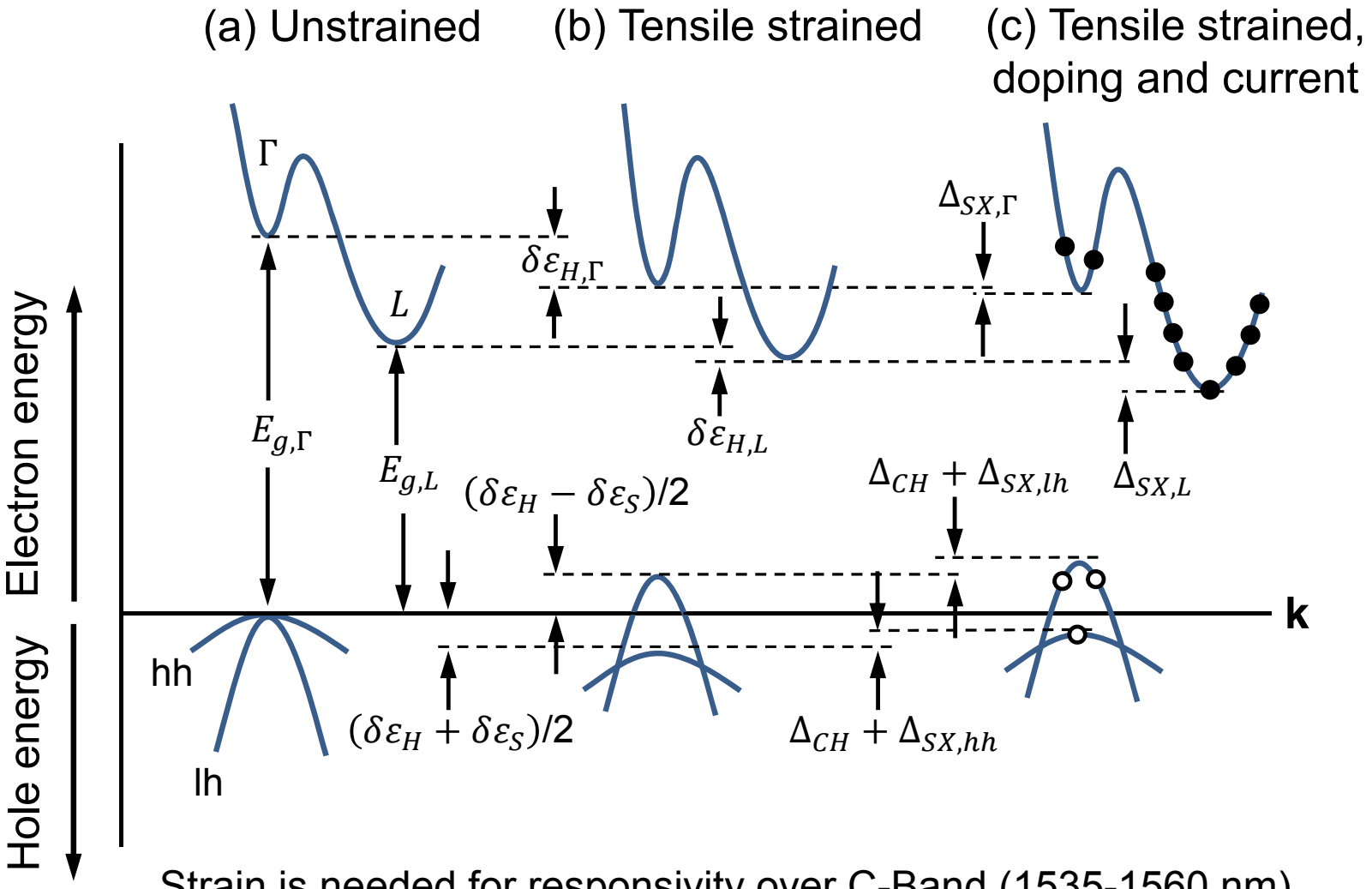
J. Jung, T. G . Pederson, JAP,113,114904,(2013)

$$\epsilon(\omega) = \epsilon_{inter}(\omega) + \epsilon_{intra}(\omega)$$

$$\epsilon_{intra}(\omega) = \frac{e^2}{8\pi^3\epsilon_0\hbar^2\omega^2}\sum_n \int \frac{\partial E_{n\mathbf{k}}}{\partial \mathbf{k}} f'(E_{n\mathbf{k}})d\mathbf{k}$$

$$\epsilon_{inter}(\omega) = 1 + \frac{e^2\hbar^2}{8\pi^3\epsilon_0 m^2}\sum_{n\neq m} \int \frac{f(E_{n\mathbf{k}}) - f(E_{m\mathbf{k}})}{E_{m\mathbf{k},n\mathbf{k}}[E^2_{m\mathbf{k},n\mathbf{k}} - (\hbar\omega)^2]} M_{m,n}(\mathbf{k})d\mathbf{k}$$

Indirect Bandgap in Strained Ge



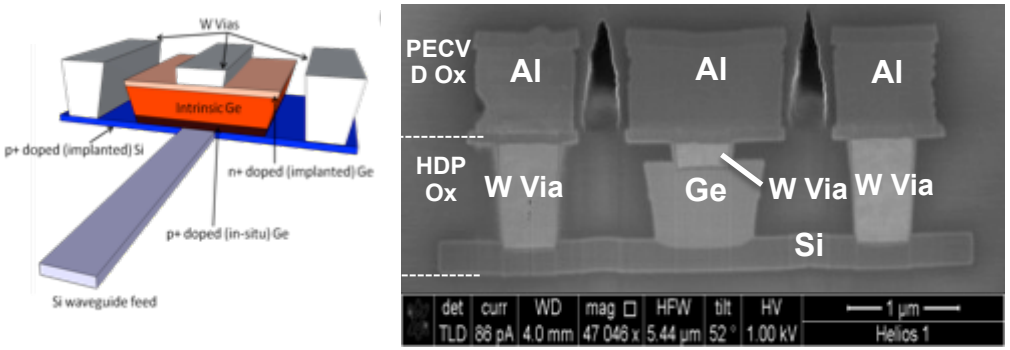
Strain is needed for responsivity over C-Band (1535-1560 nm).

Ge on Si Detector Development

Sandia National Laboratories

Compact high speed photodiode

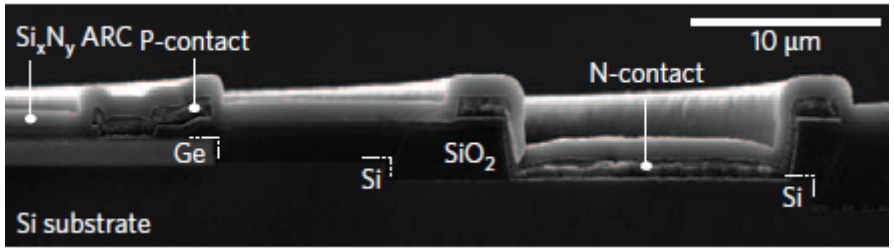
Sandia



5 December 2011 / Vol. 19, No. 25 / OPTICS EXPRESS 24897

Ge on Si Avalanche Photodiode

Intel, UCSB, UVa



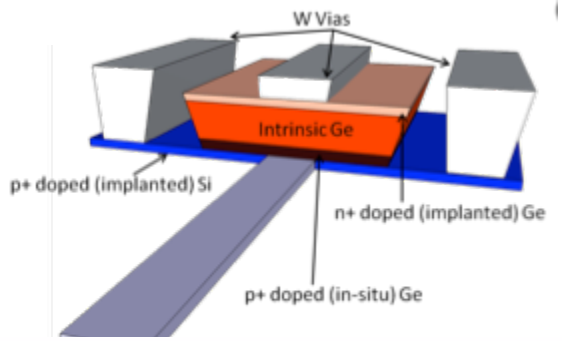
NATURE PHOTONICS | VOL 3 | JANUARY 2009 | www.nature.com/naturephotonics

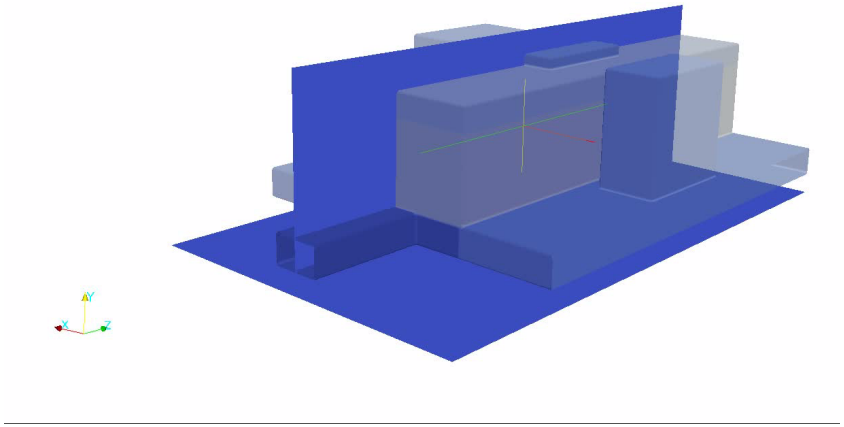
- Integrated waveguide Ge on Si photodetector demonstrated best in class performance.
- Ge on Si linear mode separate absorption multiplication avalanche photodiode demonstrated 340 GHz gain bandwidth product.
- **Combining new device concepts would enable integrated single photon detection and launch Quantum Si Photonics.**

Waveguide Coupled Ge Photodetector

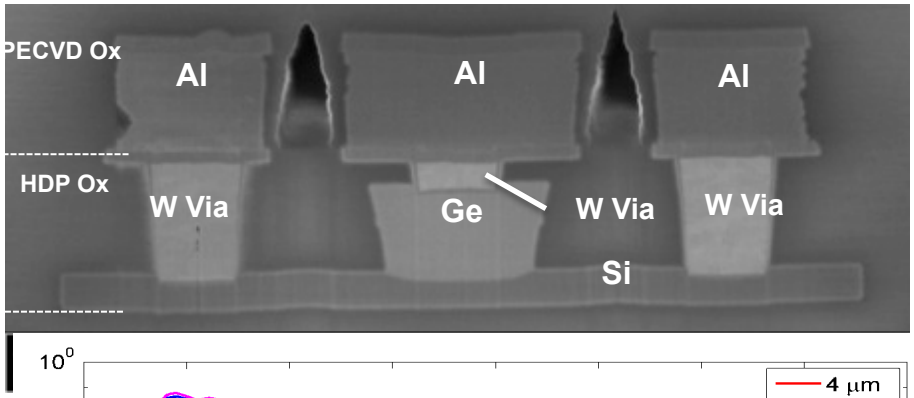
Sandia National Laboratories

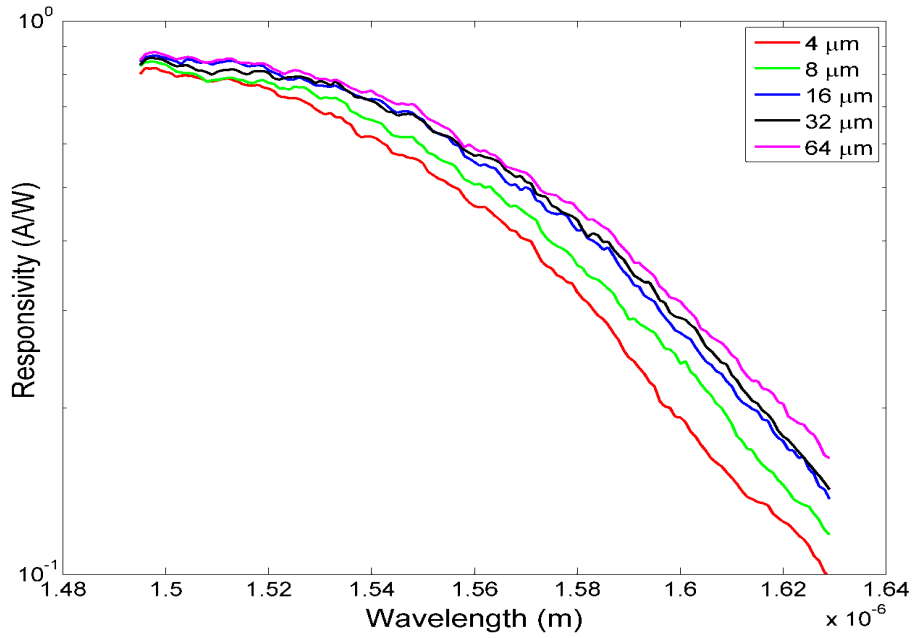
Ultra-low capacitance photodetector ~ 1fF



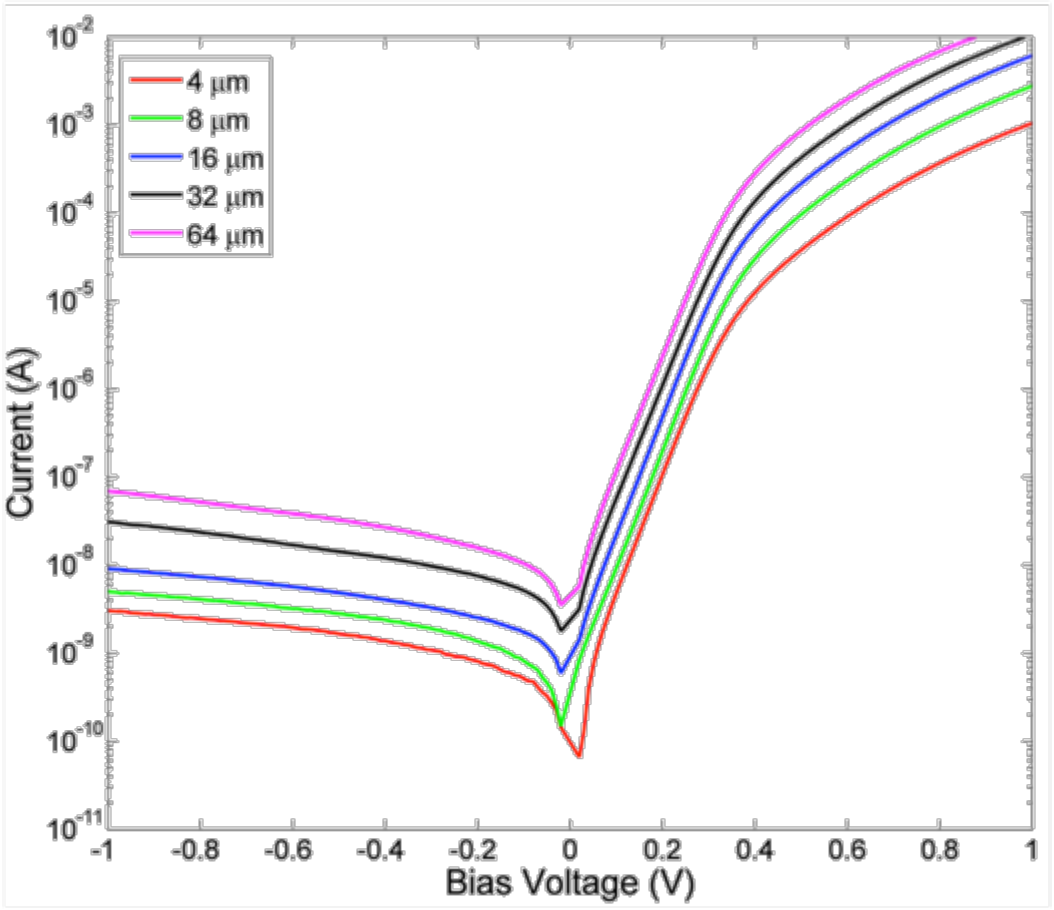


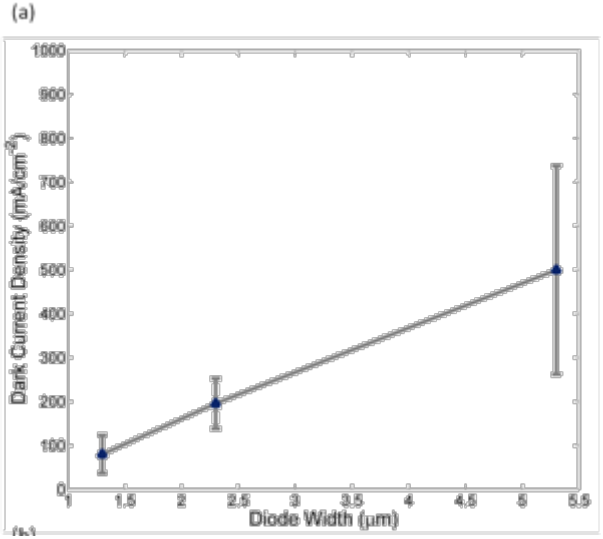
Fully processed waveguide coupled Ge detector





Low Dark Current Ge Photodetector

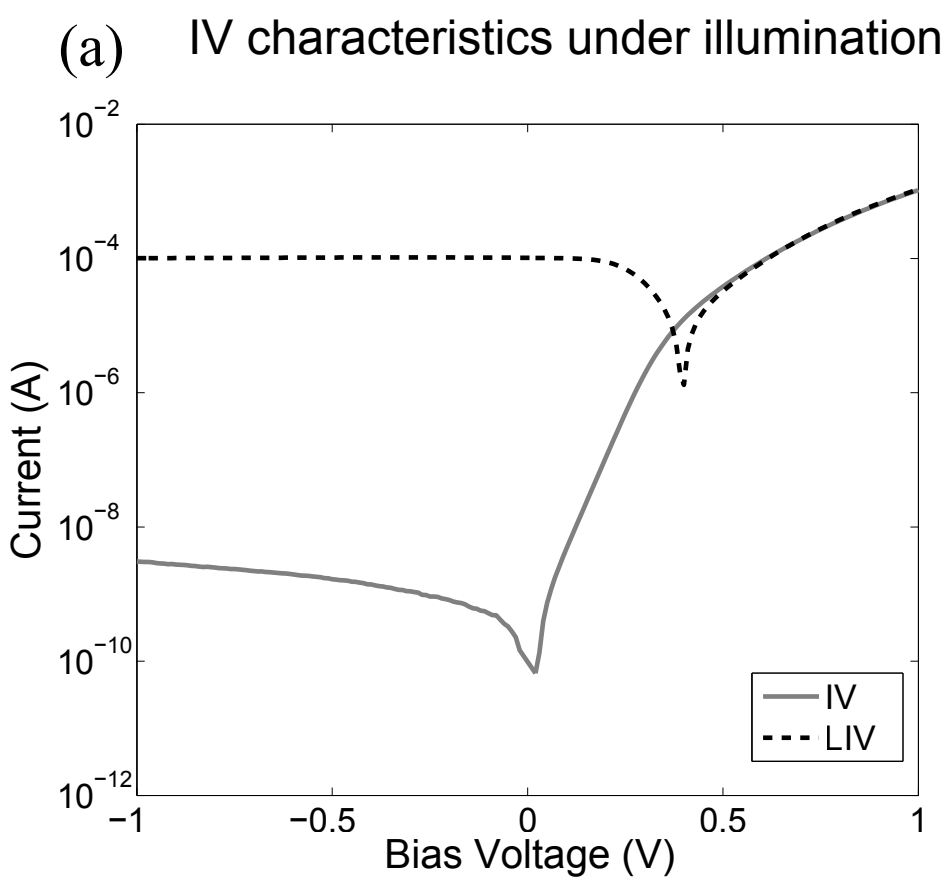


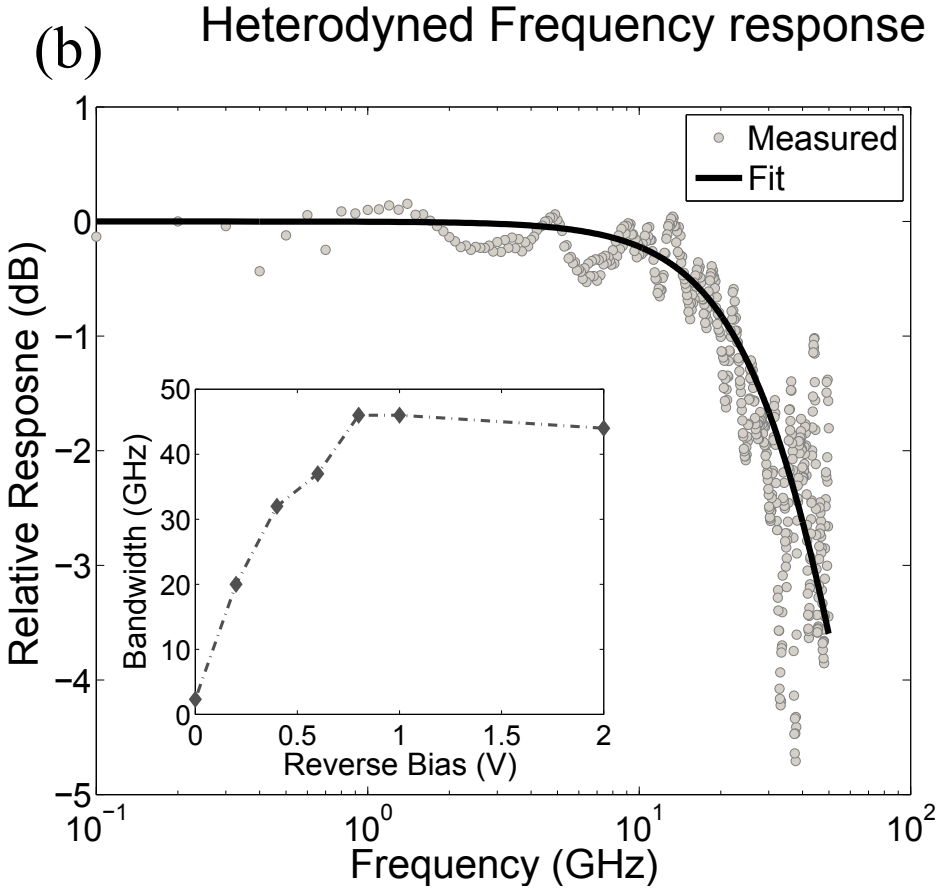


3 nA dark current in smallest area Detector.

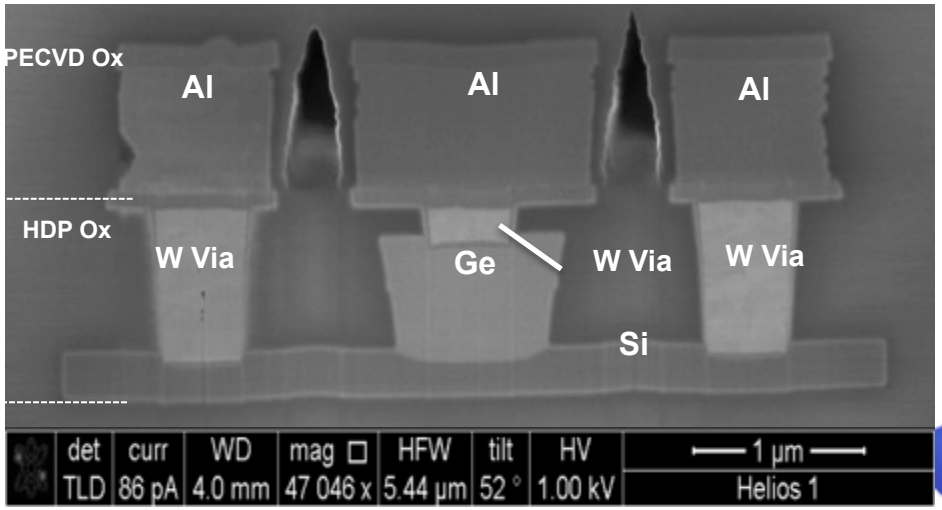
Dark current scales as Si/Ge interface
Area.

45 GHz 3dB Frequency Response

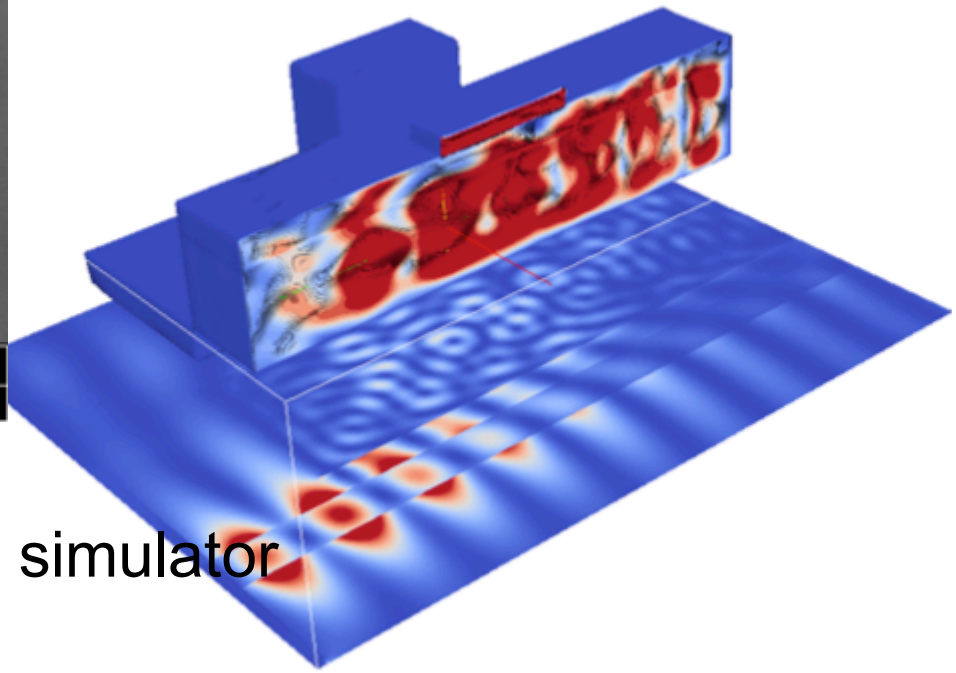




Ge Photodetector Development



Generation rate

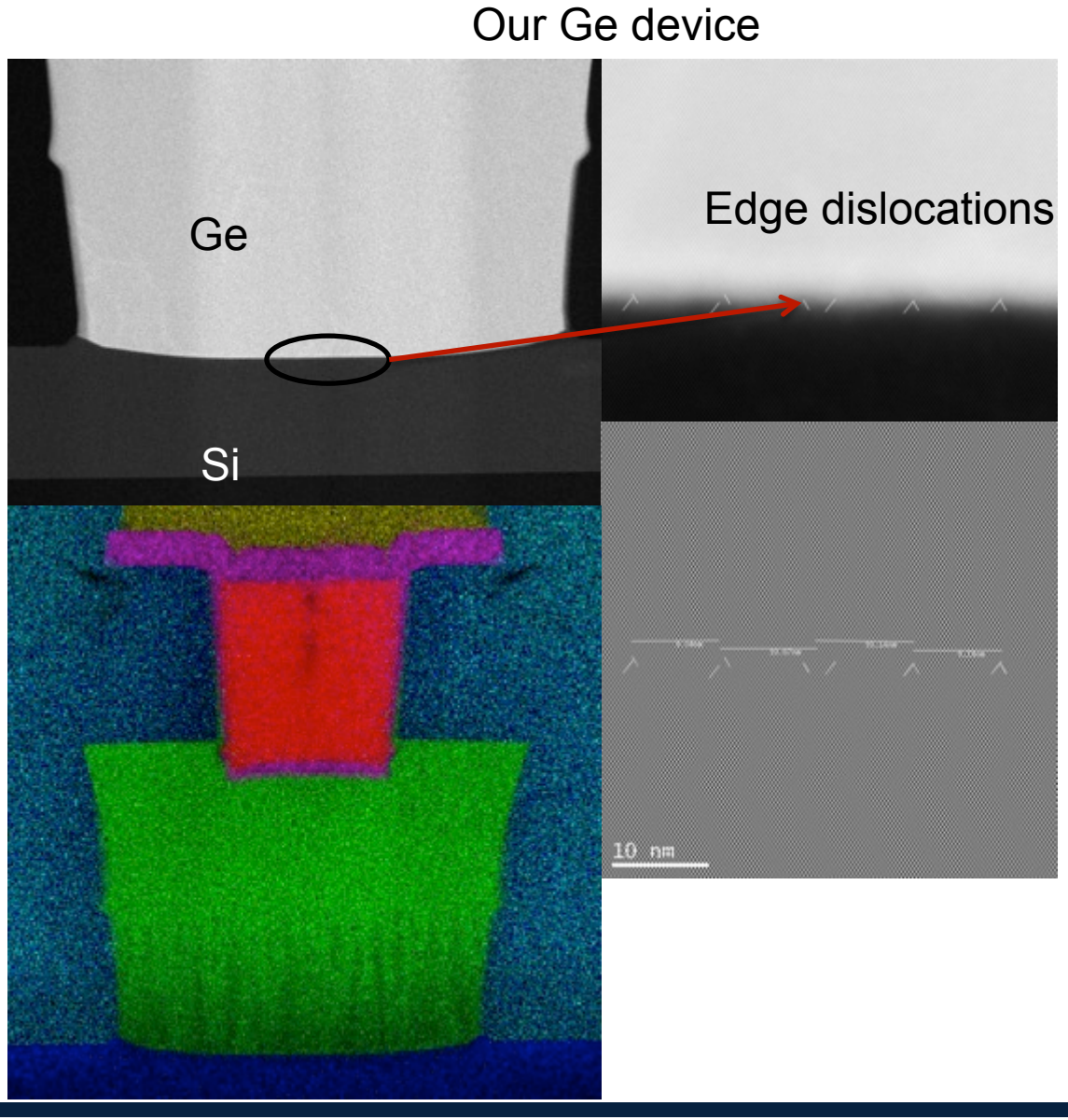


Input Generation rate into Device simulator Synopsis drift-diffusion.

C. T. DeRose, D. C. Trotter, W. A. Zortman, A. Starbuck, M. Fisher, M. R. Watts, and P. S. Davids, "Ultra compact 45GHz CMOS compatible Ge waveguide photodiode with low dark current," *Optics Express*, vol. 12, no. 25, p. 24897, 2011.

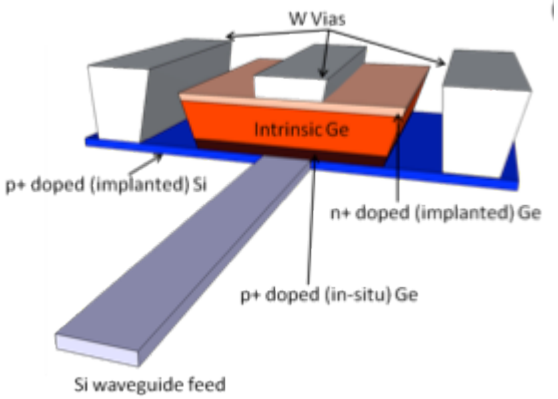
Low Dark Count Detection

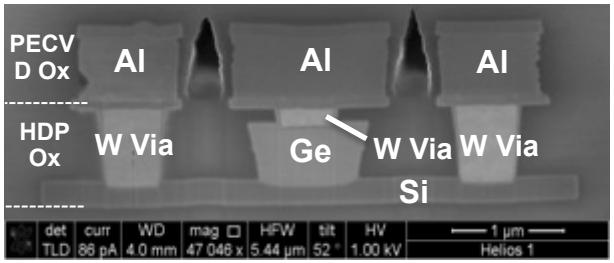
- Selective Ge on Si gives low defect count at Si/Ge interface.
- We need to reduce dark current.
- Apply analytic tools to reduce defects at interface.
  - Very low defect density.
- Field engineering, cooling, and vertical designs must reduce dark current levels.

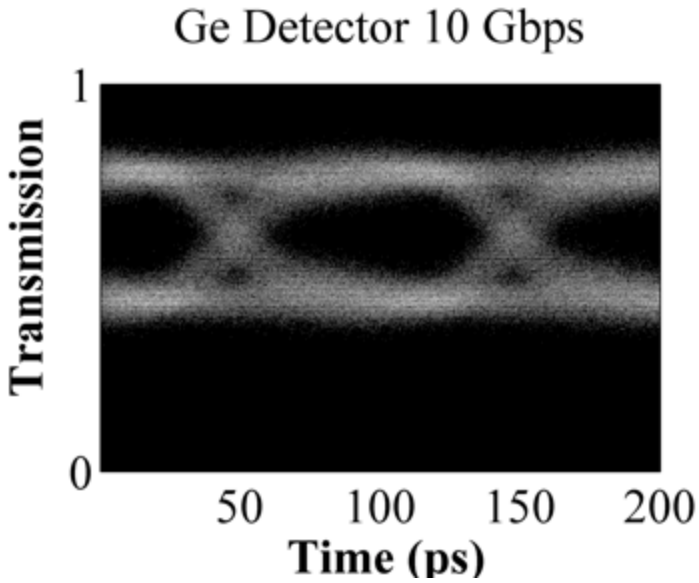


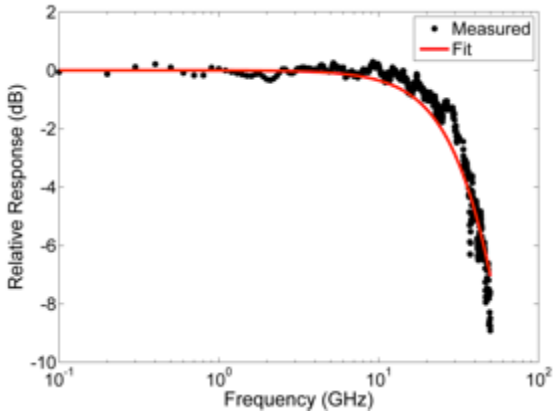
Integrated Germanium Detectors

- **Operation at 10 Gbps**
  - **equipment limited**
- **Frequency response ~ 45 GHz**
- **~ 0.8 A/W responsivity at 1540 nm**
- **< 100 nA dark current at 1 V**



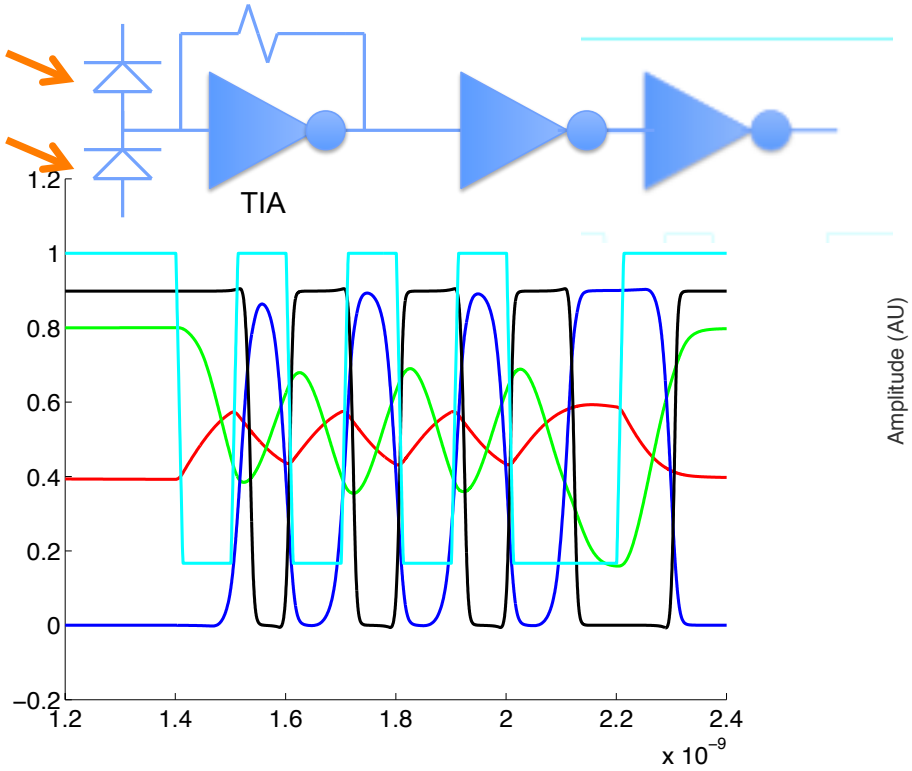


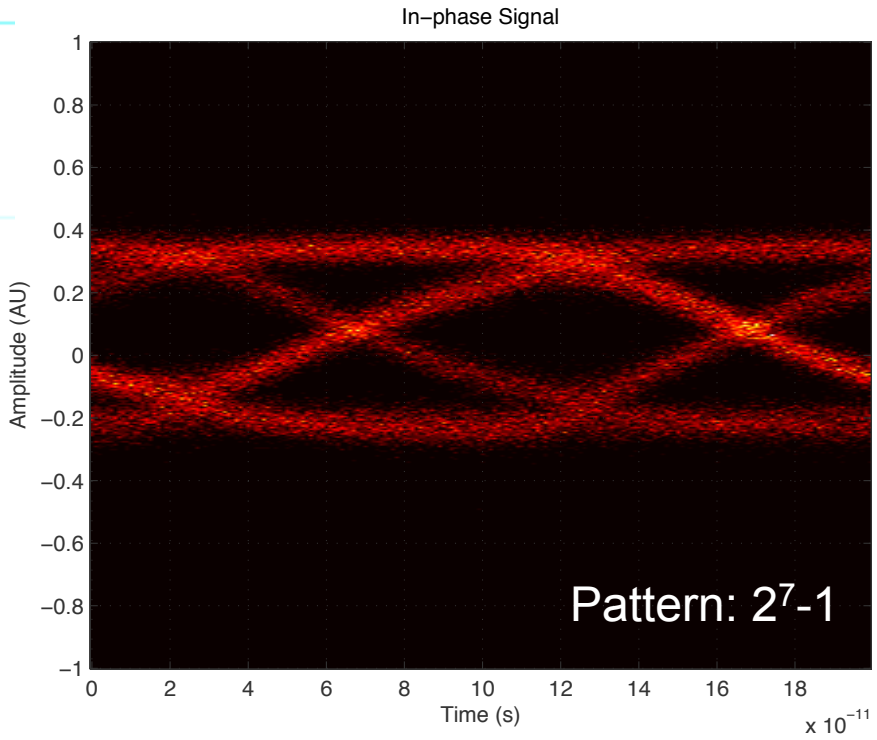




C. T. DeRose, et. al., Optics Express, 2011

Receiver Energies (*Simulation*)



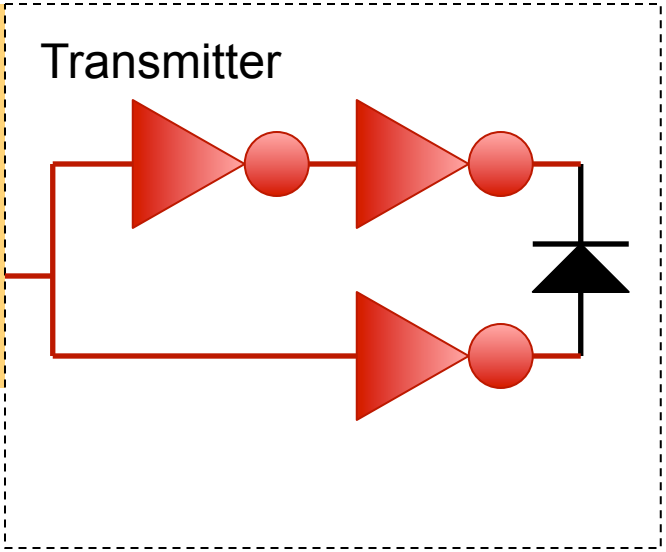


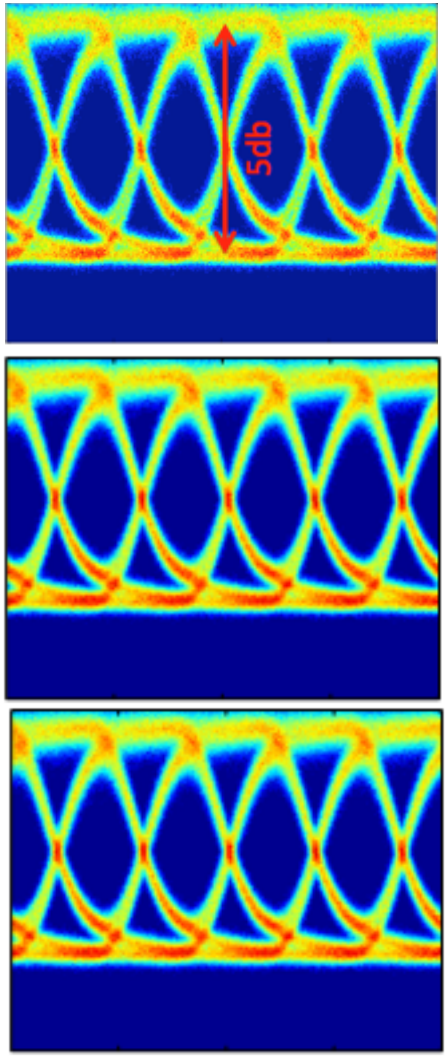
Bit Rate = 10.00Gbps, *Energy per bit = 2.74fJ*

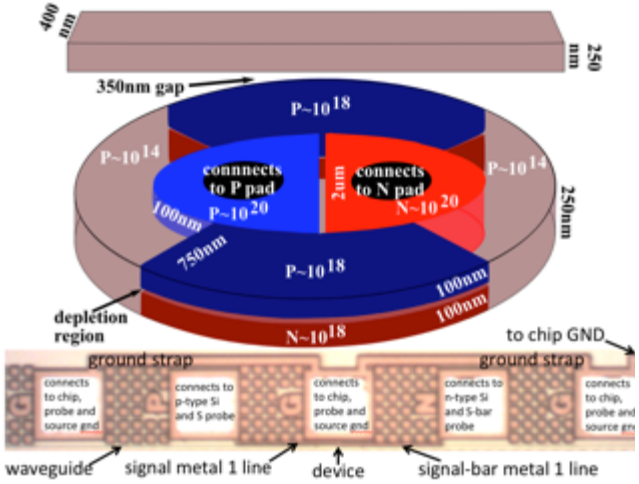
- 45 nm technology node,
- 20k transimpedance, 10 fF Total input capacitance
- -20 dBm (average) signal level (6:1 extinction)

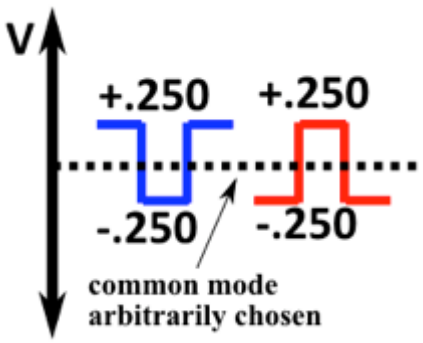
Simple Modulator Driver: Differential Signaling

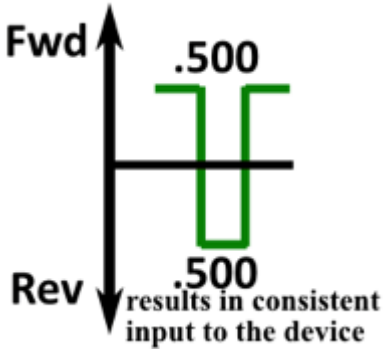
- No pre-emphasis
- No AC coupling
- No high voltages
- CMOS logic levels











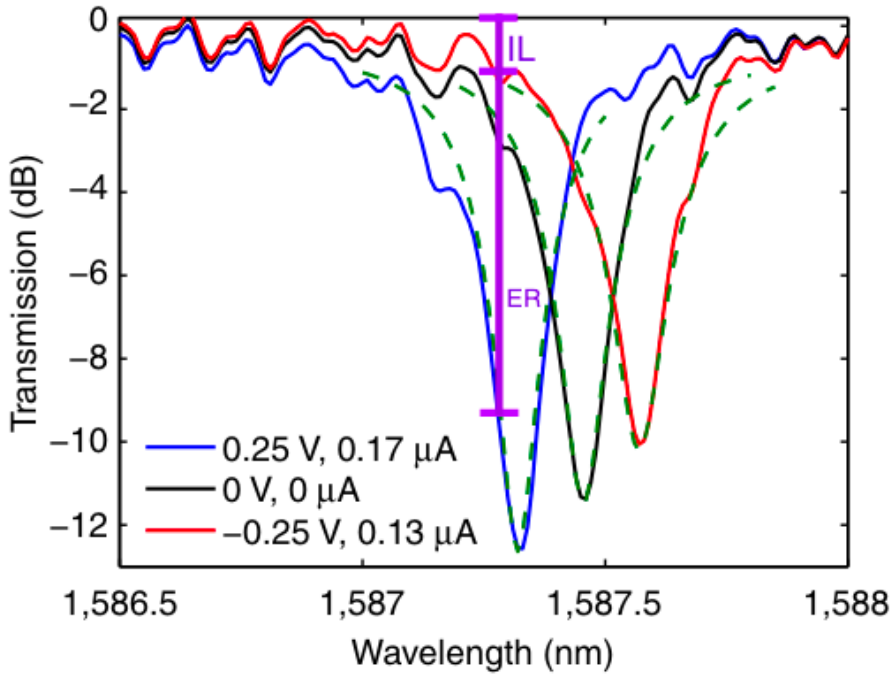
- **10 Gb/s**
- **Common Mode:**
- **.25V, .8V, 1.2V**
- **3 fJ/bit**

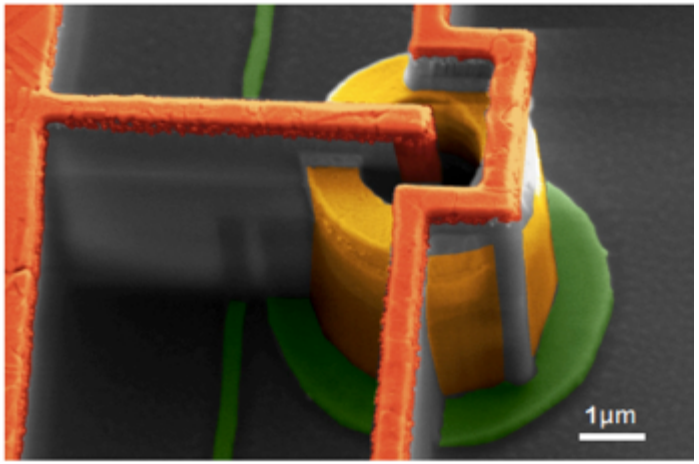
W. A. Zortman, A. L. Lentine, D. C. Trotter, and M. R. Watts, 'Low-voltage differentially-signaled modulators,' Opt. Express **19**, 26017-26026 (2011)

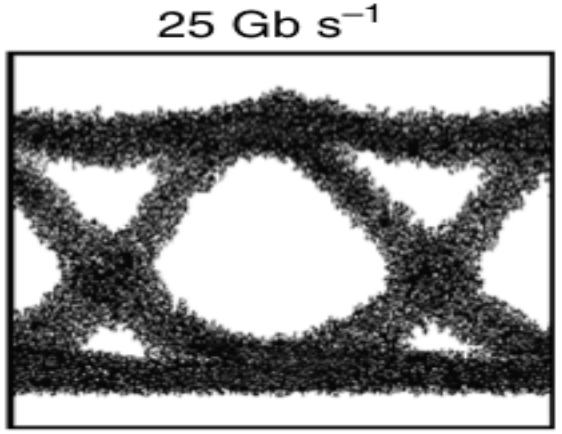
Highly doped-disk modulator (MIT)

E. Timerdogan et. al.,Nature Comm. (6) 2014

- Very high doping for maximum charge transfer as a function of voltage
- C=15 fF, R=400 (25GHz); 0.9 fJ/bit



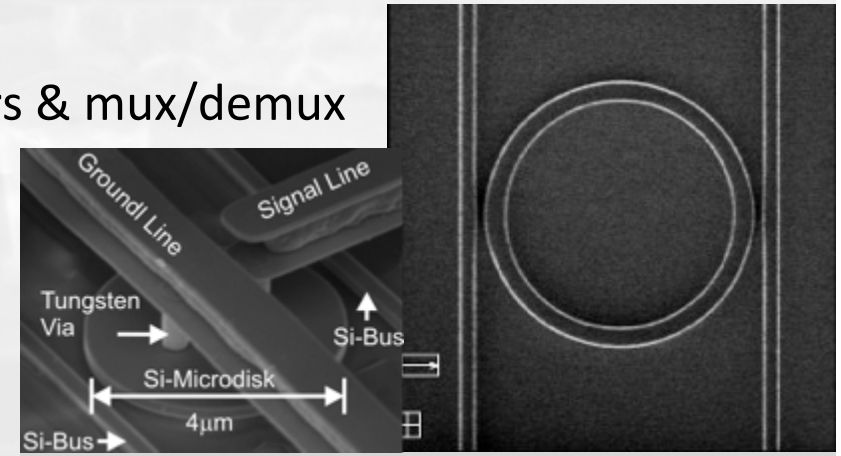


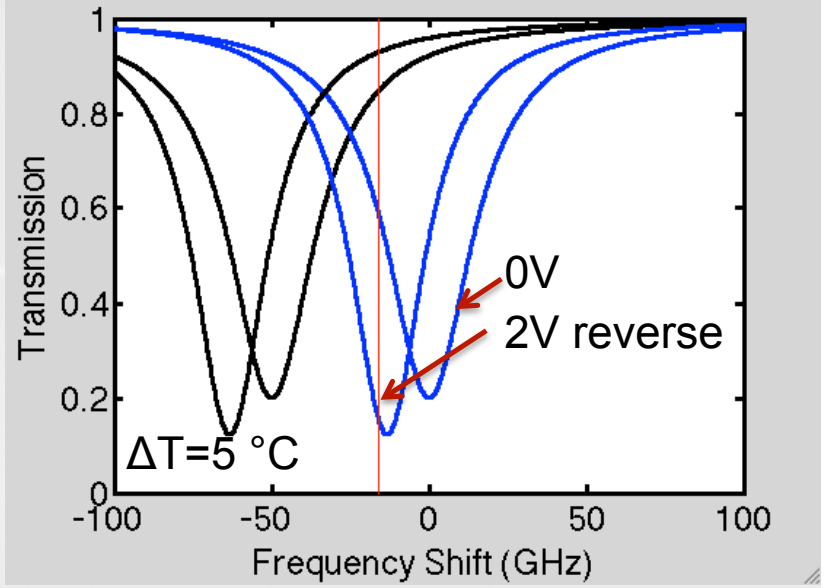


ER= 6.18 dB
IL= 1.02 dB

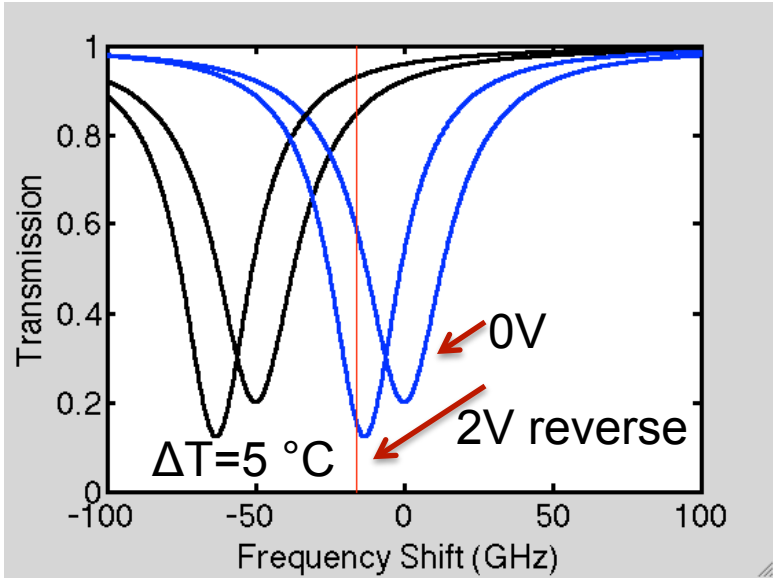
Resonant silicon micro-photonics

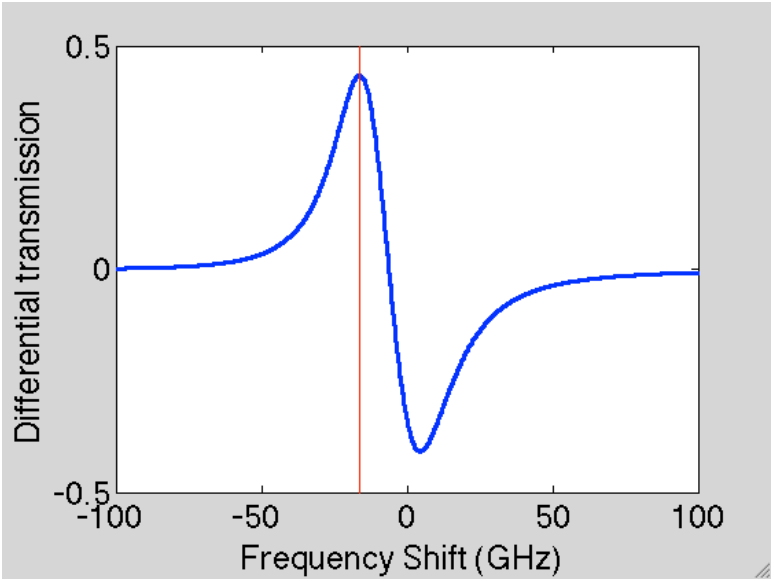
- Why resonant silicon photonics?
  - Small size (<4 um dia.)
  - Resonant frequency → DWDM modulators & mux/demux
- Benefits
  - Low energy
  - High bandwidth density
- Resonant Variations
  - Manufacturing Variations
  - Temperature Variations
  - Optical Power (1s density)
  - Aging?
- Requirements:
  - Resolution: +/- 0.25 °C (depending)
  - Range: 0 – 85 °C (depending)

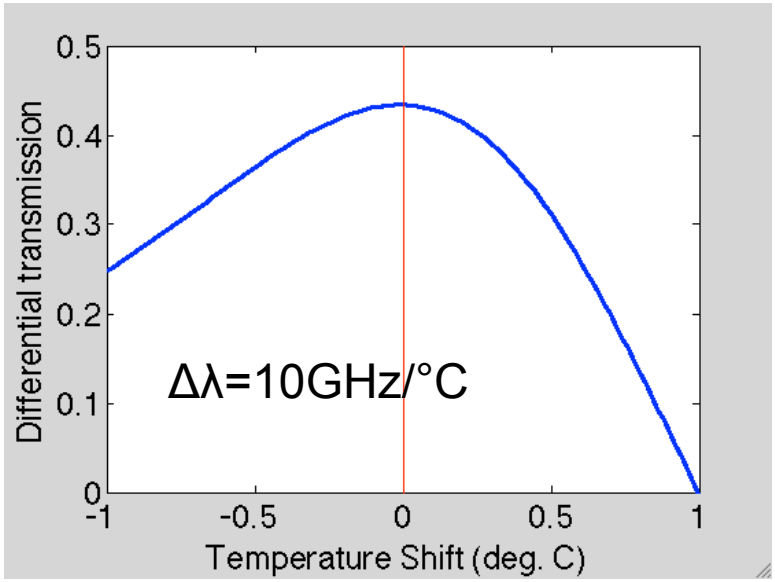


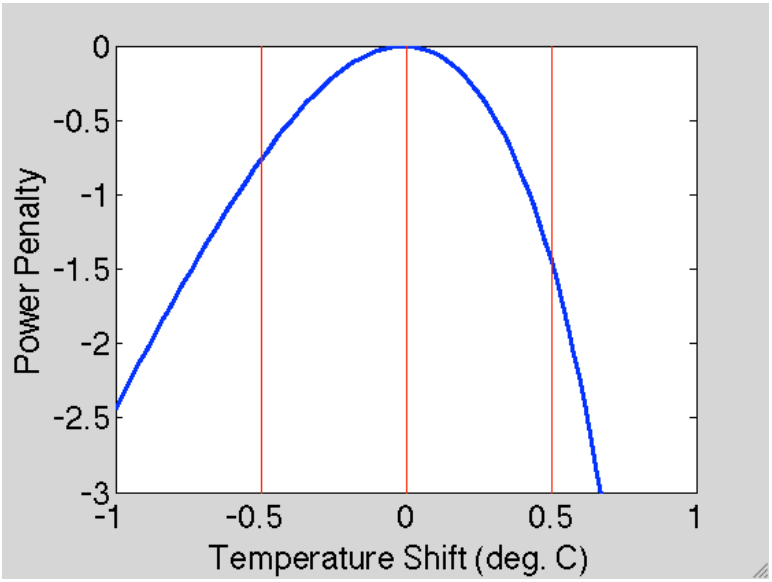


Effect of temperature on loss budget

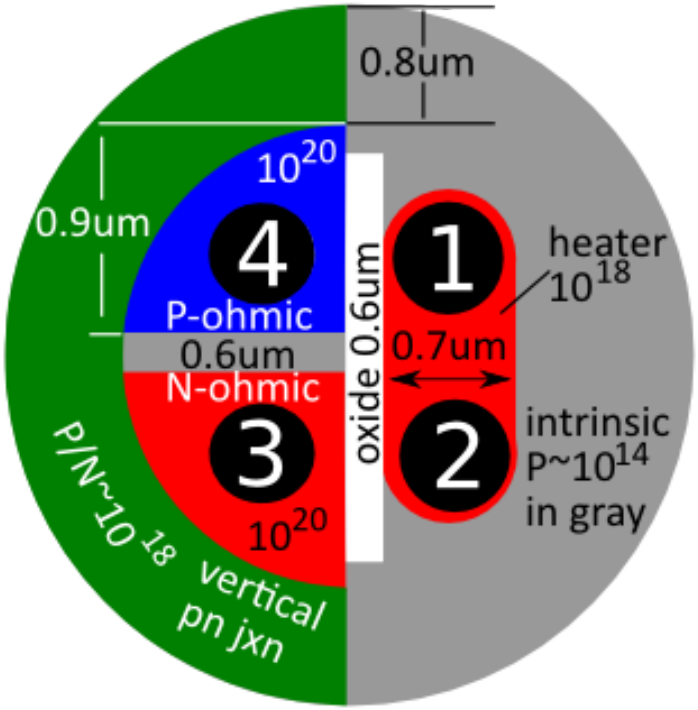


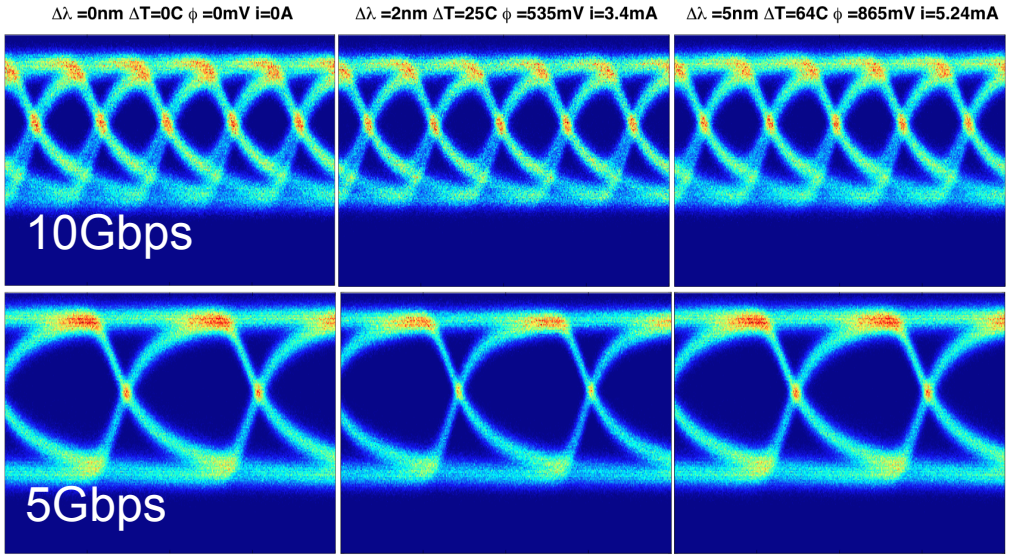


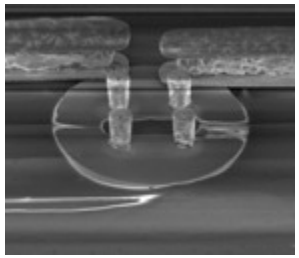




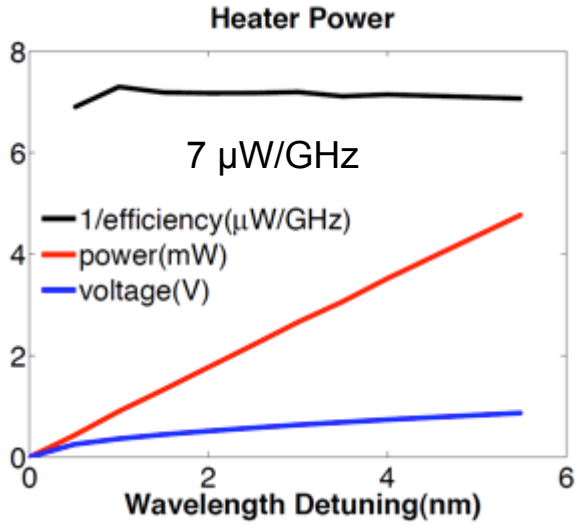
Silicon Photonics Modulator with integral micro-heater

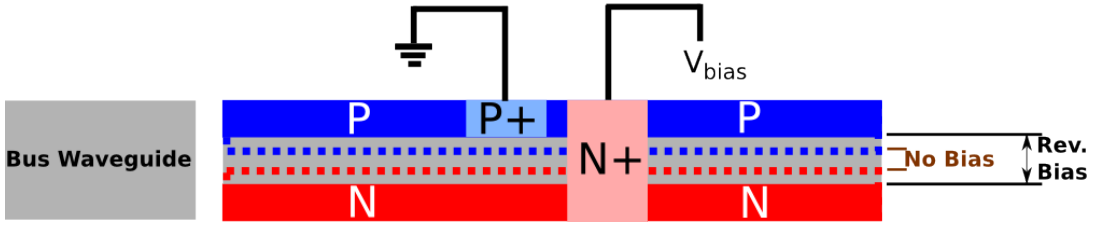






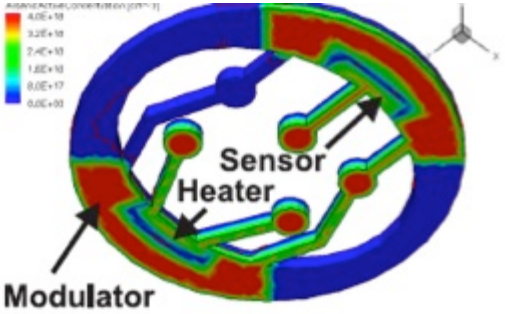
Δλ=2nm Δλ=5nm

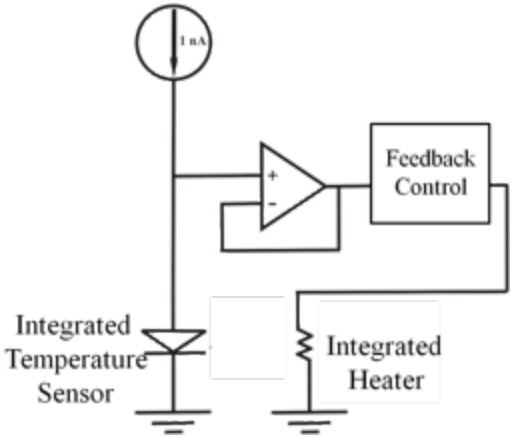


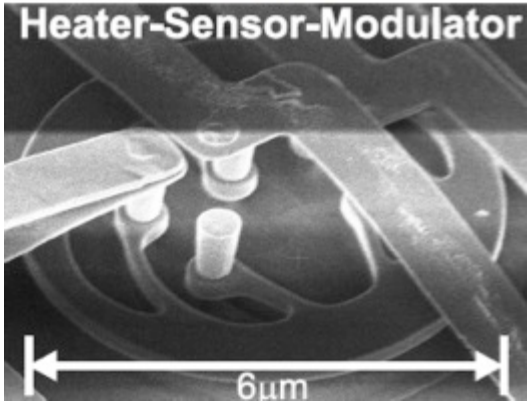


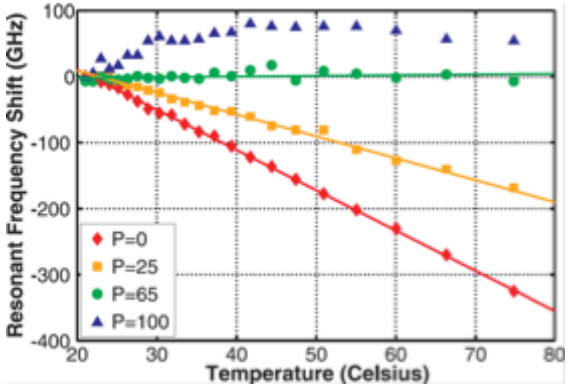
Temperature Sensor (Sandia)

- First attempt at resonant wavelength control
- Integral temperature sensors (diode)
- Sensor not independent of background temperature
- More complex device
- Not measuring other wavelength shifting affects
- Simple electronics (PI loop with P=constant)



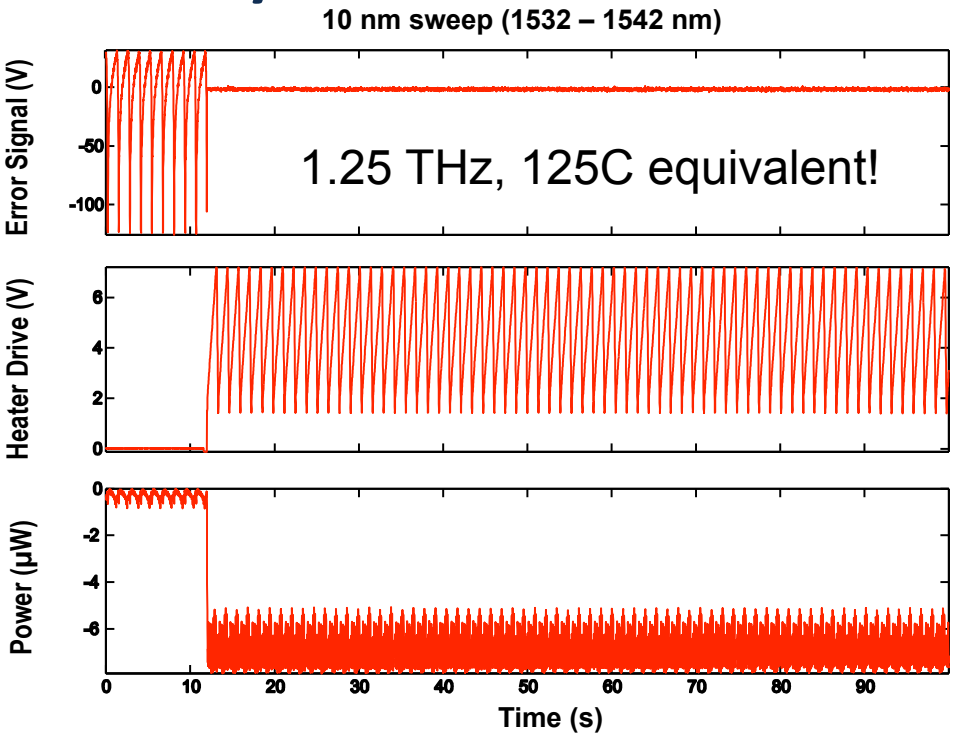


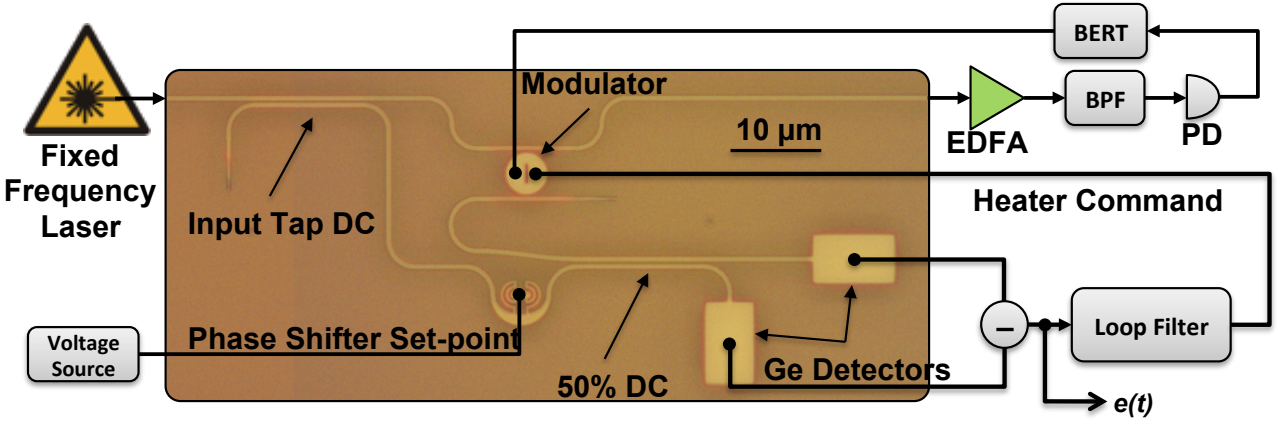


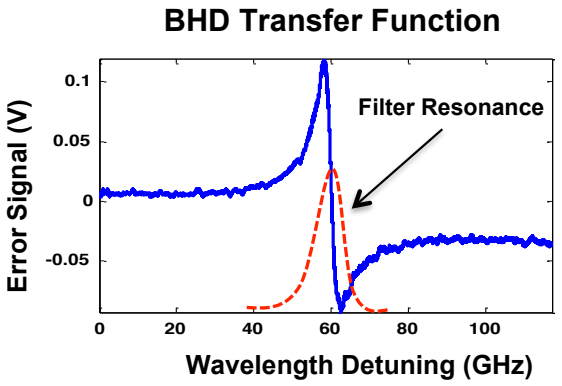


Modulator Stabilization System

- ***Lock to zero:*** No calibration or reference level needed for locking
- ***Amplitude insensitive:*** Locking point not influenced by optical intensity
- ***Precision locking:*** Resonator is not disturbed
- ***Minimum circuit complexity:*** Power and area consumption of control electronics is minimized

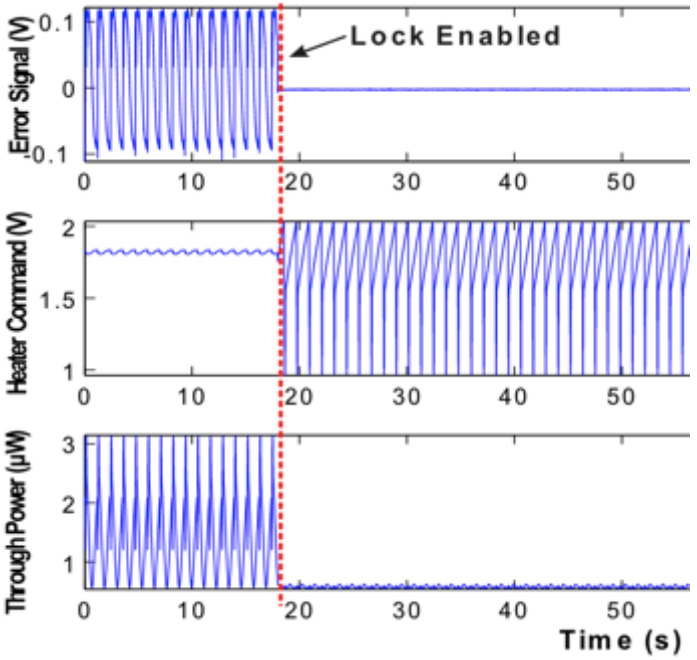


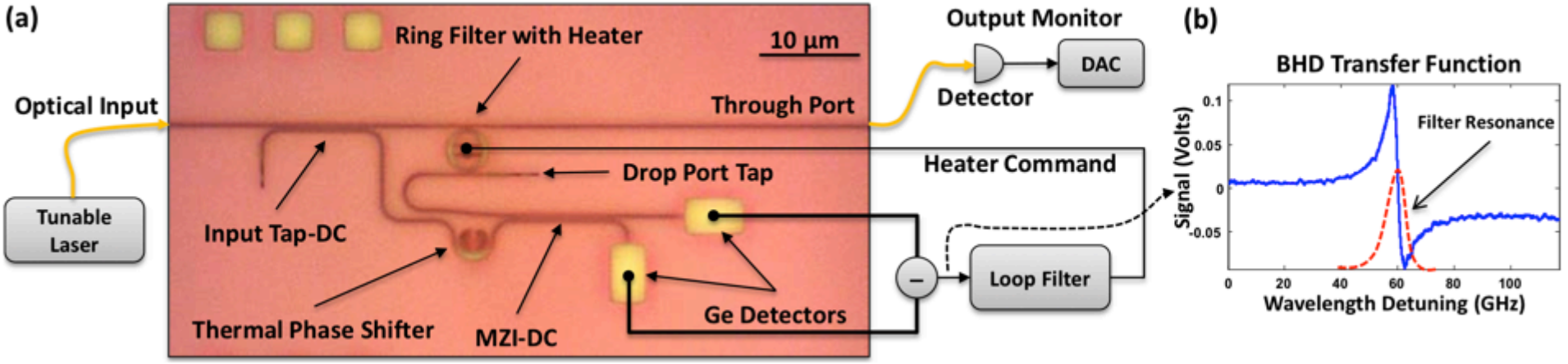




Resonant locking of a DWDM filter (Sandia)

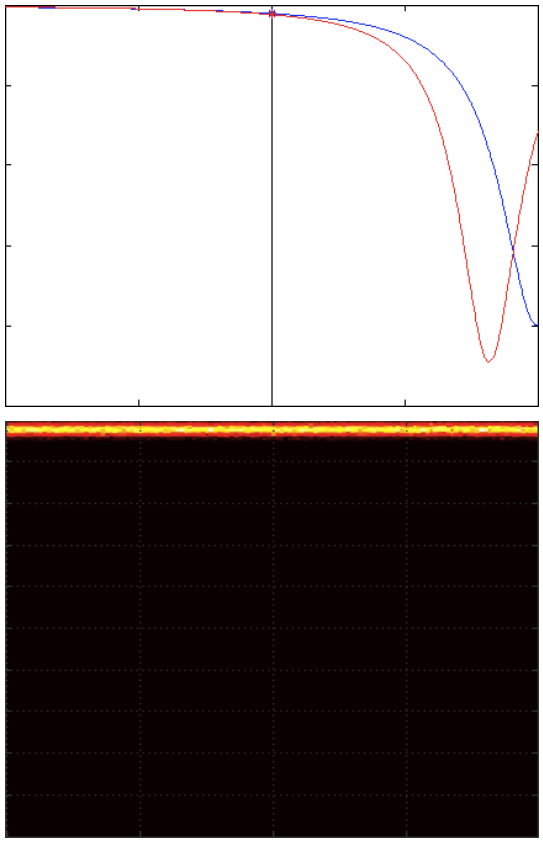
- Creates anti-symmetric signal – lock at zero (no reference)
- Build an optical interferometer with a ring in one arm
  - Can we eliminate phase adjust?
- Simple electrical circuit (minimum power)

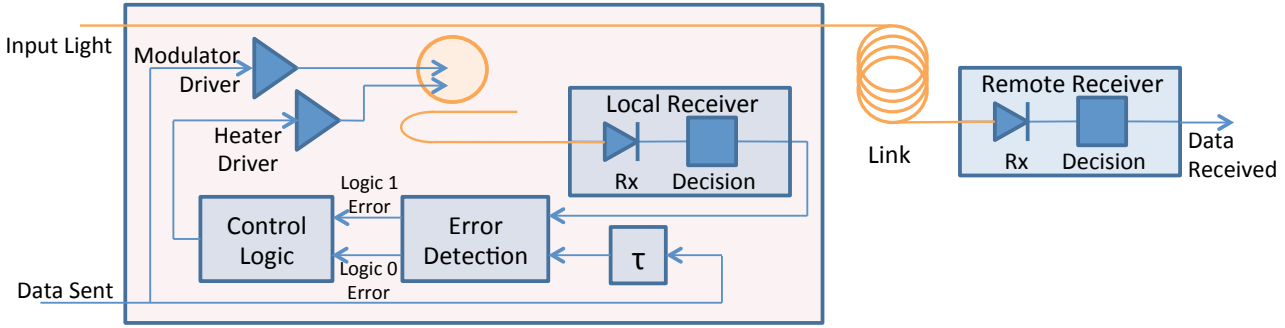


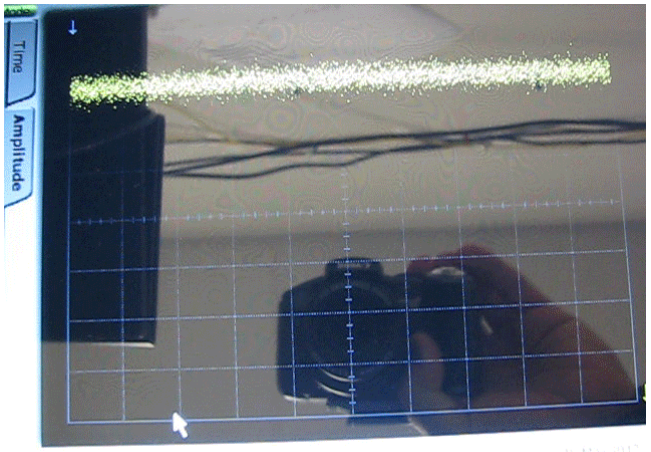


Modulator wavelength stabilization using bit errors (Sandia)

- Direct measurement of the bit errors
- Requires high speed circuitry
- Most compact solution (no low pass filtering)







Summary slide

Sandia National Laboratories

- Ge on Si detectors are key building block for Si Photonics.
  - Small size of Ge on Si detector results in small capacitance which enables low energy receiver.
  - Strain enhances responsivity of Ge on Si in C-Band (1530-1565) nm.
  - Compact size reduces dark current. Improves signal to noise.
- On-chip detectors are also key components in WDM transmitter schemes.
  - Enable stabilization of filters and modulators across chip.

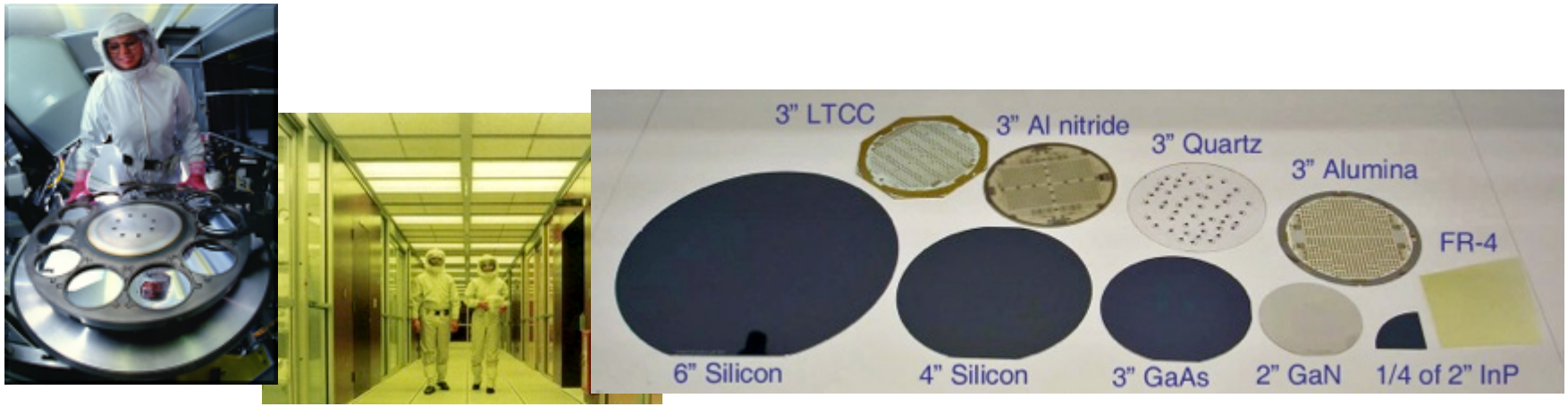
Sandia National Laboratories

Thank you for your attention!
And….

Sandia's MESA Facility

Sandia National Laboratories

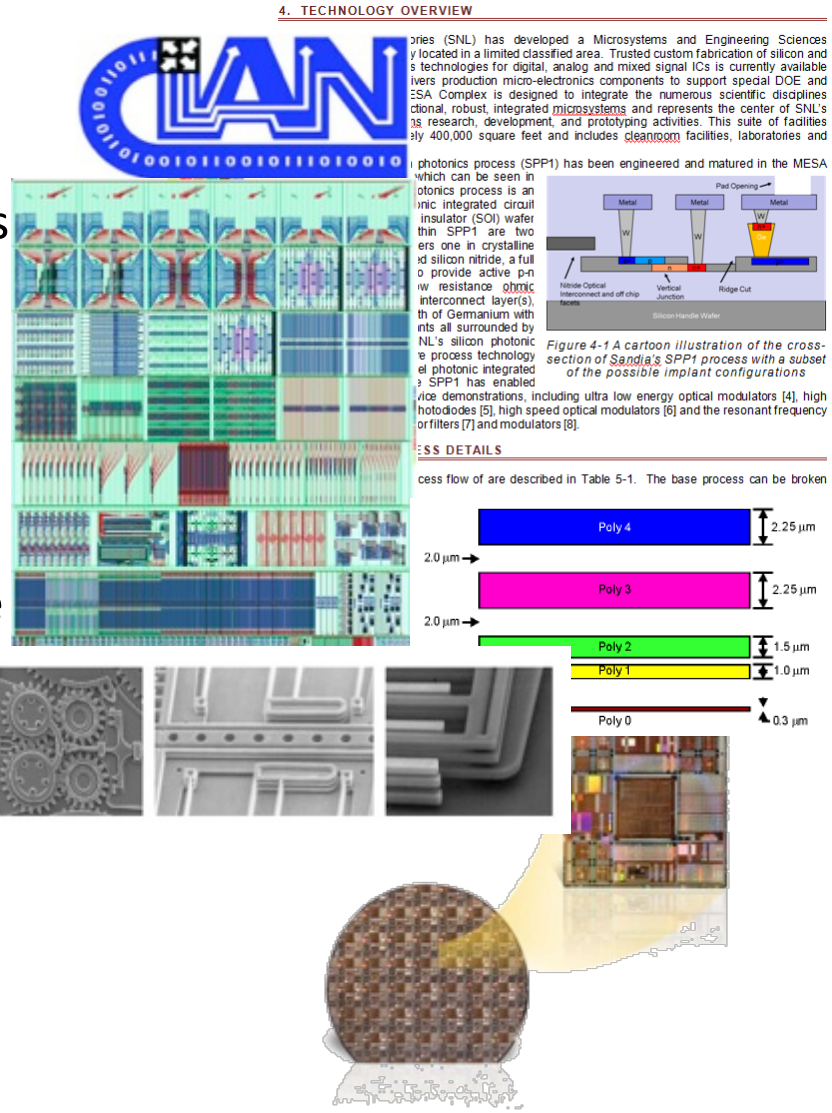
Microsystems and Engineering Sciences Applications (MESA)



- Here today, here tomorrow.
  - → Scheduled IC deliveries to NW customer beyond ten years.
- Silicon photonics processes are rooted in manufacturing.
  - → High yield, low variance in 'standard' processes.
- Can handle a wide variety of materials processing
  - → Can adapt to changing research needs
- Partner with a variety of external institutions
  - → Universities, Government, Private Industry

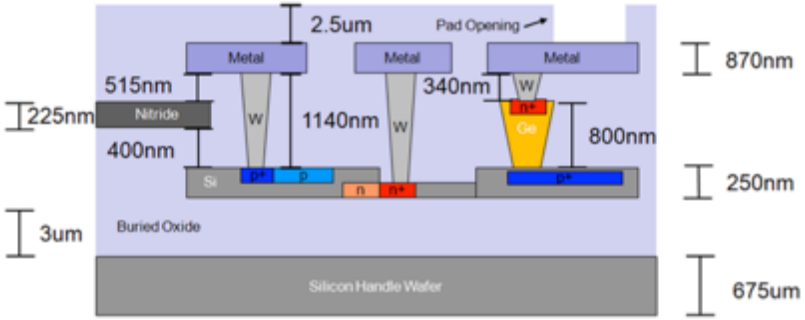
Sandia and MPW

- SPP1 silicon photonics process
  - Developed design manual, pilot MPW in process, delivered 25 chips to 5 university collaborators.
- SUMMIT V 5 layer polysilicon MEMS process
  - Developed design manual, DRC supported multiple MPWs over the last decade
- CMOS7 Rad-hard, mixed-signal CMOS technology
  - 0.35um, 3.3V core, 3.3V I/O



Silicon Photonics Design Manual

Sandia National Laboratories



6.2.1 Si Cut (GDS layer 1)

This is layer is etched after the definition of the partial ridge etch. Fully etched waveguides, disk resonators, directional couplers, etc. are all defined in this step. The design rules for t include the following:

A. Minimum line width of 100 nm
B. Minimum space (line to line separation)of 280 nm
C. Minimum taper point 80 nm. (Note tapers coming to an 80 nm point should be less um long.
D. Minimum overlap with Ridge layer of 500 nm on all sides (Note: either Si overlaps Ridge Overlaps Si). This rule may be difficult to implement in some cases, e.g. rit waveguide transitions for this we recommend use of a library device described in sect
E. *Recommended* waveguide width of 400 nm with a minimum bend radius of 1.75 um.
F. *Recommended* waveguide width to couple to ring/disk resonators of 320 nm.

The design rules for the Si cut layer are illustrated in Figure 6-1, and SEM images of the effects rule violation are shown in Figure 6-2.

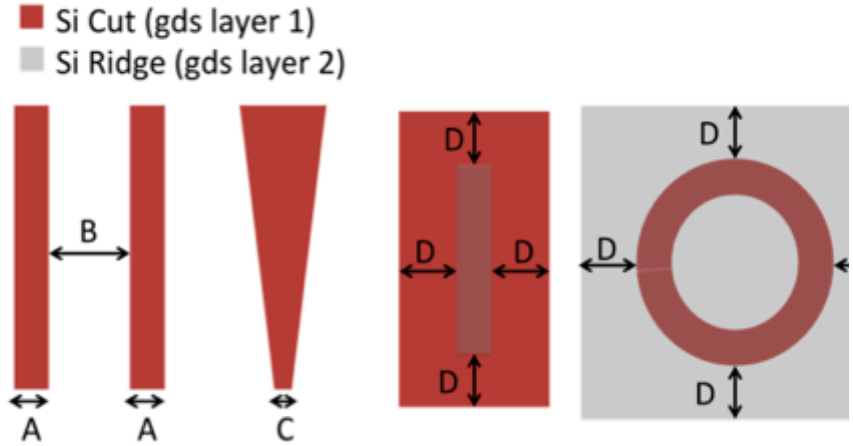
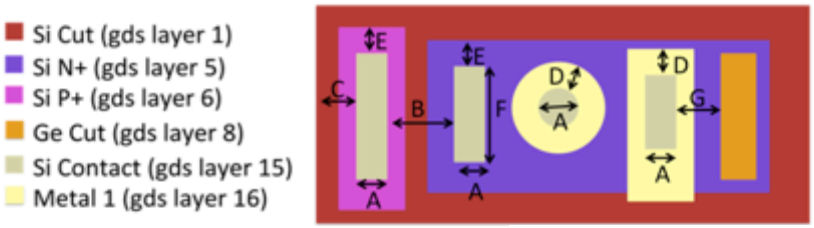


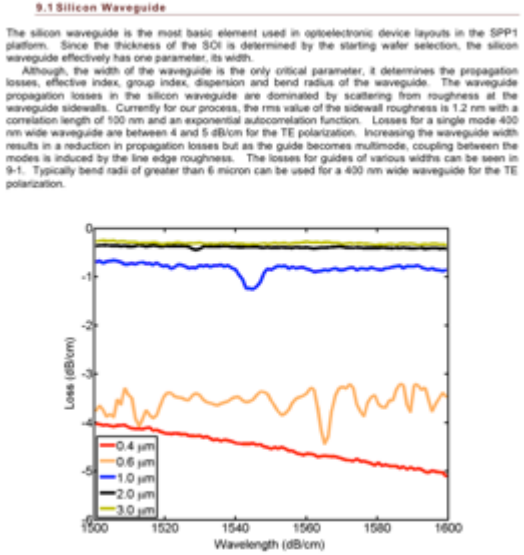
Figure 6-1 Illustration of Si cut layer design rules

6.2.12 Si Contact (GDS layer 15)

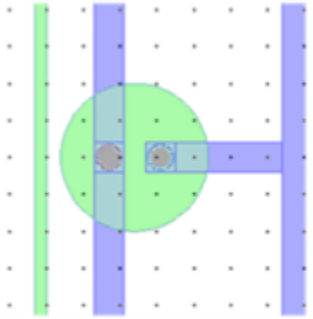
The Silicon contact layer is used for making ohmic electrical contacts to P+ and N+ doped Si. The contact width is specified to be 500 nm. The contact width is specified in order to guarantee proper filling and CMP of the Ti/TiN lined tungsten contact. For trench type contacts a rectangular shape should be used with a width of 500 nm and a length greater than 500 nm. For point type contacts, circular contacts may be used. The design rules for this layer are specified below.

A. Contact width of 500 nm
B. Minimum space of 500 nm
C. Should be surrounded on all edges by a minimum of 150 nm of Ge cut, *Recommended* 400 nm minimum.
D. Should be surrounded on all edges by a minimum of 150 nm of Metal 1
E. Should be surrounded on all edges by a minimum of 100 nm of P+ or N+ Ge
F. Length greater than 500 nm
G. The minimum space from Ge cut is 1 um





9-1 Propagation loss for the TE polarization for si waveguides of various widths. Multimode phenomena is observed in the wider waveguides.

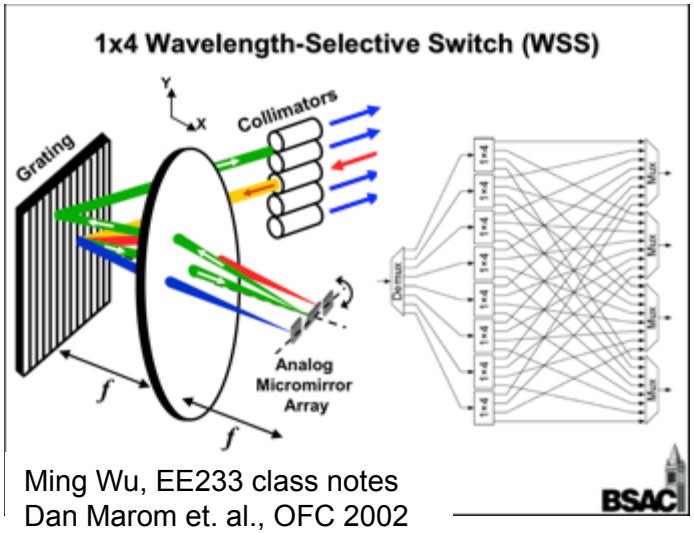


4um optical modulator

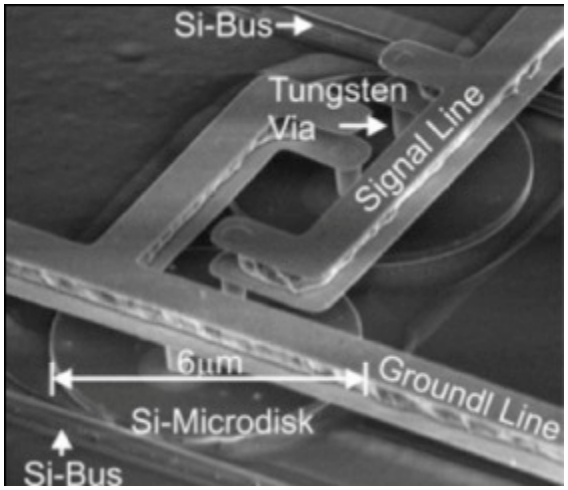
Active switching technology choices

Sandia National Laboratories

- MEMs, Liquid Crystal (WSS)
  - 1:N (good!) or 2 x 2 (bad)
  - Slow (1 us – 1 ms)
  - Often free-space (grating for WSS) {expensive}
  - Fairly scalable to large sizes?
    - 80 λ x 1 x 9
  - Flex bandwidth
  - Products
- Integrated Optics (Silicon Photonics, III-V)
  - 2 x 2 (bad)
  - Slow (1 us) or very fast (<100ps)
  - Scalable (with more maturation)
  - Flex bandwidth
  - Research

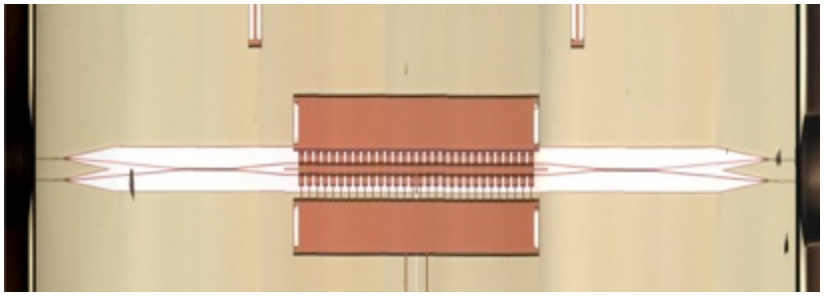


Ming Wu, EE233 class notes
Dan Marom et. al., OFC 2002

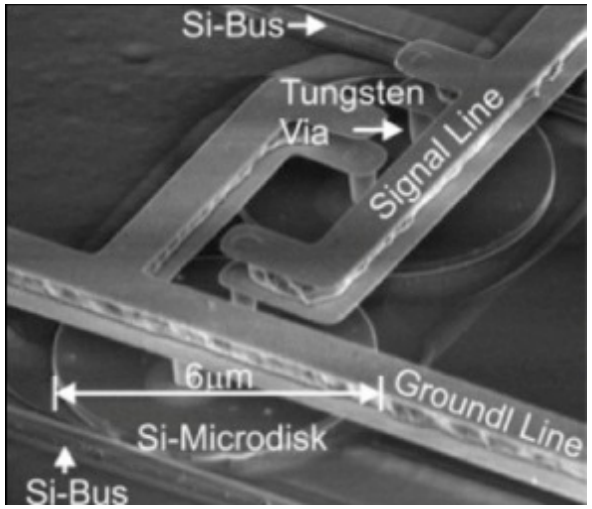


M. Watts et. al., Group IV Photonics 2008

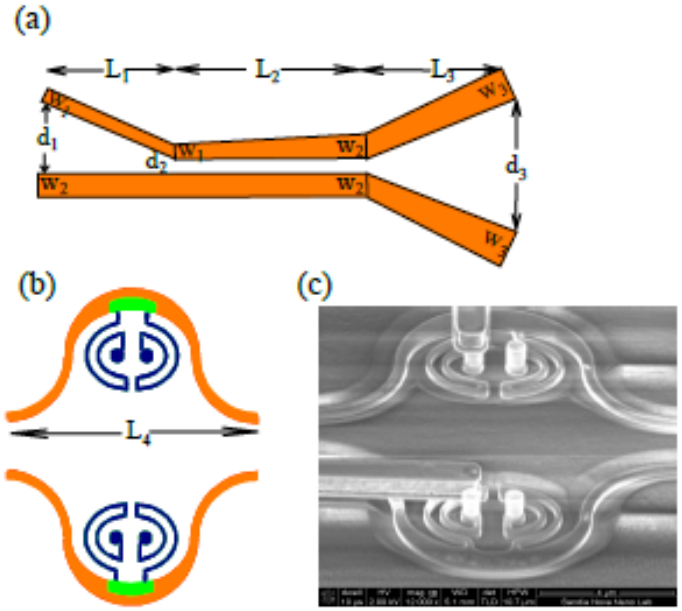
2 x 2 silicon photonics switches



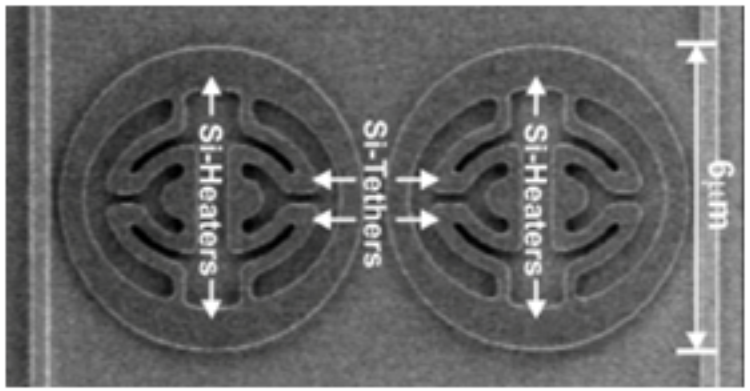
MZ – free carrier effect



MR – free carrier effect



MZ – thermo-optic



MR – thermo-optic

Refs: Watts et. al., DeRose et. al., 2008 - 2012

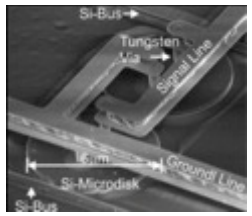
2 x 2 silicon photonics switches

Sandia National Laboratories

- Fast (< 100ps)
- Broadband
- 1pJ/switching event
- No static power
- 1 mm size

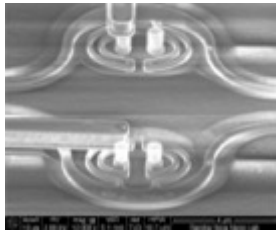
MZ – free carrier effect

- Fast (< 100ps)
- Wavelength selective*
- 1fJ/switching event
- No static power
- < 10 um size



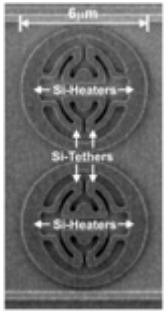
Ring – free carrier effect

- Slow (10 us)
- Broadband
- ~ 15 mW/2π
- Static power in one state
- < 10 um size + coupler



MZ – thermo-optic

- Slow (10 us)
- Wavelength selective
- ~ 4 uW/GHz (200uW)
- Static power in one state
- < 10 um size



Ring – thermo-optic