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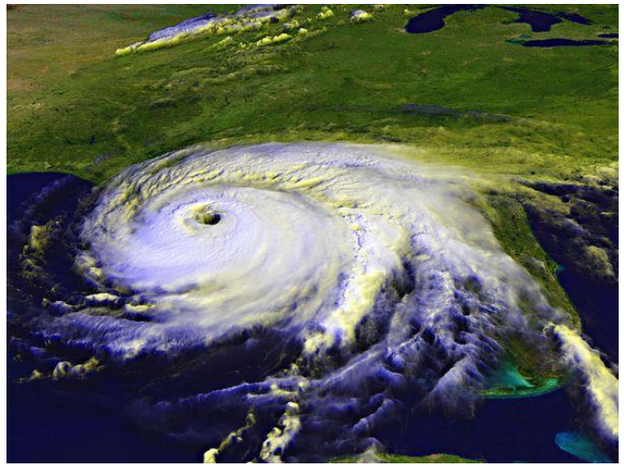

Reliability Characterization of Wide-Bandgap Semiconductor Switches

October 18, 2014

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U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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Acknowledgements

We would like to thank the DOE's **Office of Electricity** and **Dr. Imre Gyuk, Program Manager of the Electrical Energy Storage Program**, for their support and funding of the Energy Storage Program.

Project Overview

- ***Wide-bandgap semiconductors have material properties that make them theoretically superior to Silicon for power device applications***
  - Lower power loss and reduced cooling requirements would increase the efficiency and reduce the size and complexity of power conversion systems linking energy storage to the grid, *thus reducing overall system cost*
  - However, wide-bandgap materials and devices are far less mature than their Si counterparts; many questions remain regarding their reliability, *limiting their implementation in systems*
- ***Goal: Understand the reliability physics of SiC and GaN wide-bandgap power switches and how it implements circuit- and system-level performance***

Motivation and Overview for This Year's Work

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For mature Si technology, most power device reliability focuses on the packaging and thermal management

- Devices are mature and well-understood
- Manufacturing is well-controlled

For WBG materials, device instabilities due to internal charge trapping are still a concern

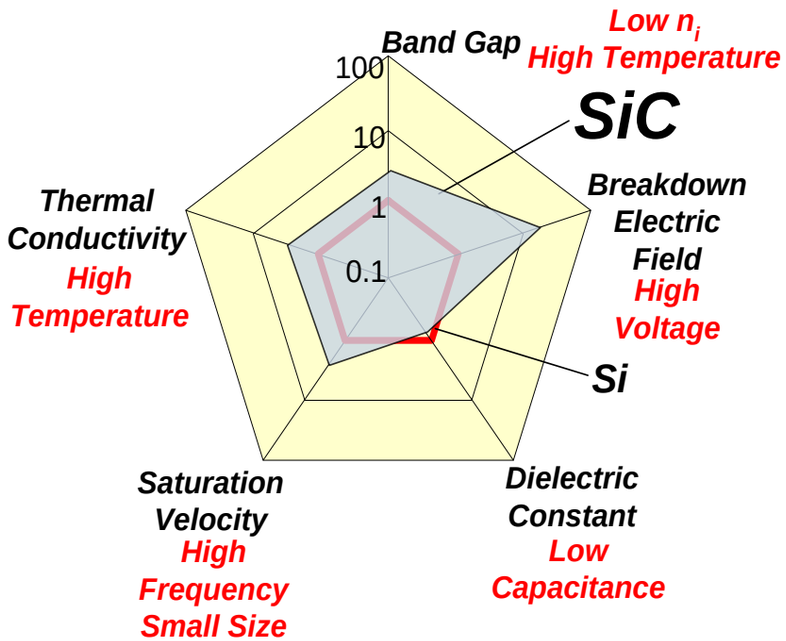
- Materials are much newer
- Manufacturing in not as well-controlled
- True for both SiC and GaN, but SiC is more mature

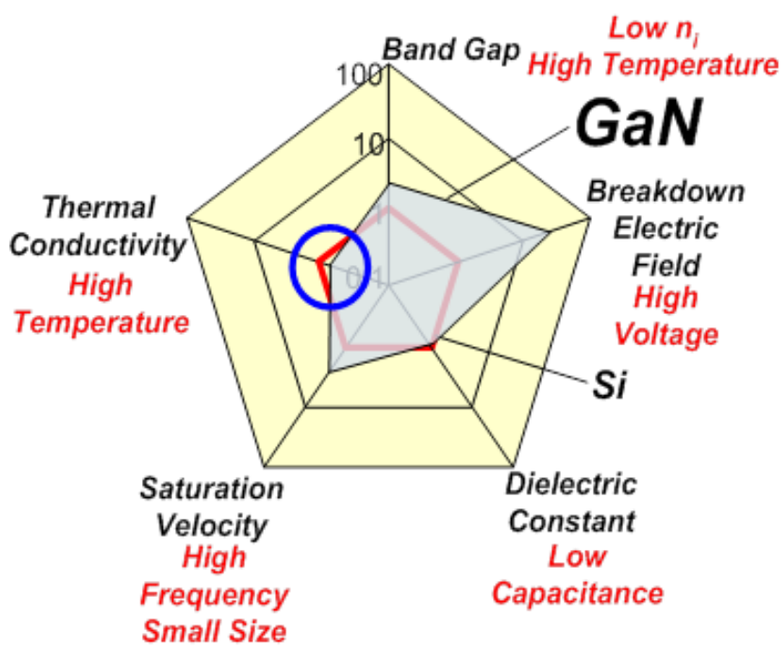
While much progress has been made, many reliability issues remain

- Easy-to-use characterization techniques that can be employed by users of devices are needed
- Coupling between defect physics and device design is not well understood
- Correlation between device- and circuit-level degradation is not well understood

Our work this year had addressed these questions

Superior Properties of WBG Materials and their Impact on Power Conversion Systems





Figures courtesy of Prof. D. K. Schroder, ASU

- **WBG semiconductors can have a strong impact on system size and weight due to higher switching frequency and reduced thermal management requirements**
- ***But their reliability is far less mature than traditional Si devices!***

13.5 kV, 100 A Si IGBT module

M. K. Das et al., ICSCRM 2011

10 kV, 120 A SiC MOSFET module
10% weight and 12% volume of Si module

Power Device Characterization Laboratory

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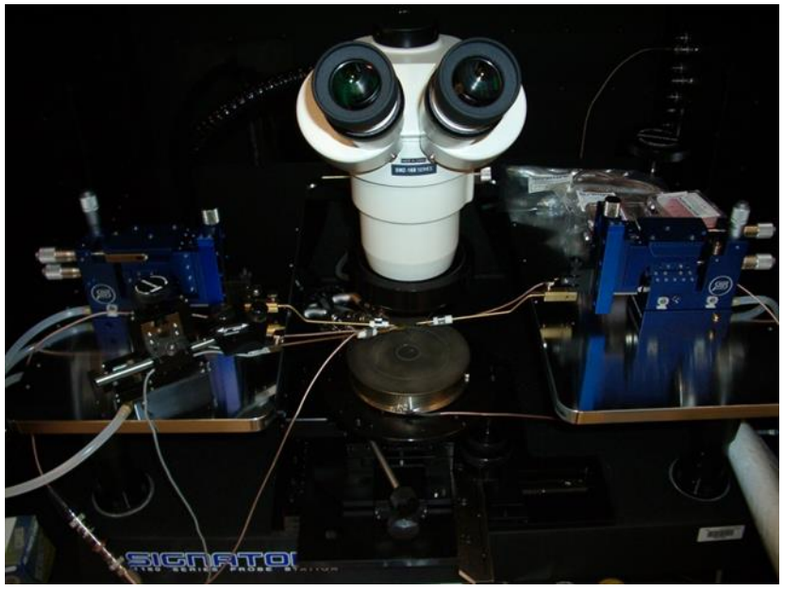
Facilities funded by this program

- Hot chuck capable of 600˚C operation (used for MOS capacitor measurements, including interfacial defect density characterization)



- High-power test system for evaluation of power semiconductor switches
  - 3 kV, 50 A
  - Packaged parts up to 400˚C
  - Wafers and die up to 300˚C

- *Leverages Sandia's role as the lead DOE lab for electronics, including significant investments in silicon (e.g. ASICs) and compound semiconductors (e.g. solid-state lighting)*

SiC Power MOSFET Reliability (1)

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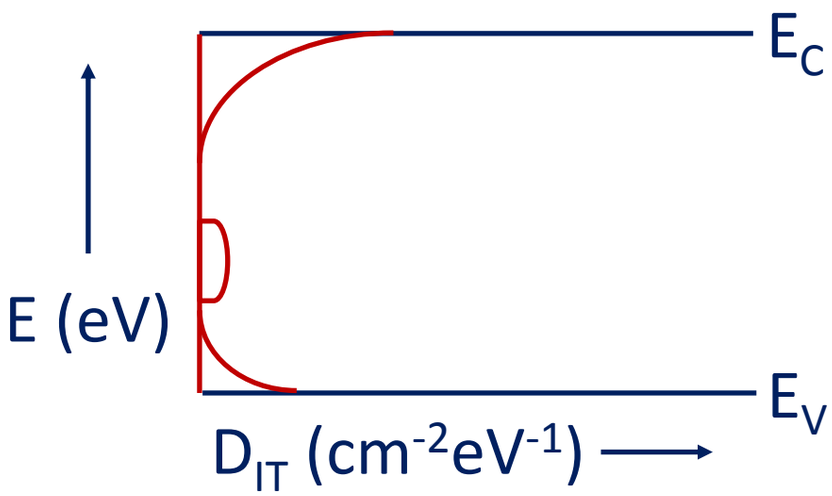
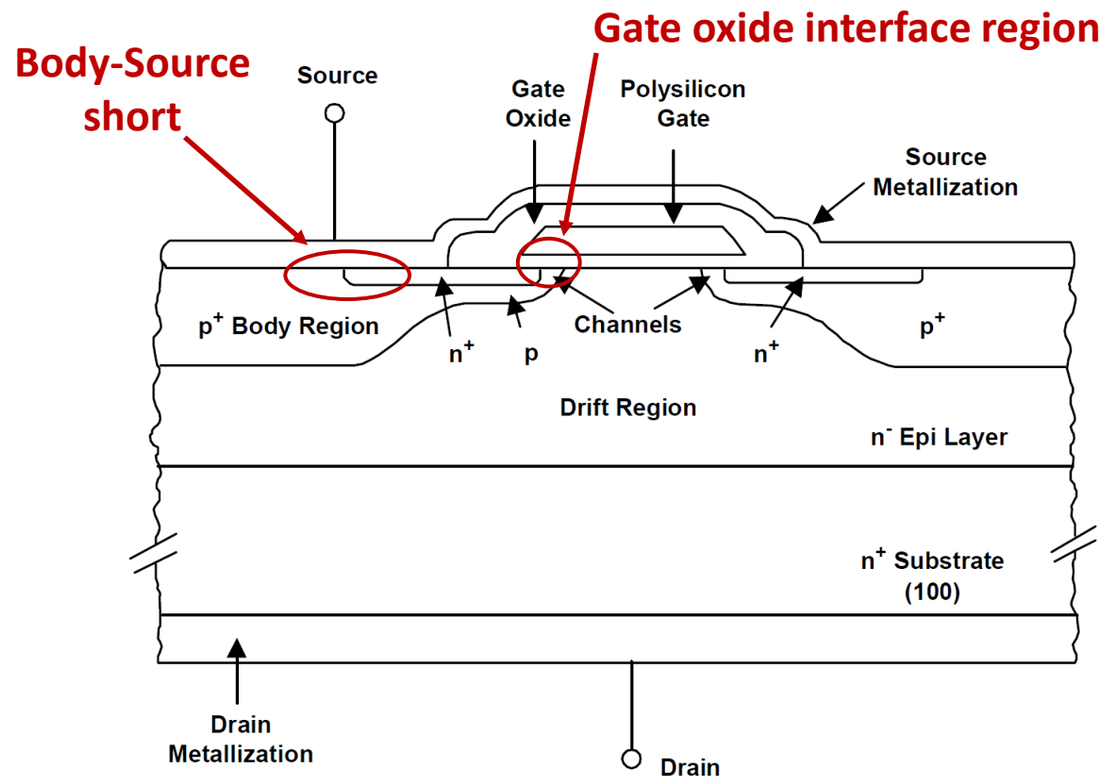
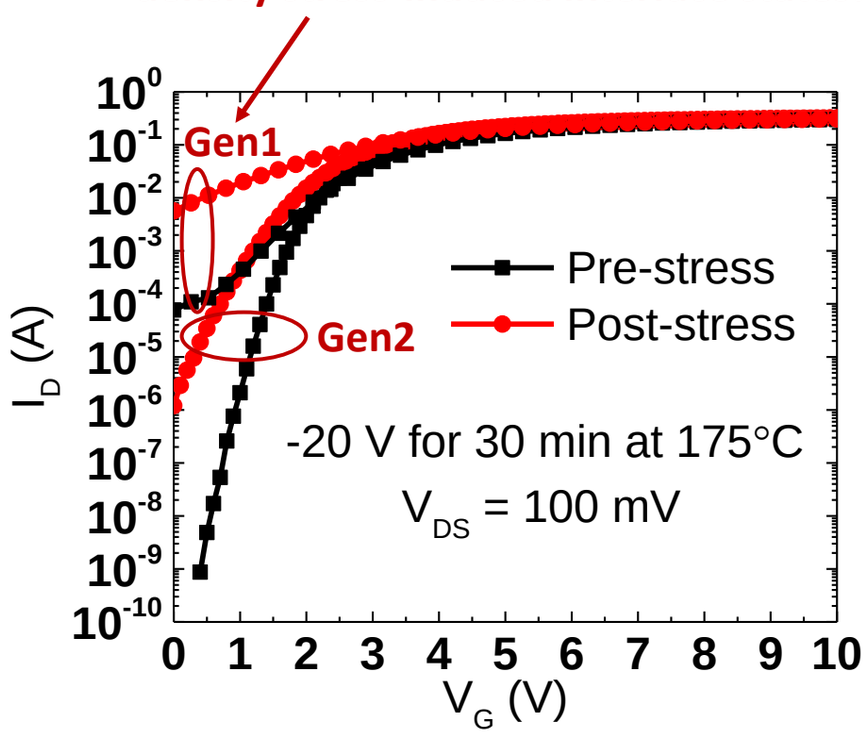
A high density of SiO_2-SiC interfaces states can render a power MOSFET useless





This device cannot be turned off due to a high density stress-induced interface states!



- **Circuit designers want to evaluate interface density in real MOSFETs, not process-monitor capacitors (and they don't have access to such caps anyway)**
- **Traditional MOSFET interface state density measurements such as charge pumping require a separate body contact, which doesn't exist for vertical DMOS power devices**
- ***A simple technique is needed for power MOSFET interface state density measurement that can be used without detailed knowledge of the process parameters***

SiC Power MOSFET Reliability (2)

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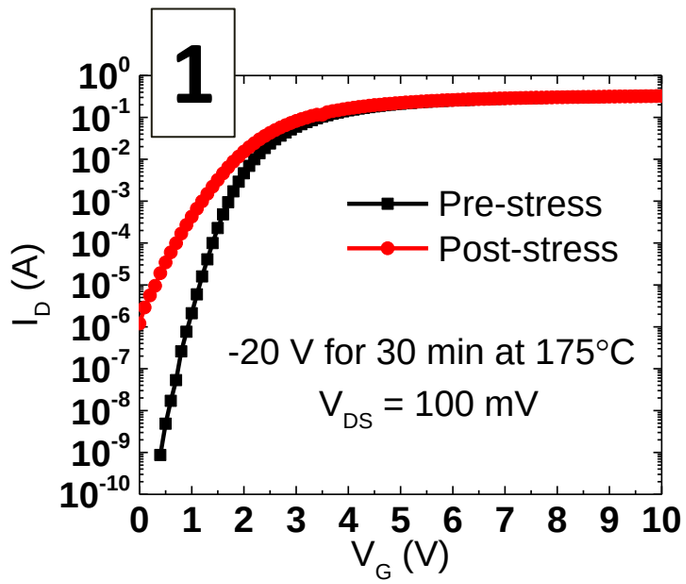
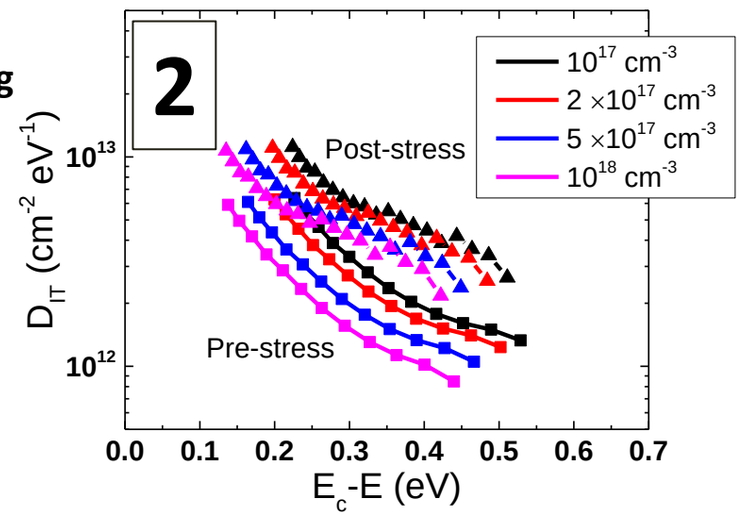
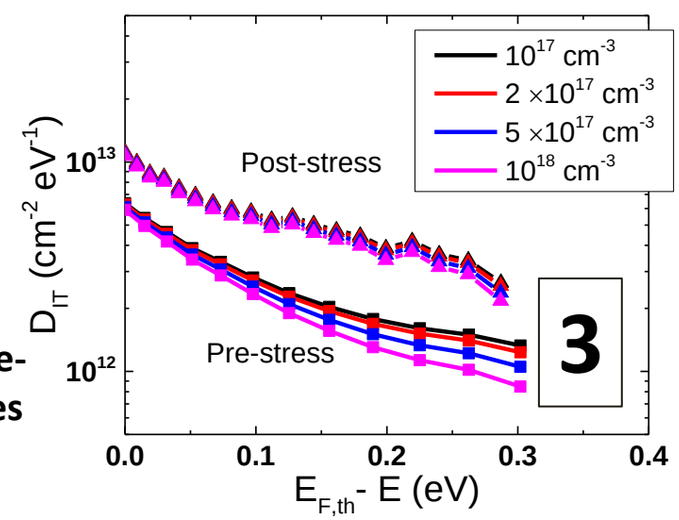
We have developed a technique that circuit designers can easily use to evaluate the reliability of commercial SiC MOSFETs



Extract D_{IT} from sub-threshold region using MOSFET equations

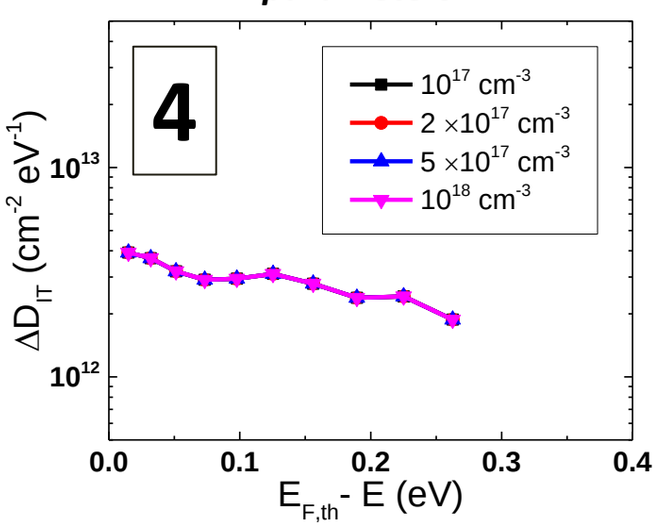


Normalize energy scale to Fermi level at threshold



Take difference of pre- and post-stress values

Universal curve that is insensitive to unknown parameters



- **Analyzed sensitivity of technique to:**
  - **Doping**
  - **Oxide thickness**
  - **Method used to determine V_T**
- **Can easily be performed on commercial devices**
  - **No knowledge of process details required**
  - **Sensitivity to major unknown parameters can be quantified**

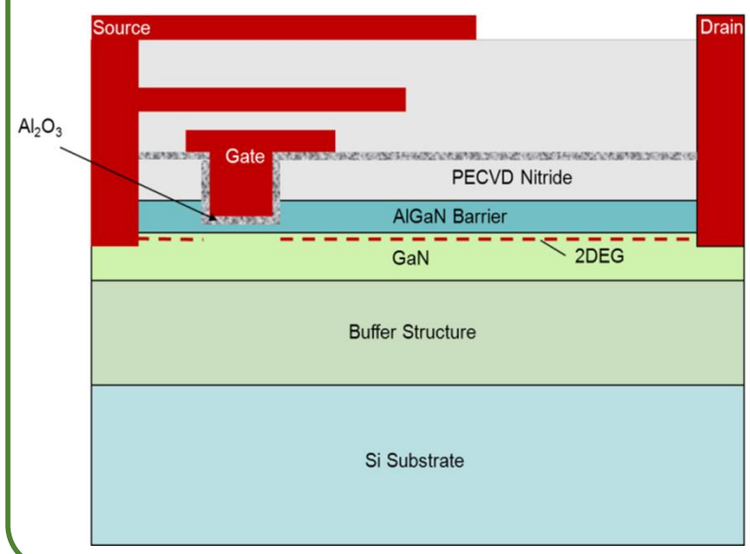
Details reported in D. R. Hughart et al., IRPS 2014

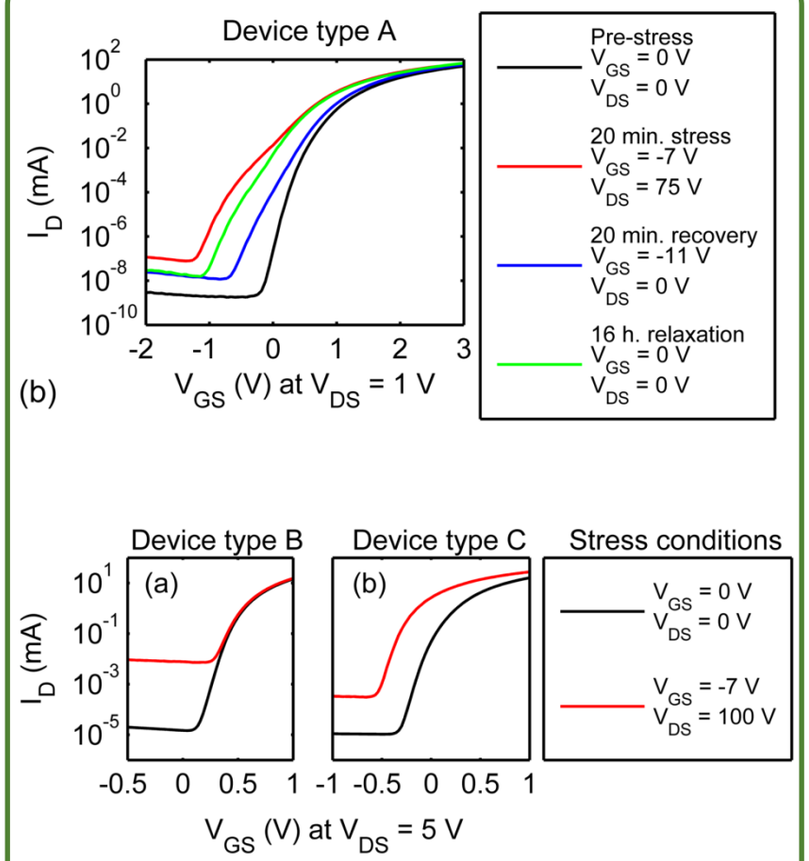
GaN Power HEMT Reliability (1)

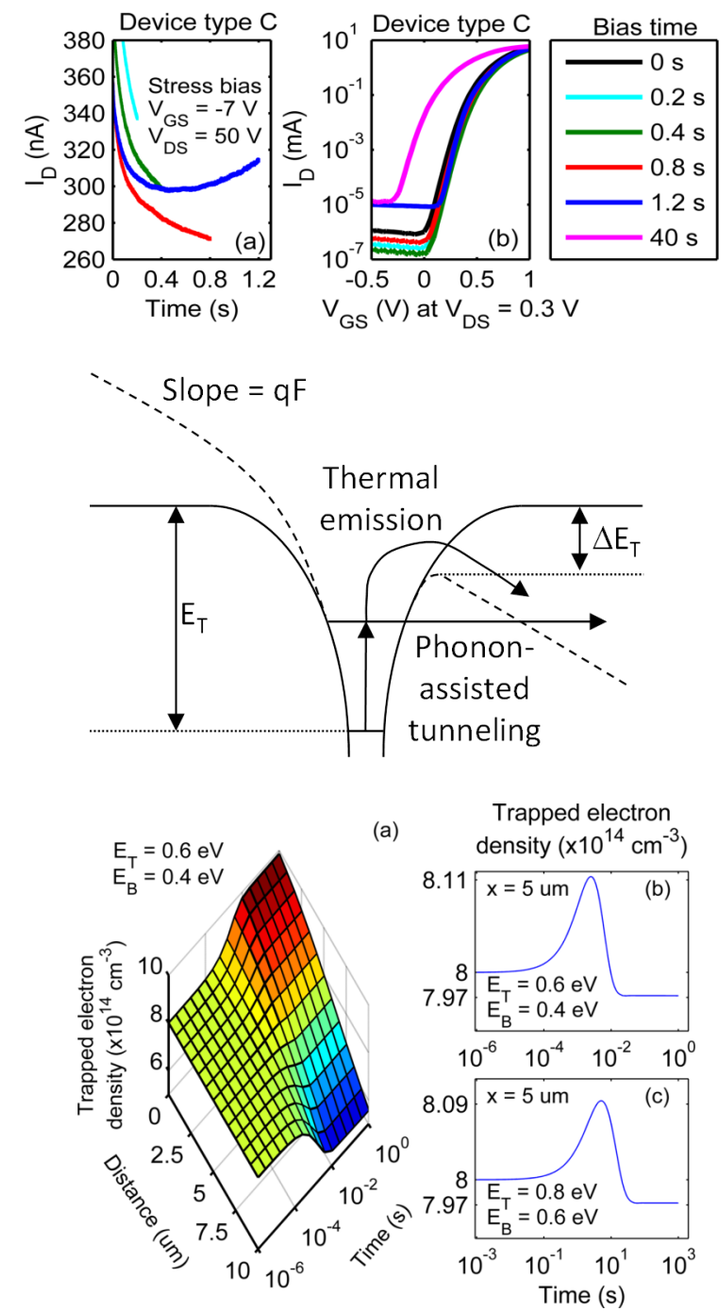
We have performed an in-depth analysis that couples defect physics to device design

Device Type	Gate Oxide (Al_2O_3)	Gate Stack AlGaN
A	Yes	Present (t ~ 5 nm)
B	No	Residual (t < 1 nm)
C	No	Present (t ~ 5 nm)

Process splits to evaluate the physical location of charge traps





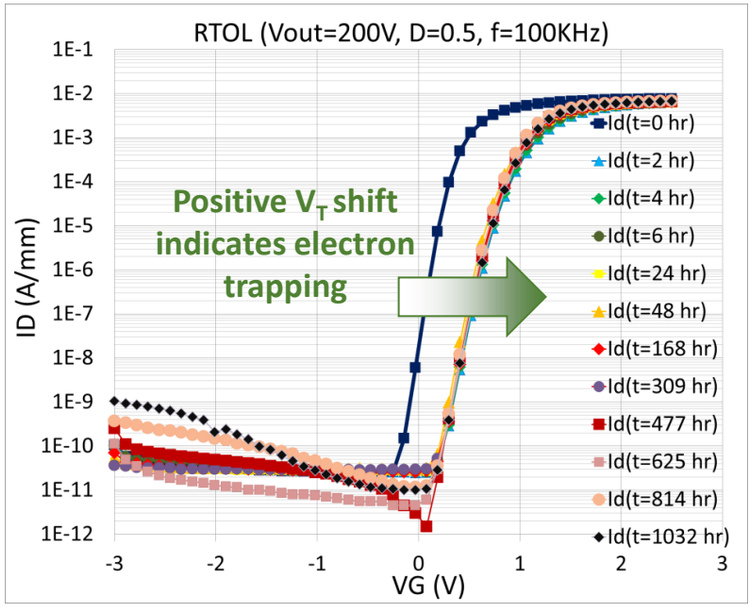


- **Recessed gate with insulator for normally-off operation**
- **Absence of V_T shift in device type B suggests that traps in the AlGaN layer are responsible for instability**
- **Coupled Poisson / rate equation model with field-induced trap barrier lowering explains reversal in current during stress**

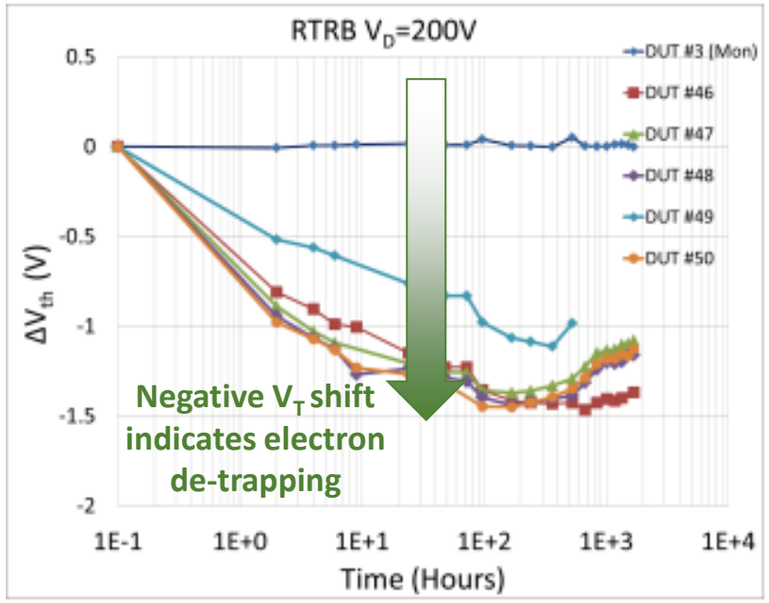
Details reported in R. J. Kaplar et al., ISPSD 2014

GaN Power HEMT Reliability (2)

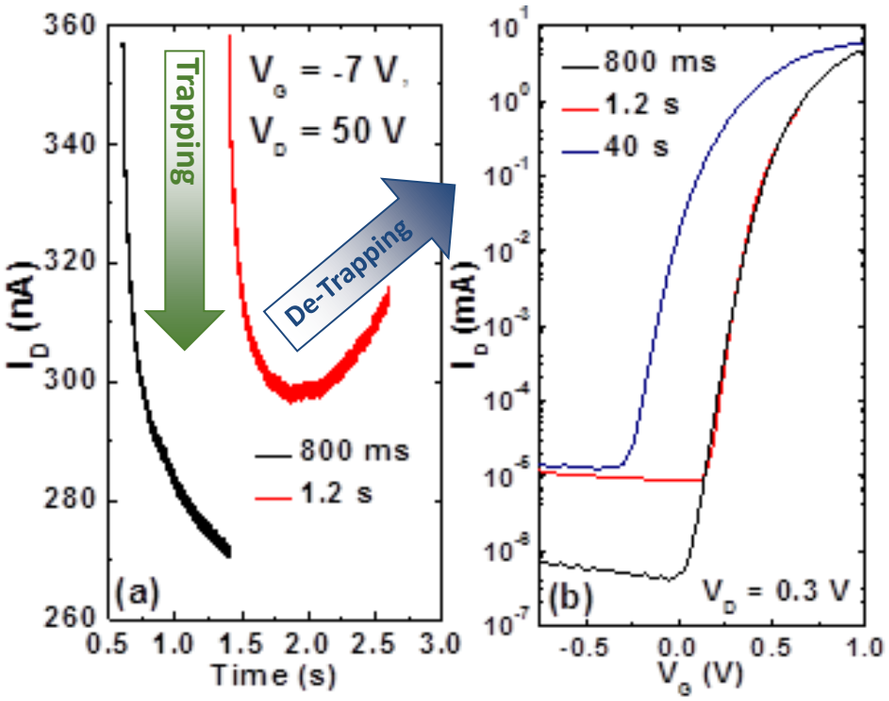
Correlation between device- and circuit-level degradation has been demonstrated



Positive V_T shift observed during switching operation



Negative V_T shift observed during DC stress



- **Apparent discrepancy is resolved by performing short-time DC stress measurements**
- **A transition from electron trapping to de-trapping is observed, and de-trapping does not have sufficient time to occur during switching stress**
- ***WBG device physics explains circuit-level behavior***

Details reported in S. G. Khalil et al., IRPS 2014

Summary/Conclusions

- SiC power MOSFET reliability
  - Developed an easy-to-use method that can be used by circuit designers to evaluate the reliability of commercial SiC MOSFETs
- GaN power HEMT reliability
  - Created a physics-based model linking defect properties to device design to explain observed degradation
  - Used the model to explain an apparent discrepancy between circuit- and device-level stress conditions, linking device physics to system design
- SiC power JFET reliability
  - Performed unbiased analysis comparing SiC JFET reliability to SiC MOSFET reliability (not shown)

Future Tasks

- Fundamental vs. process-induced MOSFET reliability
  - Working collaboratively with a second MOSFET manufacturer
- SiC MOS interface passivation
  - Collaboration with several universities to study fundamental physics of interfacial defect passivation
- Unbiased evaluation of SiC device reliability
  - Several different devices from a number of manufacturers in the test queue
- Link device physics and system-level performance
  - US Patent applicaton: “In-Situ Restoration of Semiconductor Switch Characteristics”
  - Working with a commercial company to implement the idea in a compact test system that is useful to industry

FY14 Reporting of Results

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Publications

- (Invited) M. J. Marinella, D. R. Hughart, J. D. Flicker, S. DasGupta, S. Atcitty, and R. J. Kaplar, "Progress in SiC MOSFET Reliability," *ECS Transactions* v. 58(8), pp. 211-220 (2013).
- R. J. Kaplar, J. Dickerson, S. DasGupta, S. Atcitty, M. J. Marinella, S. G. Khalil, D. Zehnder, and A. Garrido, "Impact of Gate Stack on the Stability of Normally-Off AlGaN/GaN Power Switching HEMTs," *Proc. IEEE ISPSD*, pp. 209-212 (2014).
- S. G. Khalil, L. Ray, M. Chen, R. Chu, D. Zehnder, A. Garrido, M. Munsi, B. Hughes, K. Boutros, R. J. Kaplar, J. Dickerson, S. DasGupta, S. Atcitty, and M. J. Marinella, "Trap-Related Parametric Shifts under DC Bias and Switched Operation Life Stress in Power AlGaN/GaN HEMTs," *Proc. IEEE IRPS*, pp. CD.4 .1-CD.4.9 (2014).
- D. R. Hughart, J. D. Flicker, S. Atcitty, M. J. Marinella, and R. J. Kaplar, "Sensitivity Analysis of a Technique for the Extraction of Interface Trap Density in SiC MOSFETs from Subthreshold Characteristics," *Proc. IEEE IRPS*, pp. 2C.2.1-2C.2.6 (2014).

Other presentations

- J. Flicker, D. Hughart, M. Marinella, S. Atcitty, and R. Kaplar, "Performance and Reliability Characterization of 1200 V SiC Power JFETs at High Temperatures," iMAPS HiTEC (2014).
- D. R. Hughart, J. D. Flicker, S. Atcitty, M. J. Marinella, and R. J. Kaplar, "Extraction and Comparison of Interface Trap Formation During BTI Stress in SiC Power MOSFETs Using Subthreshold Characteristics," ARL SiC MOS Workshop (2014).
- D. R. Hughart, J. D. Flicker, S. Atcitty, M. J. Marinella, and R. J. Kaplar, "Evaluation of Interface Trap Buildup in SiC Power MOSFETs using Subthreshold Characteristics," IEEE RSAMD (2014).

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Questions?