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Phase Leg Power Modules with SiC MIDSJT Devices

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Technical Objectives

The world's first Silicon Carbide power integrated circuit – the MIDSJT, is developed in this program, which combines the best-in-class features of GeneSiC's SiC SJTs and Schottky rectifiers, resulting in orders of magnitude more compact, lower inductance power modules, targeted at insertion into a wide variety of medium voltage power electronics systems.

The technical objectives of this program include:

- Detailed device design and fabrication of the SiC MIDSJT devices on mature SiC epiwafers
- Thorough on-wafer electrical characterization of SiC MIDSJTs and extract transport parameters
- Device packaging and power module assembly
- Comprehensive industry-standard reliability investigations
- Insertion into medium voltage power electronics application

Potential Applications

DoE Applications:

The SiC MIDSJT power modules to be developed in this program will drastically improve the performance and decrease the size/weight/footprint of

- Solid-State Power Station (SSPS) transformers
- Grid-tied Inverters
- FACTS-based devices
- Power System Switchgear
- Electrical Vehicles

Other Applications:

- Down Hole Oil Drilling, Geothermal Instrumentation
- Solar Inverters
- Switched Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Medical Accelerators for cancer treatment
- Induction Heating
- Motor Drives
- Naval propulsion and power distribution systems
- Aerospace applications

Device Design and Layout

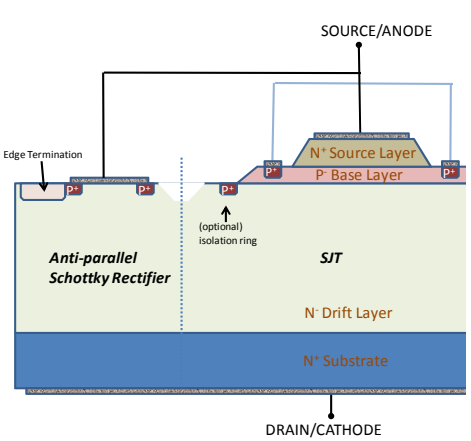

Figure 1: Cross-sectional schematic of the SiC Junction Transistor integrated with an anti-parallel Schottky rectifier. Both the devices share a common edge termination region, which is a key feature of the proposed device. This significantly reduces the expensive SiC real estate as well as the parasitic inductances associated with interconnecting discrete counterparts.

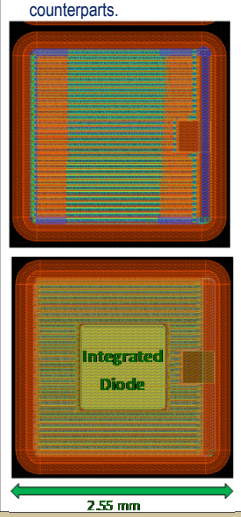

Figure 2: Device Layout of the (Top) discrete SJT and (Bottom) SiC SJT with the integrated Schottky rectifier. This design features a centrally located Schottky rectifier with a chip area of 0.94 mm^2. The peripherally located SJT has a 4 mm^2 footprint.

SiC Epilayer Design

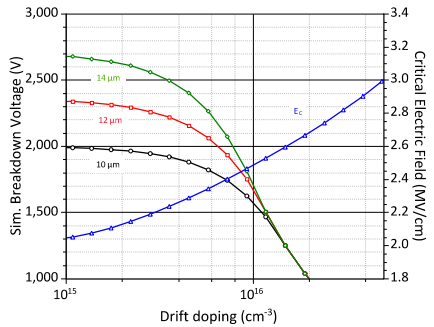

Figure 3: Simulated avalanche breakdown voltage and critical electric fields are calculated for different N- SiC epilayer thicknesses as a function of doping concentration under a punch-through eplayer design. The minimum required N- layer thickness and doping concentration can be estimated from such calculations.

SiC MIDSJT layout variations

Device ID	Source Finger width	Gate Finger width	Single/Double Level Metal
A	Narrow	Standard	Single
B/EF	Standard	Standard	Single
C	Wide	Standard	Single
B1/EG	Standard	Wide	Single
B2/EI	Standard	Standard	Double

Table 1: Summary of various SJT device designs explored during this program

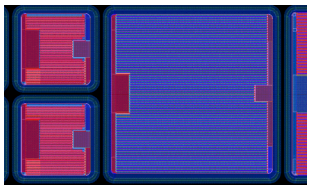

Figure 4: Snapshot of the mask layout for 2 mm x 2mm and 4 mm x 4 mm discrete SJTs

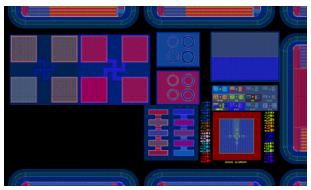

Figure 5: Snapshot of the test structures included on the mask set for process and design qualification

Unit Process Development

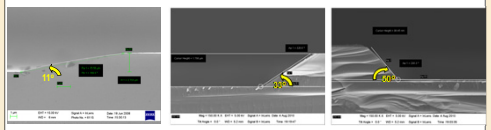

Figure 6: SEM Images of a special SiC beveling process pioneered by GeneSiC and adopted by others in the field. This novel process made it possible to etch trenches in SiC with controllable sidewall slopes for SJT fabrication.

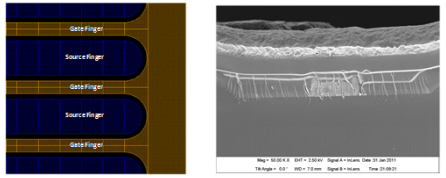

Figure 7 (Left): Snapshot of the SJT layout design showing an inter-digitated pattern formed by the Gate and Source fingers and (Right) Cross-sectional SEM image showing the special planarization process developed for fabricating SJTs with robust two-level metallization.

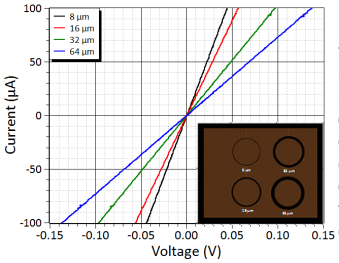

Figure 8: A state of the art low contact resistance of 0.5 mΩ-cm^2 was obtained after extensive ohmic contact optimization on p-type 4H-SiC epilayers

Project Status and Future Work

Key Accomplishments:

- Completed Key aspects of SiC MIDSJT epilayer and device design.
- Finalized optimized mask layouts
- Developed several unit process steps for high performance device fabrication

Next Steps:

- Process Integration
- Fabrication of traveler guided MIDSJT lots
- On-Wafer Electrical Characterization
- Packaging and Power Module Assembly

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