

Evaluation of Interface Trap Buildup in SiC Power MOSFETs using Subthreshold Characteristics

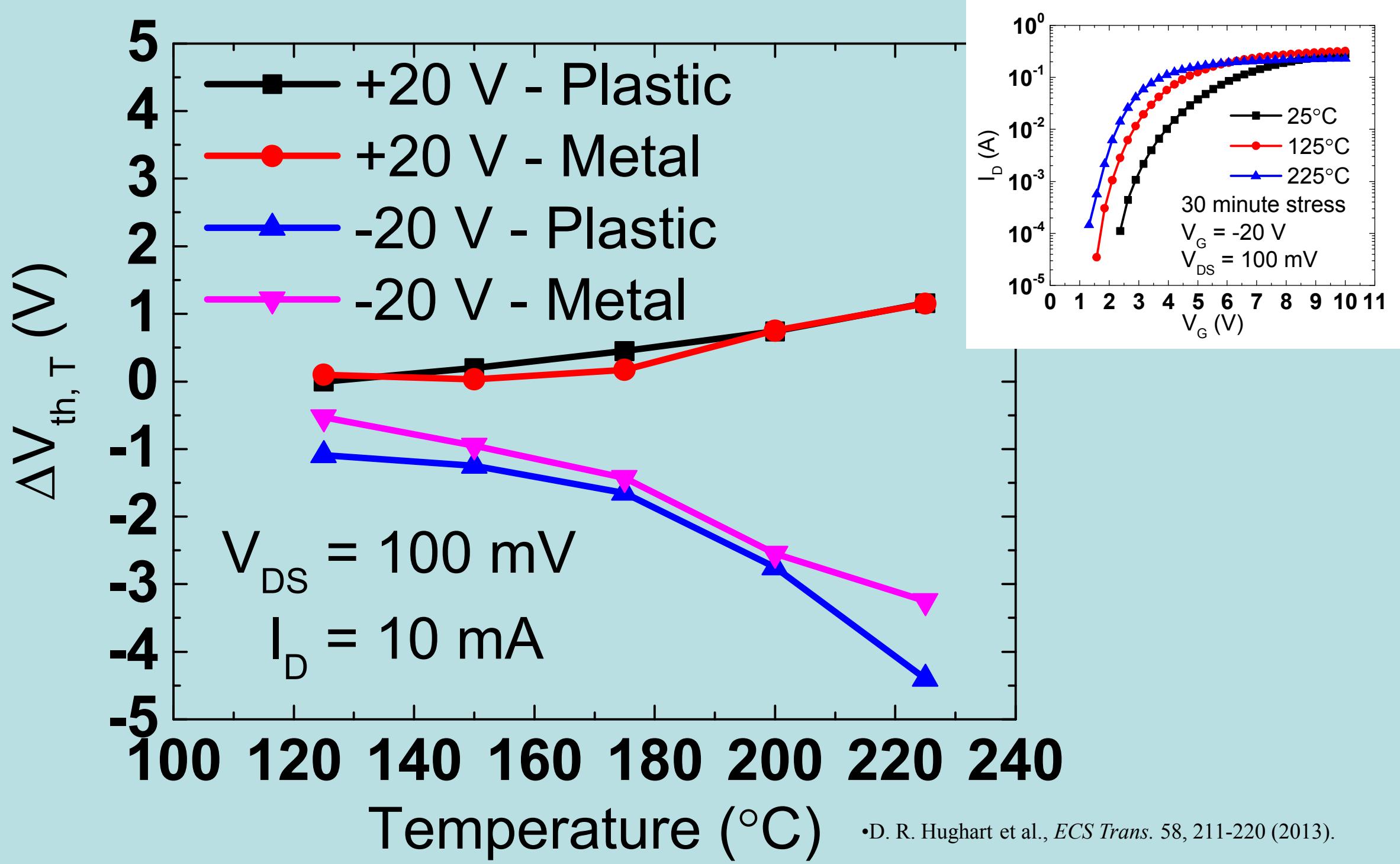
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ABSTRACT

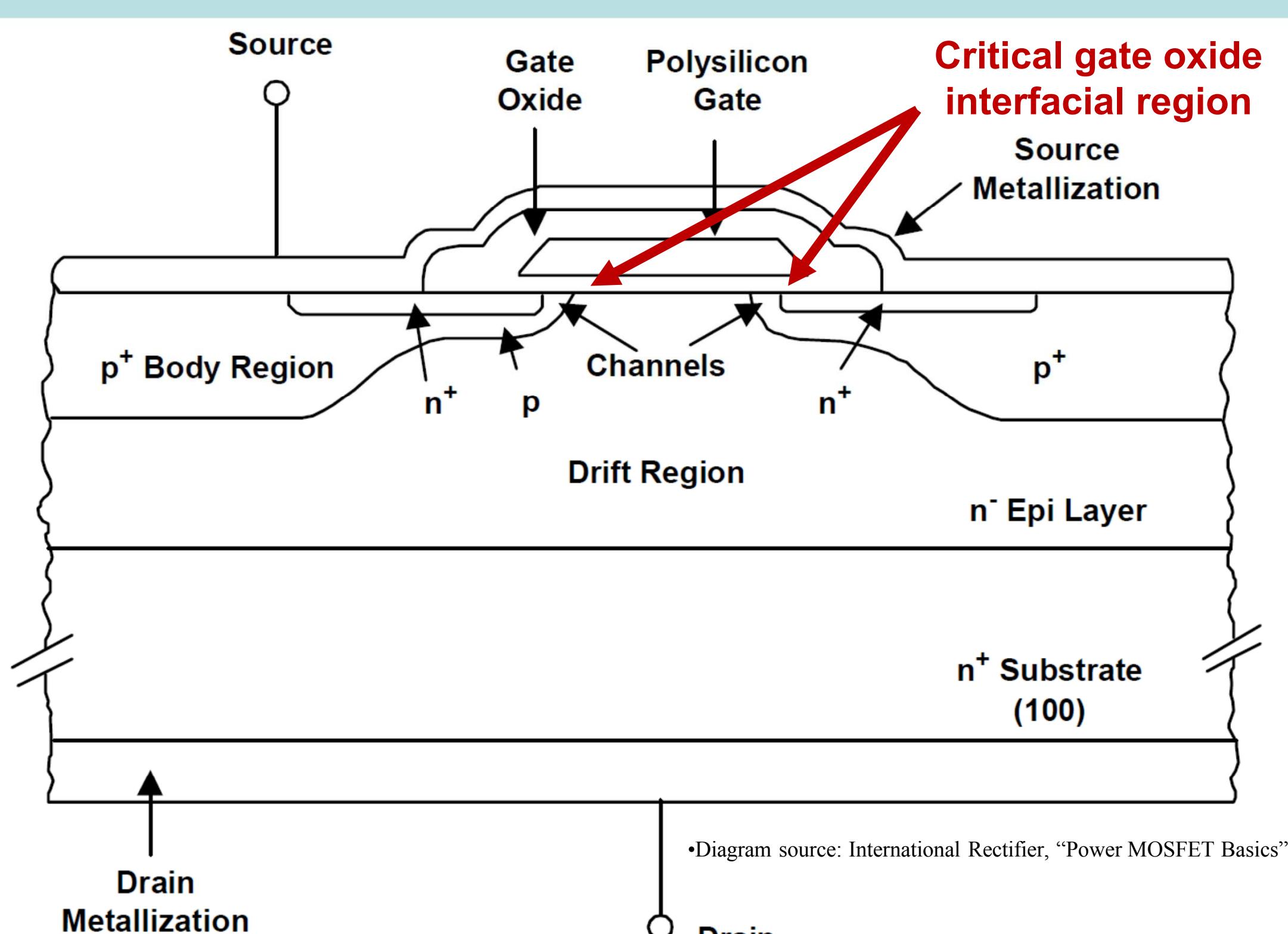
A method for extracting interface trap density (D_{IT}) from subthreshold I-V characteristics is used to analyze data on a SiC MOSFET stressed for thirty minutes at 175°C with a gate bias of -20 V. Without knowing the channel doping, the change in D_{IT} can be calculated when referenced to an energy level correlated with the threshold voltage.

BACKGROUND

- Silicon Carbide (SiC) devices are theoretically superior to Si for power electronics applications
- Reliability concerns have limited implementation
 - High interface trap density
 - V_{th} instability at elevated temperature and biases



- Graphs are for first generation SiC power MOSFETs showing V_T shifts after elevated temperature gate bias stress for plastic and metal packaging. The inset shows typical I-V curves.
- Increases in interface trap density are worse at elevated temperatures

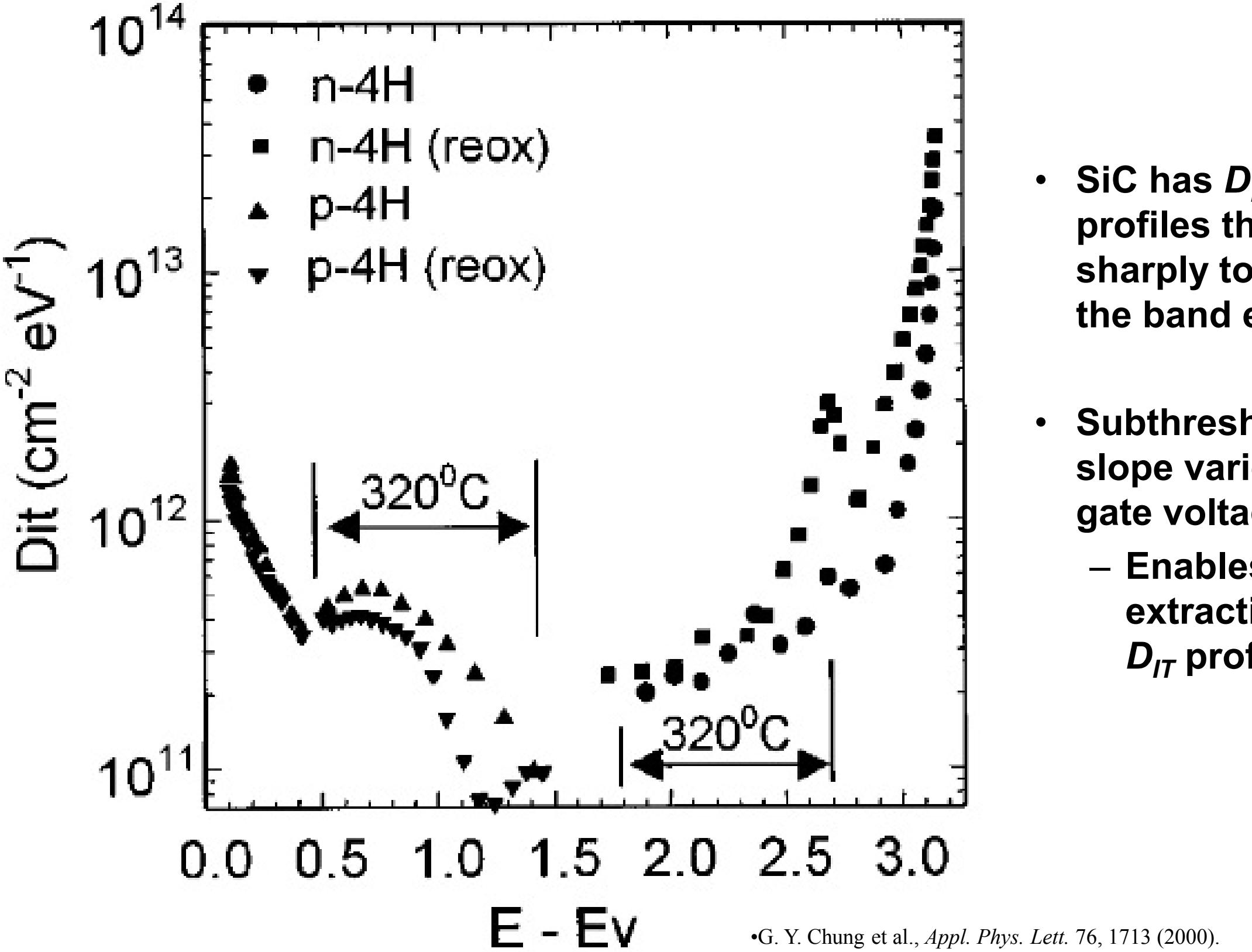


- Evaluation of interface trap density on vertical SiC power MOSFETs can be difficult without MOS capacitors and processing information from the manufacturer
- The increase in interface trap density after stress can be extracted from the subthreshold I-V curves

APPROACH

- High interface trap densities cause a change in subthreshold slope
 - Modulates the fraction of V_G that determines the barrier between source and drain

$$S = \ln(10) \frac{kT}{q} \left(1 + \frac{C_d + C_{it}}{C_{ox}} \right)$$

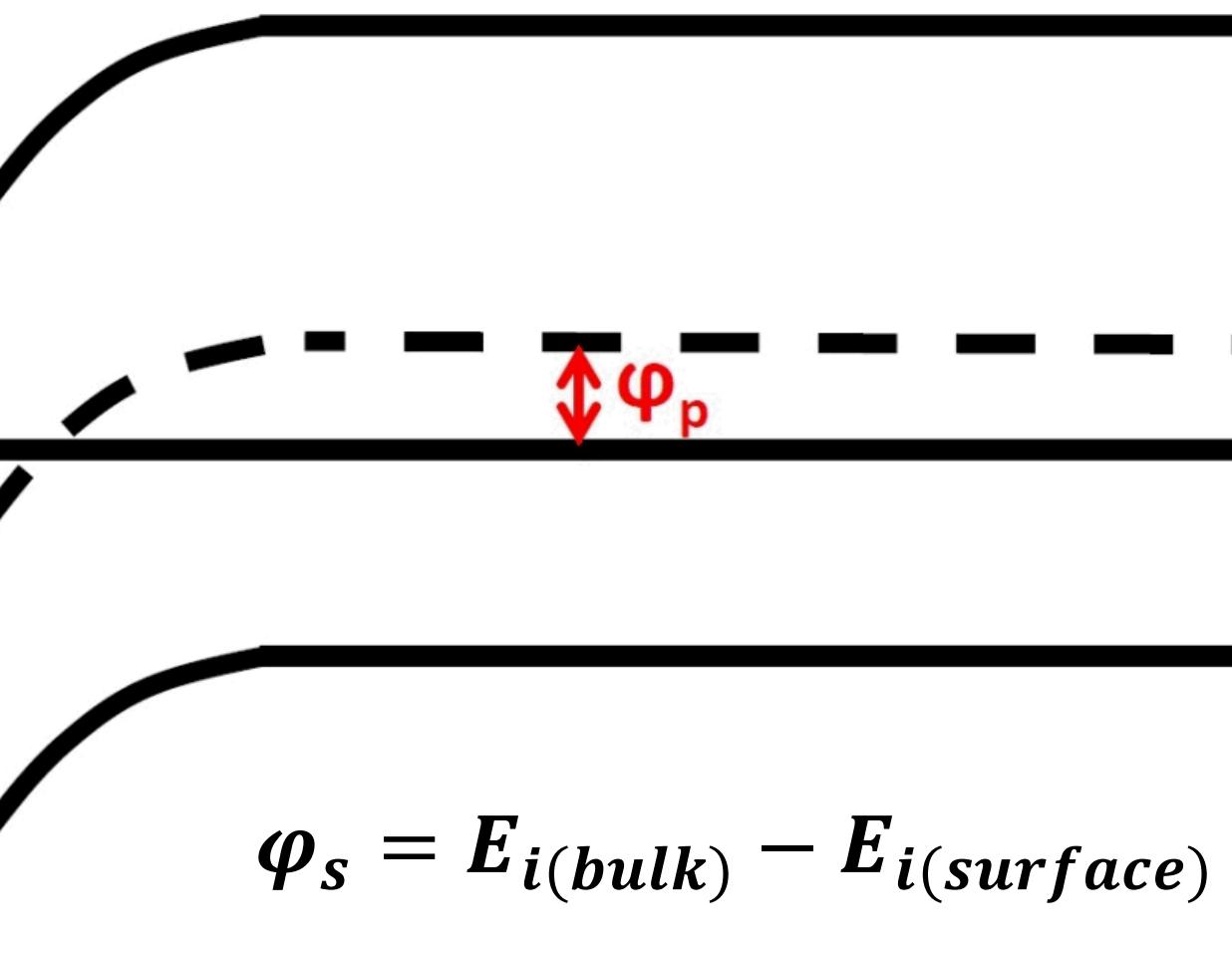


- Drain current can be related to surface potential:

$$I_D = I_{D0}(V_D) \frac{e^{\beta\varphi_s}}{\sqrt{\beta\varphi_s}}$$

- Effectively relates V_G to φ_s (band bending)

- Solve for I_{D0} at threshold



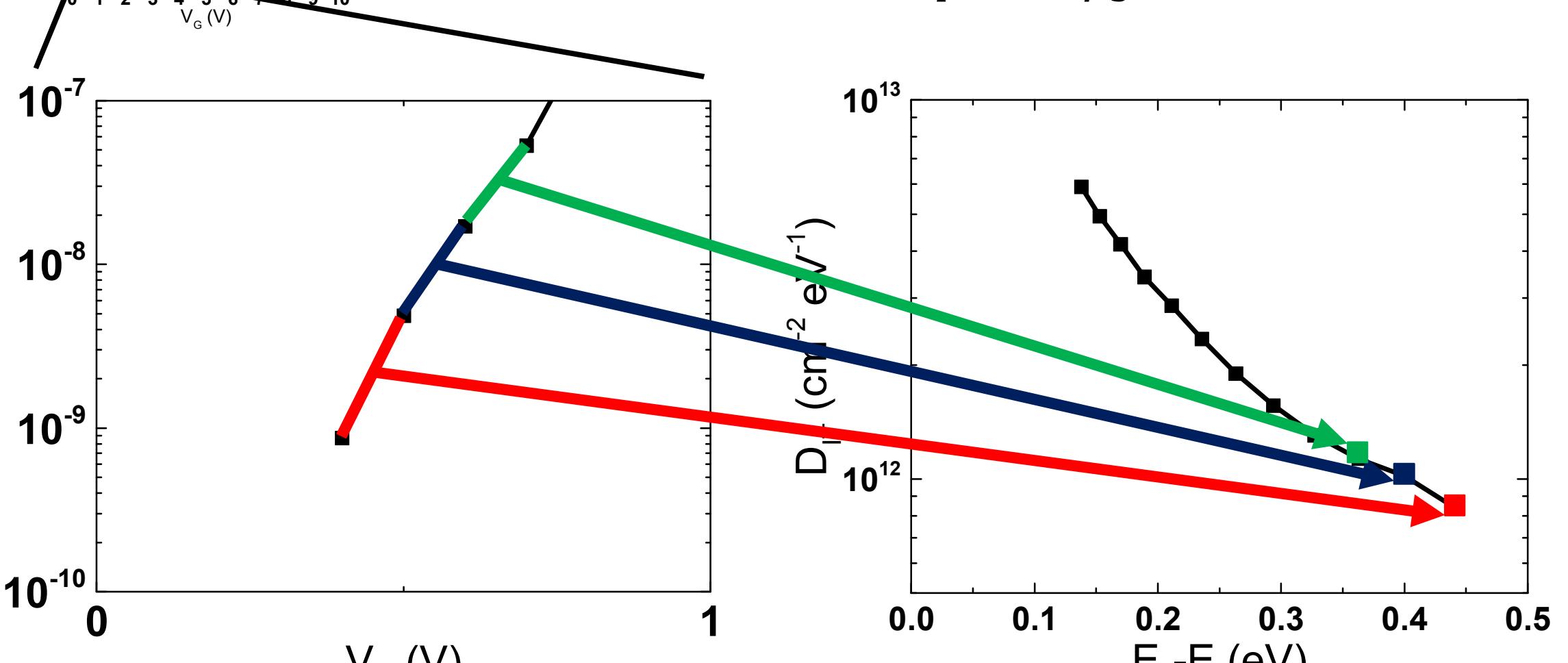
- Using V_G to φ_s , $(V_{FB} + V_{IT})$ can be solved for:

$$(V_{FB} + V_{IT}) = V_G - \varphi_s - \frac{a}{\beta} \sqrt{\beta\varphi_s - 1}$$

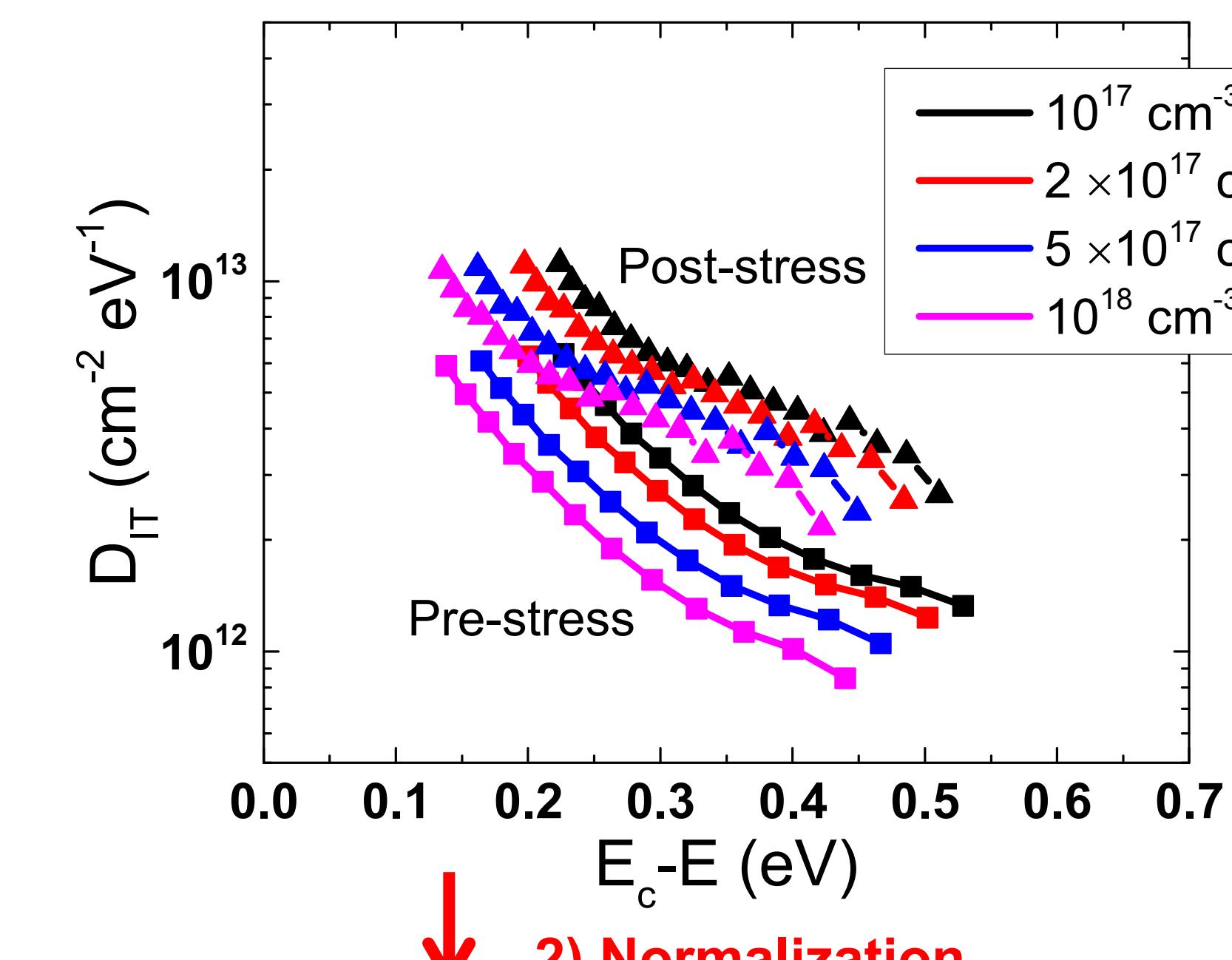
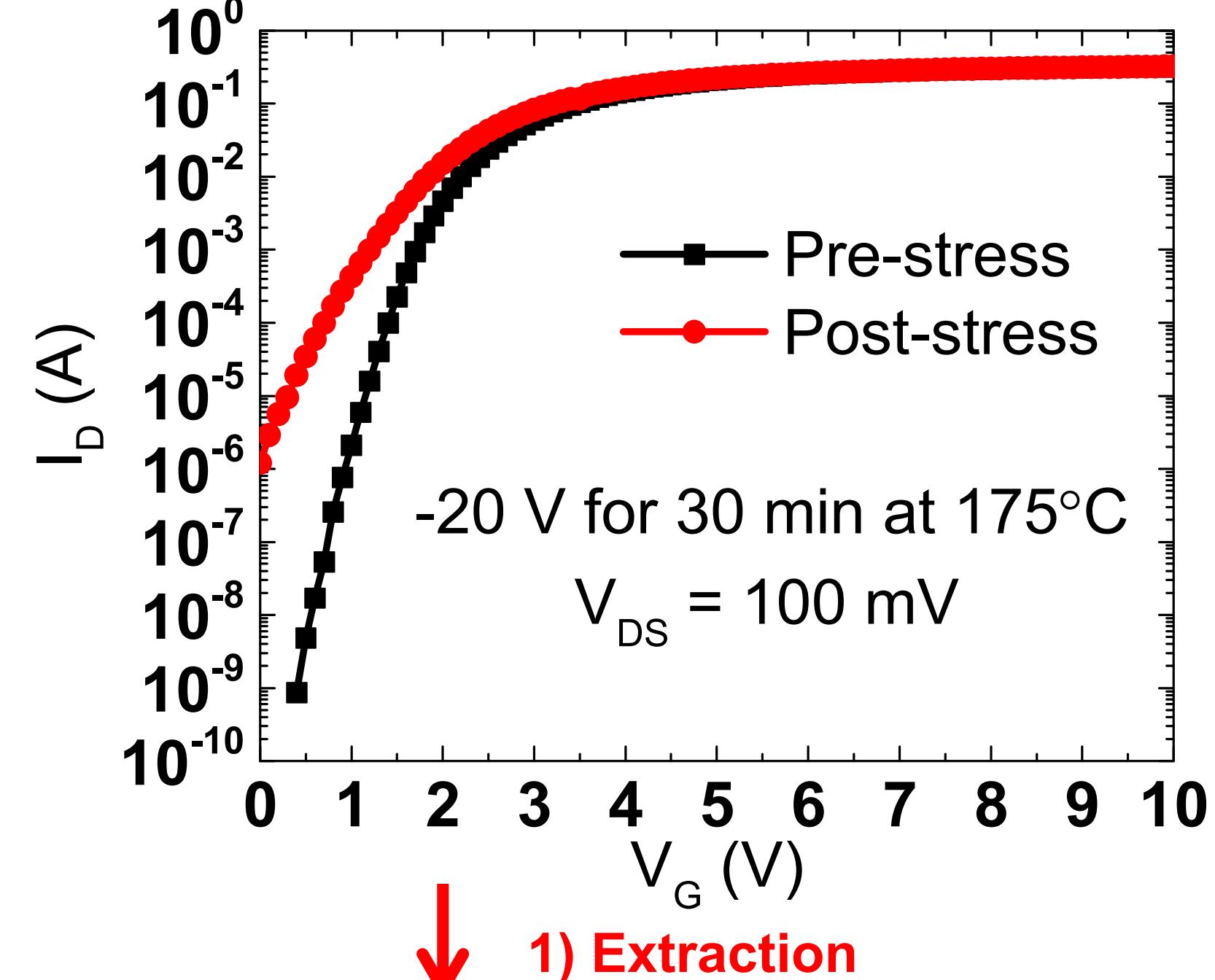
- $(V_{FB} + V_{IT})$ is solved for at each point

- D_{IT} is calculated over the intervals between points via:

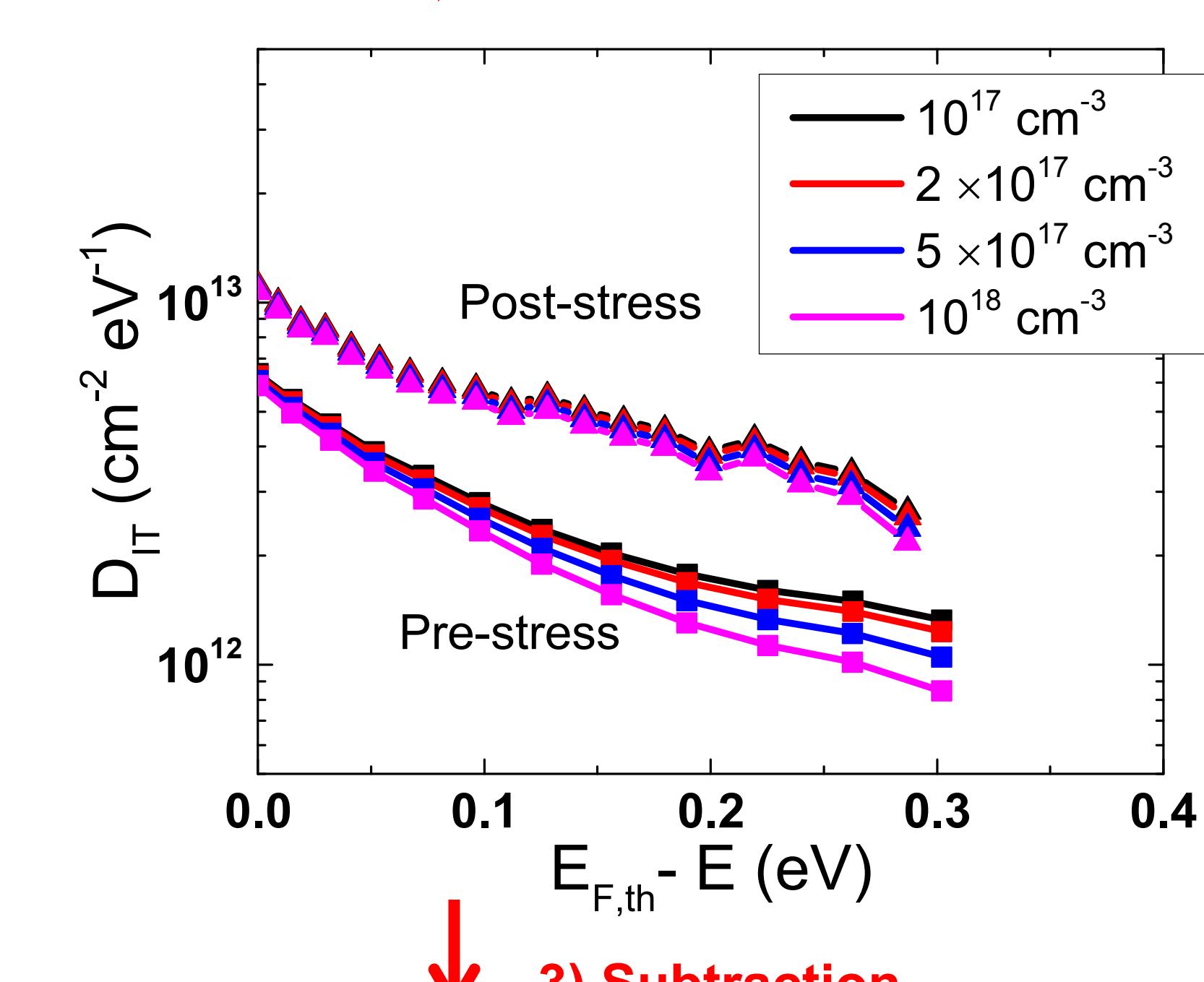
$$D_{IT} = \frac{C_i}{q} \times \frac{\Delta V_{IT}}{\Delta \varphi_s}$$



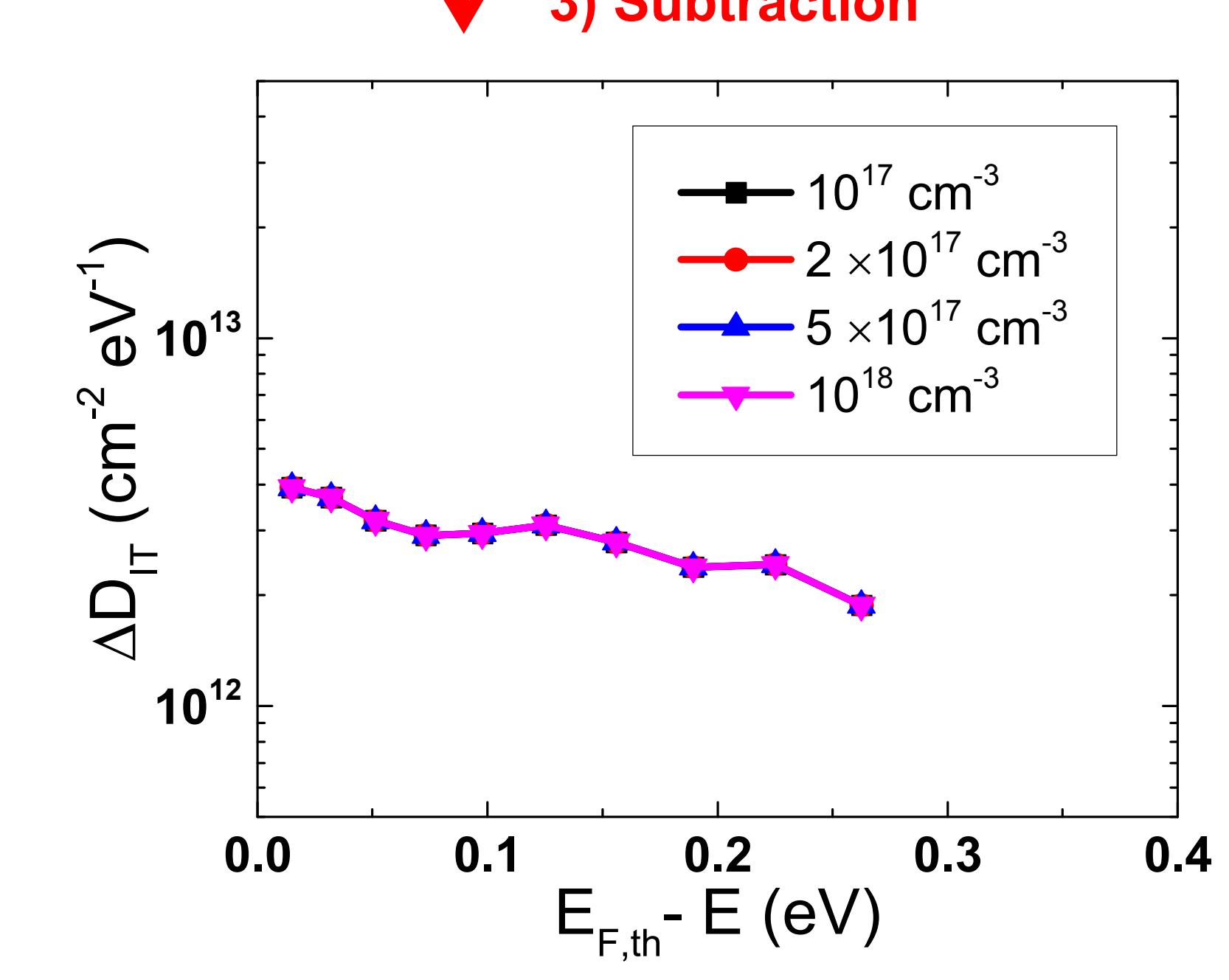
RESULTS



- Variation in assumed doping values causes shifts in the D_{IT} profiles



- Varying the assumed doping changes the bulk potential, altering φ_s at V_{th}



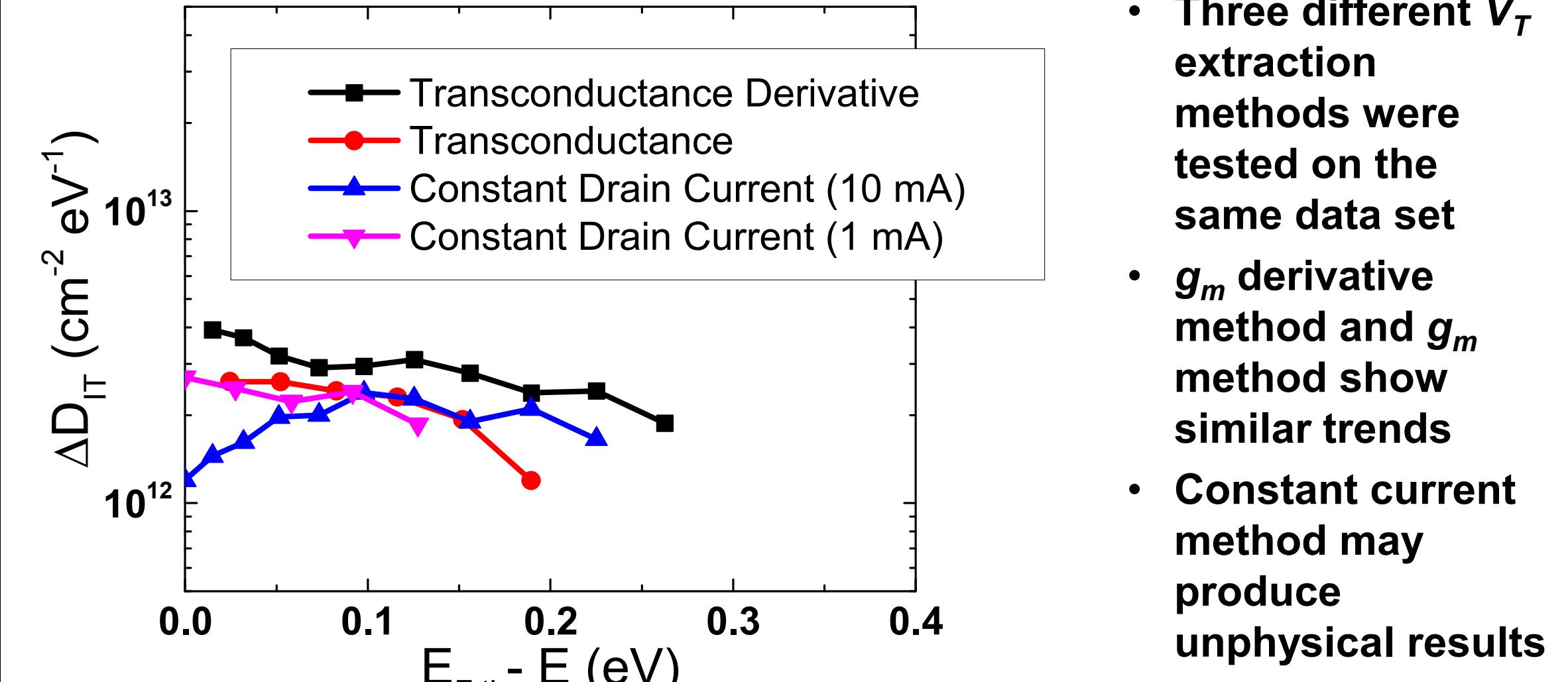
- D_{IT} profiles can be aligned by normalizing the energy level to the Fermi level

- Variations in assumed doping cause changes in calculated D_{IT} concentrations

- ΔD_{IT} profiles are independent of assumed doping concentration when referenced to $E_{F,th}$

DISCUSSION AND CONCLUSIONS

- Three sources of uncertainty: Doping, V_T selection, oxide thickness
- ΔD_{IT} has been shown to be independent of assumed doping



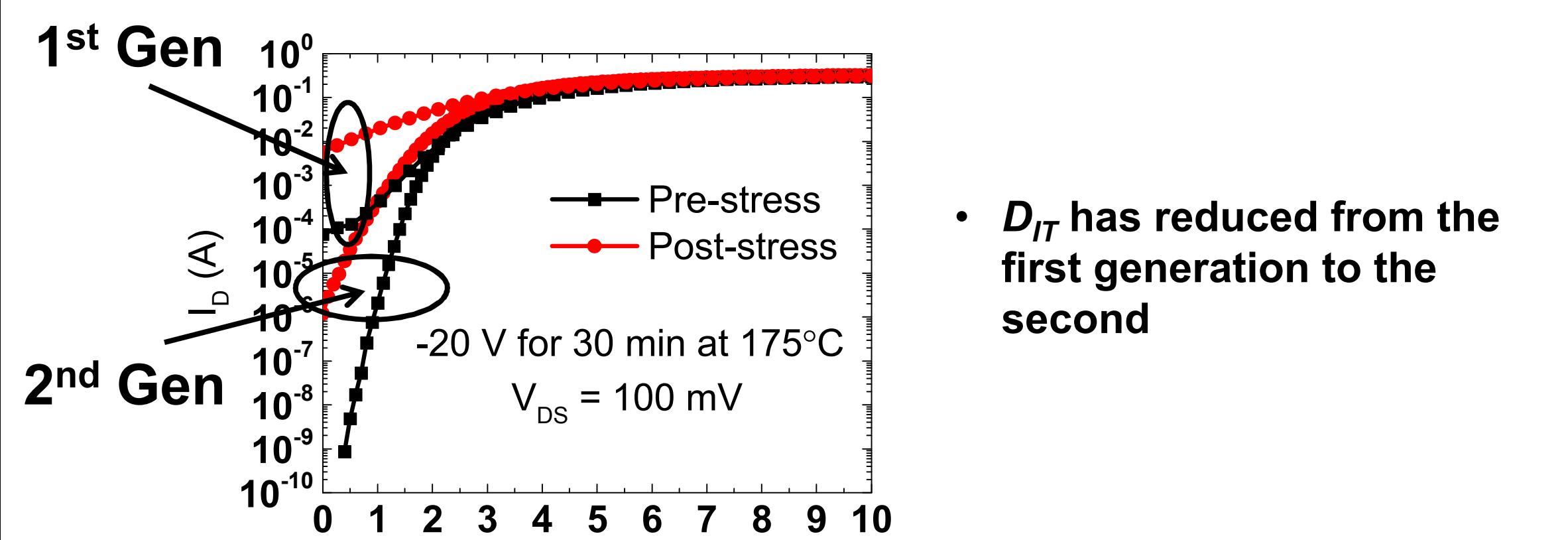
- Three different V_T extraction methods were tested on the same data set
- g_m derivative method and g_m method show similar trends
- Constant current method may produce unphysical results

- Calculated ΔD_{IT} varies with oxide capacitance
- Oxide thickness

- ΔD_{IT} changes by the ratio of the assumed C_{ox}
- 70nm/50nm = 1.4

- Typical oxide thickness range small

- ΔD_{IT} profiles for first and second generation SiC power MOSFETs have been extracted for identical stress conditions



- D_{IT} has reduced from the first generation to the second

- Less information for first generation devices
- Equivalent voltage sweep covers fewer energies due to higher D_{IT}
- Fewer data points on first generation I-V curves

- This method provides a fast and easy way to evaluate the effects of BT stress on SiC vertical power MOSFETs using only subthreshold curves
- Independent of assumed doping
- Threshold voltage extraction technique must be carefully considered
- Minimal effects of oxide thickness uncertainty

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