Microsystems
Science, Technology & Components

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Emerging Ferroelectric Memories: Critical Discussion

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Outline and Purpose

- Emerging FE Memories: Friendly-Critical Outlook
  - FeFET
  - FTJ
- Organized Discussion

Emerging Ferroelectric Memories had two “advocates,” hence this talk will bring up some of the critical points before the general discussion

2013 ERD FeFET Parameters

		A. Emerging Ferroelectric Memory		B. Carbon Memory	C. Mott Memory	D. Macromolecular Memory	E. Molecular Memory
Subclass		**FeFET**	**FE Tunnel Junction**	NA	NA	NA	NA
Feature size F	Best projected	Same as CMOS transistor	<10 nm	< 5 nm	5-10 nm	5 nm	5 nm
	Demonstrated	28nm	50 nm	22 nm	110nm	100 nm	30 nm
Cell Area	Best projected	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$
	Demonstrated	$4F^2$	not available	not available	not available	$4F^2$	not available
Write/Erase time	Best projected	< 100pS	<1 ns	not available	<1 ns	< 10 ns	<40 ns
	Demonstrated	20ns 10 ns	10 ns	10 ns	2 ns	15 ns	10s , 0.2s
Retention Time	Best projected	10 yr	>10 y	not available	not available	> year	not available
	Demonstrated	$2.5x10^5$s (3 days)	3 days	168 h @ 250°C	not available	10^5 s	2 months
Write Cycles	Best projected	$>10^{12}$	10^{14}	not available	$>10^{16}$	not available	$>10^{16}$
	Demonstrated	10^{12}	$4x10^6$	$5x10^7$	~100	10^5	$2x10^3$
Write operating voltage (V)	Best projected	not available	1 V	not available	not available	~ 1	80 mV
	Demonstrated	+/- 5	2-3 V	5-6V	1.25/0.75	1.4	4V, ~±1.5 V
Read operating voltage (V)	Best projected	not available	0.1 V	not available	not available	< 0.1	0.3V
	Demonstrated	0.5V	0.1 V	1.5V	0.2	0.2	0.5V , 0.5V
Write energy per bit	Best projected	0.1 fJ	1 fJ	not available	not available	0.1 fJ	0.1 aJ
	Demonstrated	1 fJ	10 fJ	not available	~1 fJ	10 fJ	not available
Research activity		30	27	52	31	80	21

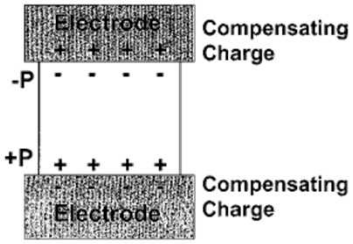
FeFET Key Issue: Retention

386 IEEE ELECTRON DEVICE LETTERS, VOL. 23, NO. 7, JULY 2002

Why is Nonvolatile Ferroelectric Memory Field-Effect Transistor Still Elusive?

T. P. Ma, *Fellow, IEEE,* and Jin-Ping Han, *Student Member, IEEE*

Abstract—**In principle, a memory field-effect transistor (FET) based on the metal–ferroelectric–semiconductor gate stack could be the building block of an ideal memory technology that offers random access, high speed, low power, high density and nonvolatility. In practice, however, so far none of the reported ferroelectric memory transistors has achieved a memory retention time of more than a few days, a far cry from the ten-year retention requirement for a nonvolatile memory device. This work will examine two major causes of the short retention (assuming in the ferroelectric**



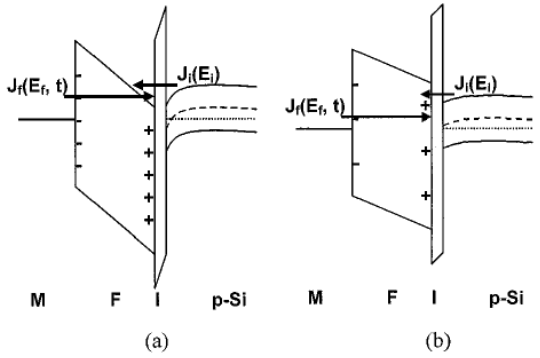
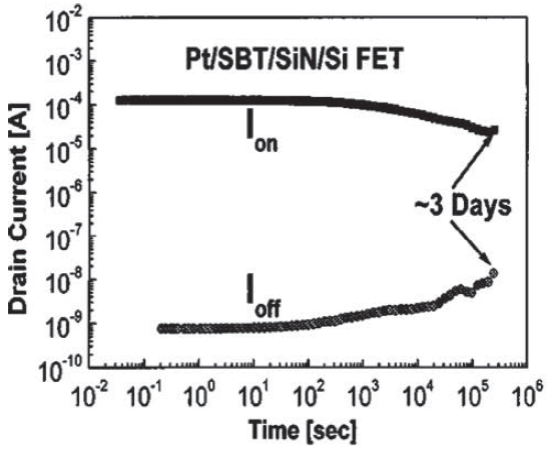


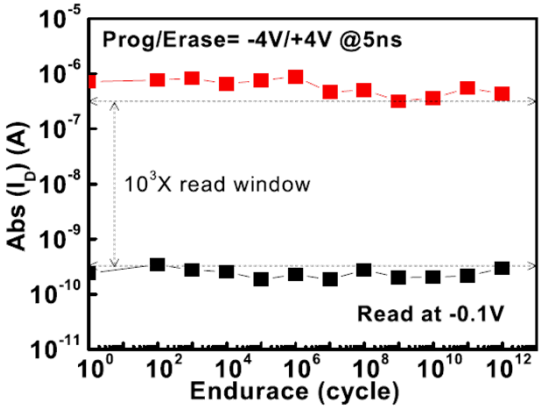
Fig. 3. (a) FEM gate stack has just been programmed such that the ferroelectric polarization induces an inversion layer in the p-type semiconductor. The FEMFET is in its "on" state and the electric field distribution favors electron injection toward the ferroelectric/buffer interface where some electrons are trapped in the dielectric stack and (b) sufficient electron trapping has taken place that results in diminished polarization effect and the semiconductor is no longer inverted. The FEMFET is in its "off" state.



HfO FeFET Tradeoffs
Voltage vs Retention vs Endurance

- **Retention**
  - **Projected 10 years at RT, however, best data is still 10^5 seconds (3 days)**
  - **Large write window requires 4-6V**
  - **DRAM-like : 4V,10^{12} cycles, but 300s retention**
  - **Tradeoff between endurance, write voltage, and retention**

Cheng and Chin, EDL 2014



Muller et al, VLSI 2012

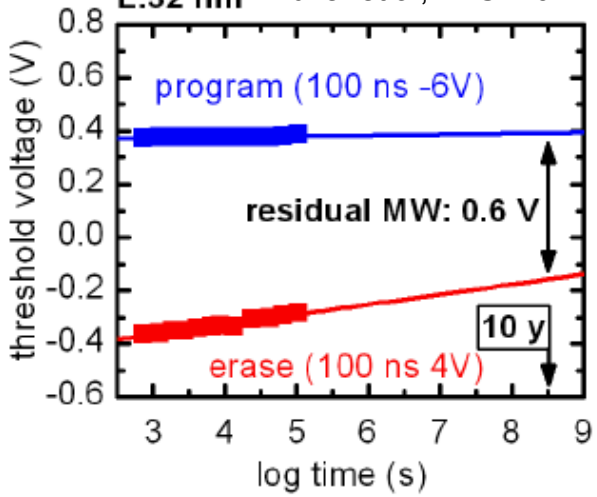


Fig 8. Low retention loss after cycling (10^2) is demonstrated. A memory window of 0.6 V after 10 years at RT is predicted.

Muller et al, IEDM 2013

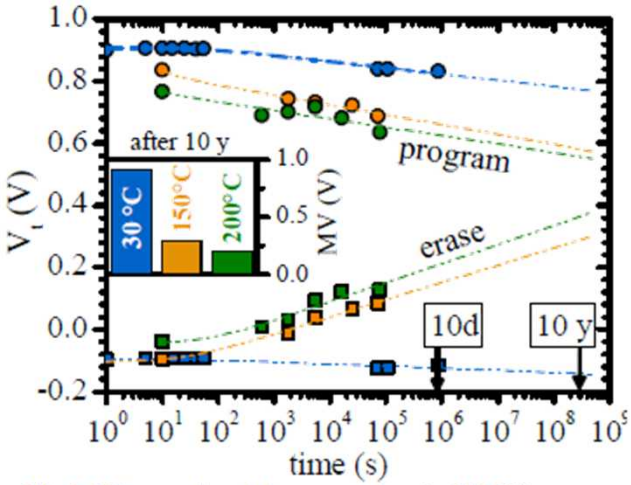


Fig 16 Extrapolated data retention in Si:HfO_2-FeFETs for RT, 150, and 200°C. A residual memory window after 10 years is extrapolated up to the highest temperature tested.

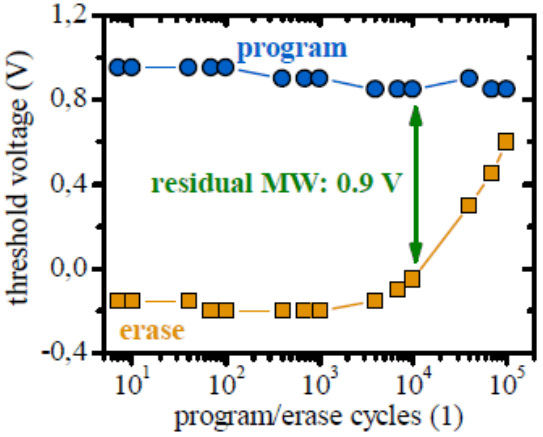


Fig 17 Endurance of Si:HfO_2-FeFETs is currently limited to 10^4-10^5 pgm/ers cycles. Further cycling degrades I_dV_g- and I_{on}/I_{off}-characteristics due to charge injection following the bipolar stress.

2013 ITRS ERD Memory Survey

- **FeFET perceived as a leading emerging memory technology**

	Overall	Scalability	Speed	Energy Efficiency	ON/OFF "1"/"0" Ratio	Operational Reliability	Room Temperature Operation	CMOS Technological Compatibility	CMOS Architectural Compatibility
ReRAM	18.7	2.9	2.5	2.1	2.2	1.6	2.5	2.4	2.4
FeFET	17.4	2.0	2.4	2.3	2.1	1.7	2.4	2.3	2.4
FTJ	17.3	2.3	2.2	2.2	2.1	1.7	2.4	2.1	2.2
Carbon-based	17.0	2.2	2.2	2.0	2.3	1.7	2.4	2.0	2.2
Mott	16.6	2.1	2.4	2.1	2.2	1.7	1.9	2.0	2.2
Macromolecular	13.9	1.8	1.7	1.7	1.6	1.3	2.2	1.7	1.8
Molecular	13.9	2.6	1.7	2.0	1.3	1.1	2.0	1.6	1.8

Scalability key perceived drawback…
Due to FET structure?

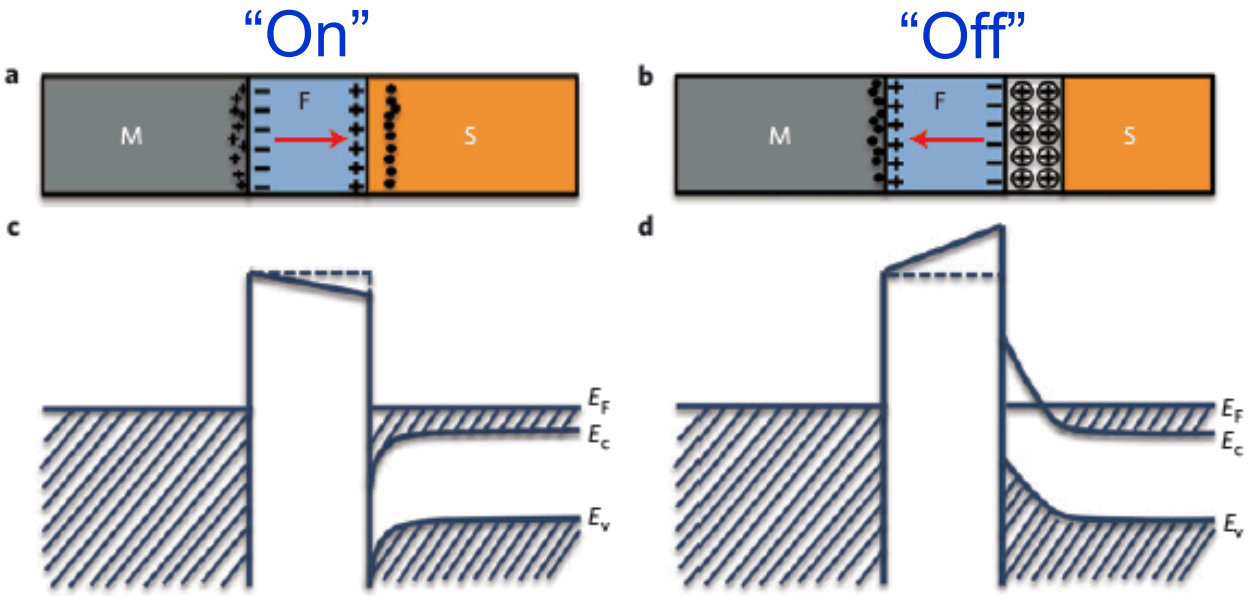
FeFET Perspective

- There are still some questions about the FeFET capabilities
  - Retention may not be adequate for S-SCM, esp at operating temperatures (85°C)
  - Improved retention requires higher set voltage
  - Scaling: transistor structure limits scaling to CMOS
- Hence, may not be suitable for S-SCM, or flash replacement
- However, for M-SCM, FeFET may have advantages over STT-RAM

Ferroelectric Tunnel Junction

FTJ physical mechanism:

- **Metal/Ferroelectric/Metal or Metal/Ferroelectric/Semiconductor**
- **Tunnel barrier is modulated by polarization direction**
- **TB height controls resistance between electrodes**
- **Resistive switching, hence can use crossbar configuration**



Wen et al, Nature 2013

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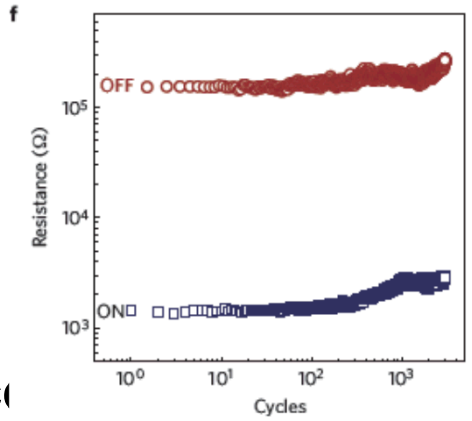
Due to traditional ferroelectric materials?

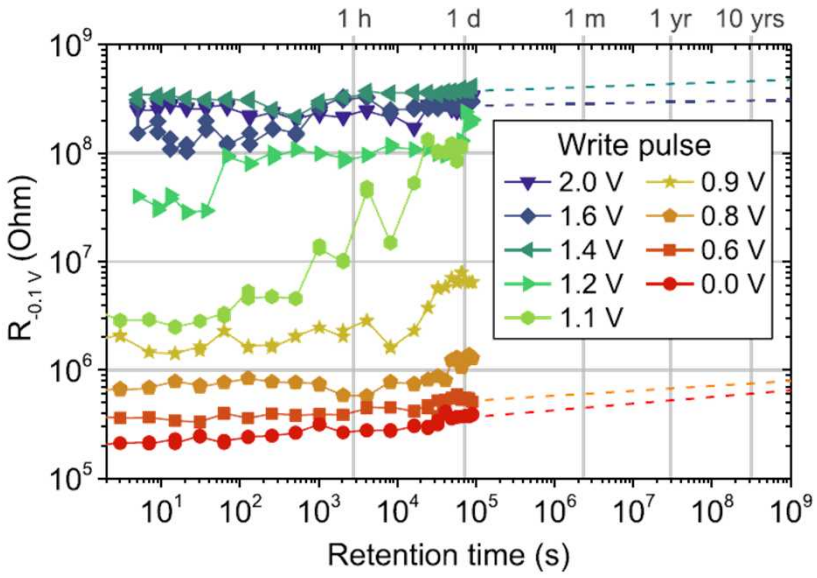
Drawbacks of FTJ

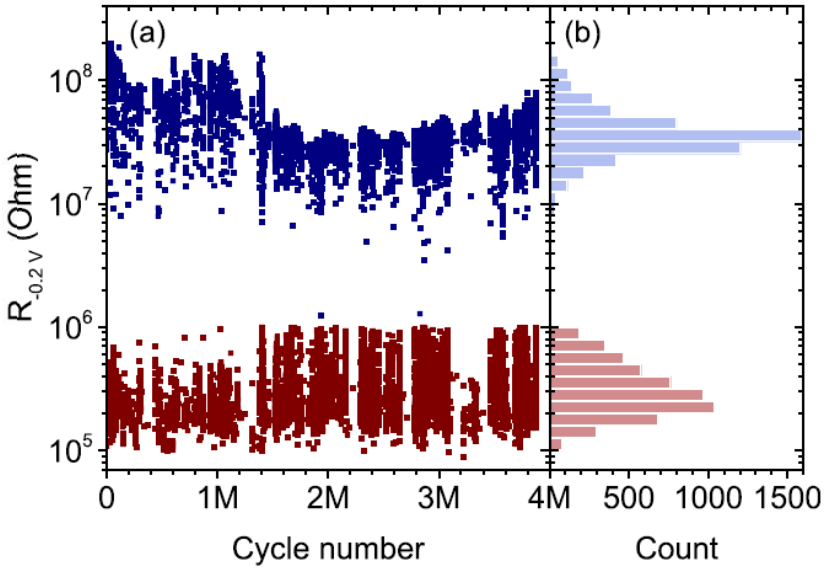
- Requires traditional FE material, e.g. BTO
  - Difficulty integrating into CMOS process
  - Sensitive to contamination
- Max published endurance: 4x10^6 cycles
- Max retention: ~3 days (tradeoff with endurance)
- Relatively new – little statistical reliability data

Wen et al, Nature 2013



Boyn et al, APL 2014





FTJ Perspective

- Similar to ReRAM (ionic)
  - Bipolar resistive switching device
  - Crossbar configured
- Hence, may be a viable competitor to ReRAM for S-SCM
  - Comparable or reduced switching energy
  - Comparable switching time
  - These properties will most likely be determined by line RC
- However, some disadvantages over ReRAM
  - Requires perovskite – integration more challenging
  - Retention may not be adequate for S-SCM
  - Questionable scalability below 10 nm
- Pessimistic point of view:
  - Advantages over ReRAM for S-SCM are not great enough to justify added integration expense

But…maybe reliability will be better than ReRAM…

Possible Discussion Topics

- What are the fundamental scientific and technological challenges for Emerging Ferroelectric Memories?
- Where do FE fit in the application space?
- What are the advantages of FTJ over ReRAM for S-SCM?
- What are the advantages of the FeFET for M-SCM?
  - Over STT-RAM?
  - Traditional SRAM, or integrated DRAM?

Application Space

	Embedded NVM Replacement[1]	NAND Flash Replacement (e.g. SSD)[2]	S-Type Storage Class Memory[3]	M-Type Storage Class Memory[3]	Stand-Alone DRAM (DIMM) Replacement[4]	CMOS Integrated DRAM/Storage/Main Memory[5]
Time to Implementation	**Now**	**5 years**	**5 years**	**5-10 years**	**5-10 years**	**> 10 years**
Quantitative Requirements						
Min Bit Level Endurance	10^3-10^6	10^3	10^6	10^9	10^{16}	10^{16}
Min Bit Level Retention	10 y	6-12 months	10 y	5 days	64 ms	10 y
Max System Level Read/Write Latency	100 µs	100 µs	5 µs	200 ns	100 ns	10 ns
Max System Level Write Energy	10^4 pJ	100 pJ	25 pJ	100 pJ	100 pJ	1 pJ
Max Feature Size	180 nm	12 nm	20 nm	20 nm	20 nm	10 nm
Min 2D Layer Density	10^9 bit/cm	10^{11} bit/cm	10^{10} bit/cm	10^{10} bit/cm	10^9 bit/cm	10^{11} bit/cm
Max Cost	30 $/GB[6]	2 $/GB	4 $/GB	10 $/GB	10 $/GB	10 $/GB
Qualatative Requirements						
Performance	Low	Low	Moderate	High	High	High
Reliability	High	Low/Moderate	Moderate	Moderate	Moderate	High
CMOS Compatibility	Required	Useful/Not Req	Useful/Not Req	Useful/Not Req	Useful/Not Req	Required
BEOL Process	Required	Not Required	Not Required	Not Required	Not Required	Required
Layering Capability	Not Required	Required	Required	Useful/Not Req	Required	Required

1: Based on common embedded microcontrollers with flash based program/data memory

2: Based on modern NAND flash characteristics, considering a stand-alone module.

3: Based on SCM info from 2013 ITRS ERD Tables

4: Based on modern DRAM characteristics.

5: High performance logic CMOS integration based on estimated requirements for data-center level processor (e.g. a "nanostore" [6]). This could also be thought of as a "univeral memory" which does not require tradeoffs in performance or reliability.

6: Based on the cost of a standalone external microcontroller memory; information on the cost per bit of flash integrated in a microcontroller is not available.

Additional Slides

Other drawbacks of FeFET

- Doped HfO has solved several traditional problems
  - Non CMOS materials in gate stack
  - Sensitivity to contamination
- Requires a FET structure
  - This limits scaling potential
- Ferroelectricity in doped HfO is a recent discovery
  - Physical mechanism not yet well understood
  - HfO FeFET devices not yet widely explored