State-of-Art (SoA) System-on-Chip (SoC) Design
HPC SoC Workshop

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Sandia Microsystems & Engineering Sciences Applications (MESA)

400,000 Sq-ft Complex with >650 Employees

Sandia National Laboratories

- **Trusted Digital, Analog, Mixed Signal & RF Integrated Circuits Design** & Fabrication
- **Custom IC Design**
  - Secure microcontrollers
  - Analog/Digital/RF
  - IBM Trusted Foundry
  - Tamper Resistant
- Micromachining
- RAD Effects & Assurance
- Failure Analysis, Reliability Physics
- Test & Validation
- 3-D Integration Features

Compound Semiconductor Fabrication

Silicon Fabrication

Materials Research

- Compound Semiconductor Epitaxial Growth
- Photonics, Optoelectronics
- MEMS, VCSELs
- Specialized Sensors
- Materials Science
- Nanotechnology, Chem/Bio
- Mixed-Technology Integration & Processing
- III-V Semiconductor Devices
  - Neutron-Immune HBT
  - Rad-hard Optical Links
  - Solid-State RF Devices

Modeling, Simulation & Systems Integration

- Advanced Computation
- Modeling & Simulation
- COTS Qualification
- Advanced Packaging
- Custom Electronic Components
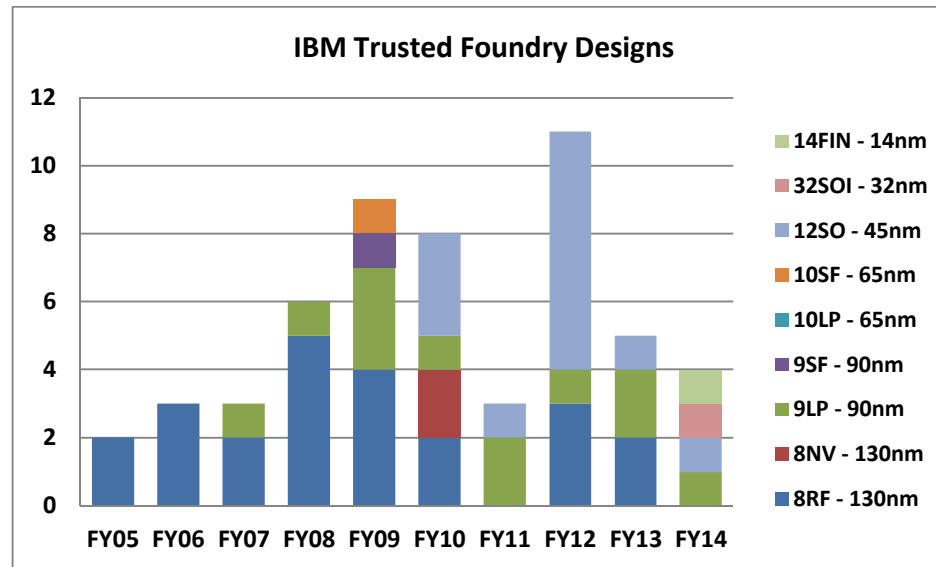- System Design & Test

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Sandia Microelectronics Development

- Develop *digital, analog, and mixed-signal integrated circuits (IC)* along with a deep understanding of technology offerings and design methodologies
- Develop *trusted* integrated circuits
  - Access to trusted resources and facilities for design, layout, fabrication, packaging, test, qualification, and product delivery assuring full chain-of-custody
    - On-shore, US owned, no foreign nationals
    - Security clearances, processes and/or facilities
    - DOD trusted accreditation
  - Mature relationship with IBM Trusted foundry using advanced technology
  - Access to other government trusted suppliers
- Develop *radiation hardened* integrated circuits
  - Access to strategic radiation hardened in-house technology
  - Radiation hardened by design for commercial technologies
- Develop *high-reliability* integrated circuits for *high consequence* systems
  - Weapons system components
  - Security-based and/or classified components
- Deliver *low volume* integrated circuits
  - Providing ICs where commercial industry cannot or will not supply

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Sandia Trusted Design

- Delivering ASICs from Sandia Radiation Hardened Trusted Foundry
  - Meets the needs for strategic radiation hardened programs
  - Flexible to accommodate research activities
- IBM Trusted Foundry: 52 Designs

IBM Trusted Foundry Designs

Legend:
- 14FIN - 14nm
- 32SOI - 32nm
- 12SO - 45nm
- 10SF - 65nm
- 10LP - 65nm
- 9SF - 90nm
- 9LP - 90nm
- 8NV - 130nm
- 8RF - 130nm

(Bar chart showing years FY05 through FY14 on x-axis, values 0 to 12 on y-axis)

- History and Experience with Other Trusted Suppliers
  - National Semiconductor Corporation Foundry
  - Honeywell Aerospace Foundry
  - Partnerships with Northrop Grumman
  - Jazz Semiconductor

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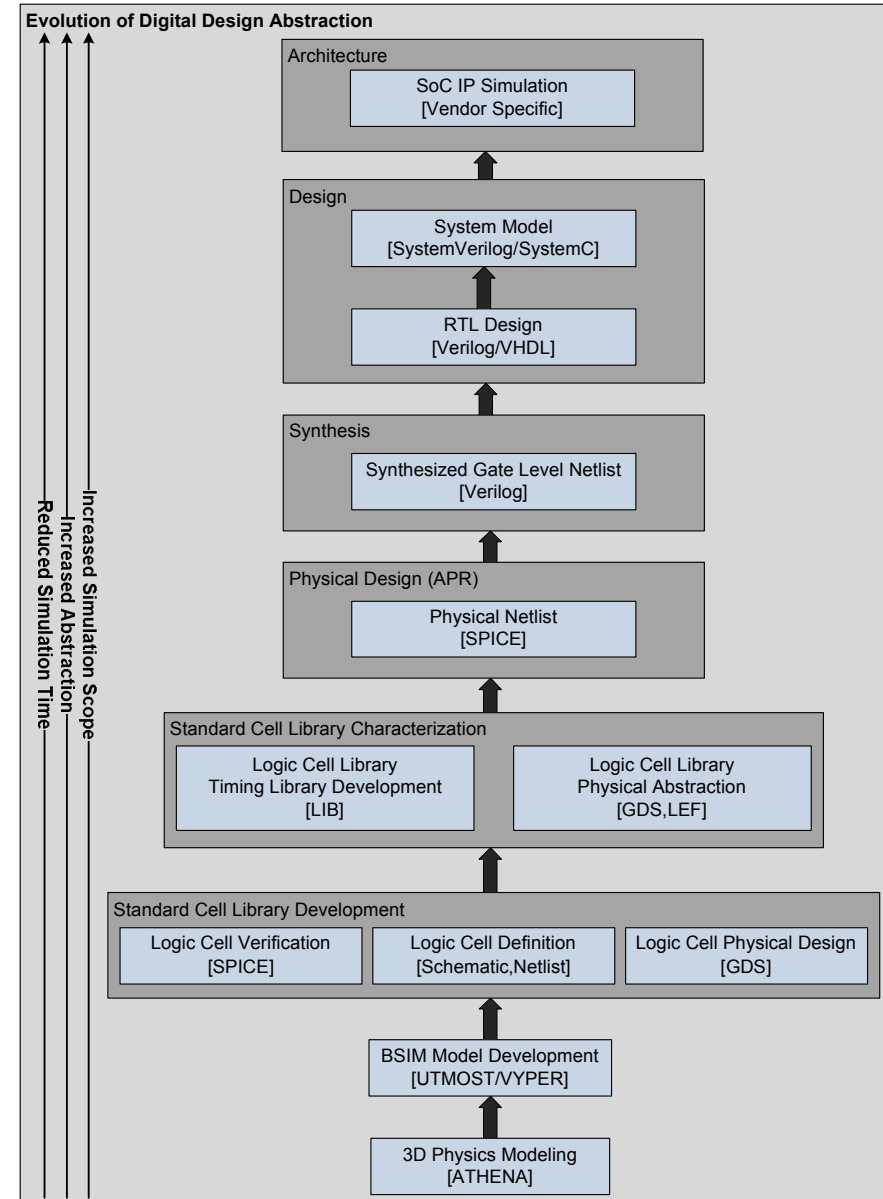# State of the Art Mixed Signal SoC Design

- **Full Mixed-Signal IC Design Flow**
  - Latest Industry EDA/CAD Tools
  - Mixed-Signal Verification & Co-Simulation
    - SPICE; Verilog-A; AMS; RTL
- **SoA SoC Verification**
  - Universal Verification (UVM)
  - Formal Verification
- **SoA Digital Synthesis Flow**
  - Topographical Synthesis
  - Power Aware (Clock Gating/Voltage Islands)
- **Intellectual Property (IP)**
  - Silicon Fabric/Motherboard SoC Design
  - Integration & Verification
  - Custom IP (Hard & Soft)
- **3D Integration & Verification Flow**
  - 3D Automated Place & Route
  - 3D Verification

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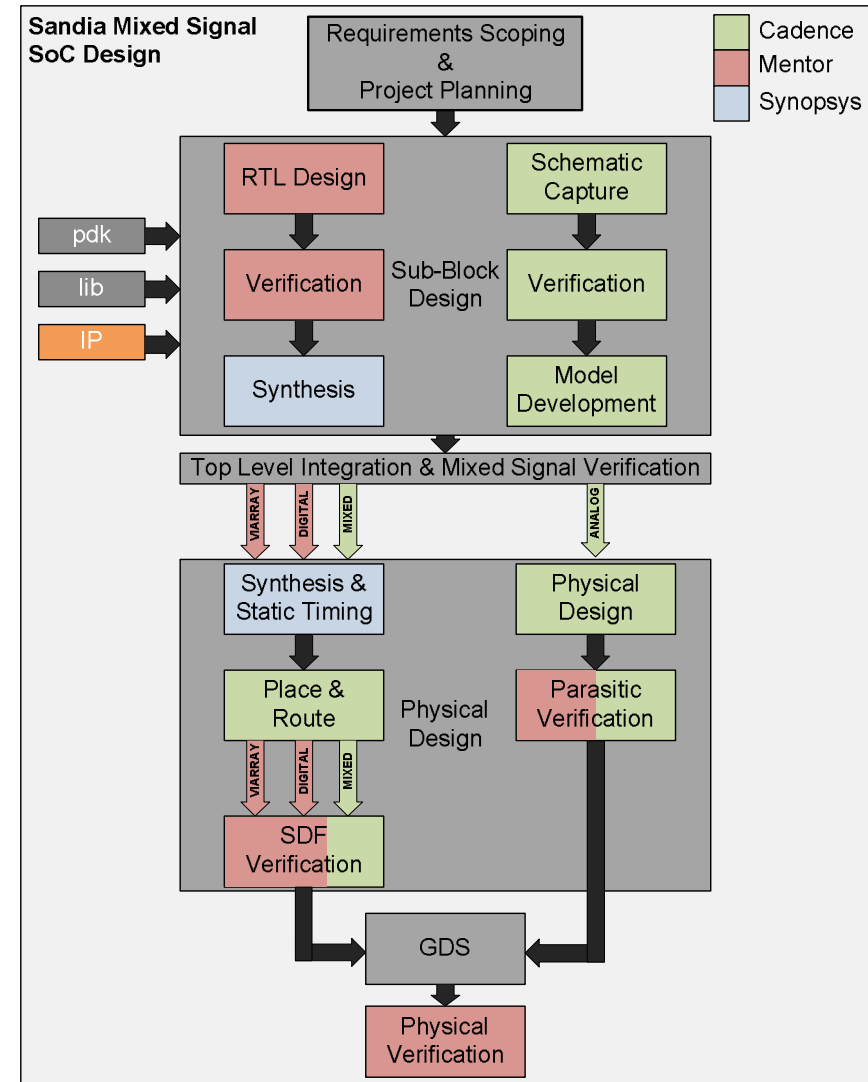
SoC Design Abstraction Evolution & HPC

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- Evolution of abstraction (Digital/Analog/AMS)
  - Driven by complexity, cost, & time to market
  - Analogous to the evolution of COTs PCB design
  - Chip scale architecture evaluation & trade space
  - Rapidly optimize architecture to the problem
- New hierarchy of designers in SoC development
  - System level designers drive architecture trades
  - Rapid prototyping & simulation tools
  - High performance, scalable, multi-core platforms
- Proliferation of suite of IP building blocks
  - Silicon fabric or motherboard (3D?)
  - Reduced cost and risk
    - Pre-verified IP with design kits
    - Verification suite
    - Optimized for yield and manufacturing
- FPGA SoC platforms
  - Traditional FPGA benefits
  - Less flexibility

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Evolution of Digital Design Abstraction

Increased Simulation Scope
Increased Abstraction
Reduced Simulation Time
Increased Simulation Time

Architecture
SoC IP Simulation
[Vendor Specific]

Design
System Model
[SystemVerilog/SystemC]

RTL Design
[Verilog/VHDL]

Synthesis
Synthesized Gate Level Netlist
[Verilog]

Physical Design (APR)
Physical Netlist
[SPICE]

Standard Cell Library Characterization
Logic Cell Library
Timing Library Development
[LIB]

Logic Cell Library
Physical Abstraction
[GDS,LEF]

Standard Cell Library Development
Logic Cell Verification
[SPICE]

Logic Cell Definition
[Schematic,Netlist]

Logic Cell Physical Design
[GDS]

BSIM Model Development
[UTMOST/VYPER]

3D Physics Modeling
[ATHENA]

# 3D Integration Development & Commercial Adoption

- Niche applications with specialized process flows
- Requires specialized processing, tools, materials research
- Additional yield loss in handling and process steps
- New design and test paradigms
  - Limited CAD tool support (custom flow development)
  - Combined assembly & test for yield (known good die)
- Limited by additional cost of 2.5D/3D fabrication
  - Through Silicon Via's (TSV)
    - Precision Etch & Singulation
    - Liner Deposition & Metal Fill
  - Bonding
  - TSV Exposure
    - Backgrinding and Thinning

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3D Integration Considerations
Custom u-Systems & Heterogeneous Integration

- Layer-to-Layer Interconnect Density

- TSV Requirements (diameter, pitch)

- Stacked Alignment Accuracy

- Tiling Accuracy Placement Requirements

- Wafer Level vs. Die Level Requirements & Assembly

  - Most High Density Processes Require Wafer-To-Wafer Bonding

    - Wafer level processing required to define TSV's and interconnect layers

    - Wafer level processing required to thin wafer backside to reveal TSV's

  - Wafer Level Fabrication At Advanced Technology Nodes Can Be Cost Prohibitive

  - Costs Are More Manageable Using Multi-Project Wafer (MPW) Runs

    - Wafer contains designs for other users; Only die are ultimately available, which can complicate 3D processing approach

    - Circuitry must be partitioned to contain interconnect density

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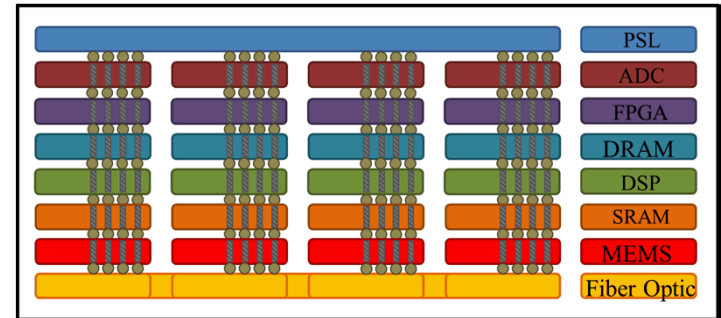
Commercial Trends

- **2.5D will continue to see extended use and will dominate market first**
  - Easy adoption (evolutionary not revolutionary)
- **3D Drivers**
  - High performance processors to overcome bandwidth limitations and improve power performance
  - Mixed-signal designs in which analog functionality does not benefit from node shrink (cost savings)
  - Higher cost of adoption, requires new paradigm in design
  - Heterogeneous integration may offset cost of adoption long-term
- **Applications drive development**
  - High Density Interconnect:
    - Pixelated sensors require high density interconnect, small pitch, millions of connections
    - Can tolerate less than 100% functionality (a dead pixel is "ok")
  - Low/Medium Density Interconnects:
    - High performance processors and custom heterogeneous solutions will drive low/medium density solutions.
    - Requires high yield and will tolerate larger interconnects.

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Recent Sandia Integrated Circuit Applications

- **Focal Plane Array Design**
  - Remote Sensing
  - High Speed X-Ray Imaging
  - Advanced Packaging & 3D Integration
- **NW Program Support**
  - Secure Processing
  - Full Custom Analog
- **Secure Processing**
  - NSA Certified Designs
- **Technology Assessments**
  - Memory Characterization
  - Fundamental Device Response
- **Research Collaboration**
  - Physically Uncloneable Functions (PUFs)
  - Radiation Effects
  - Memristors
  - Exascale Computing
  - Sensors
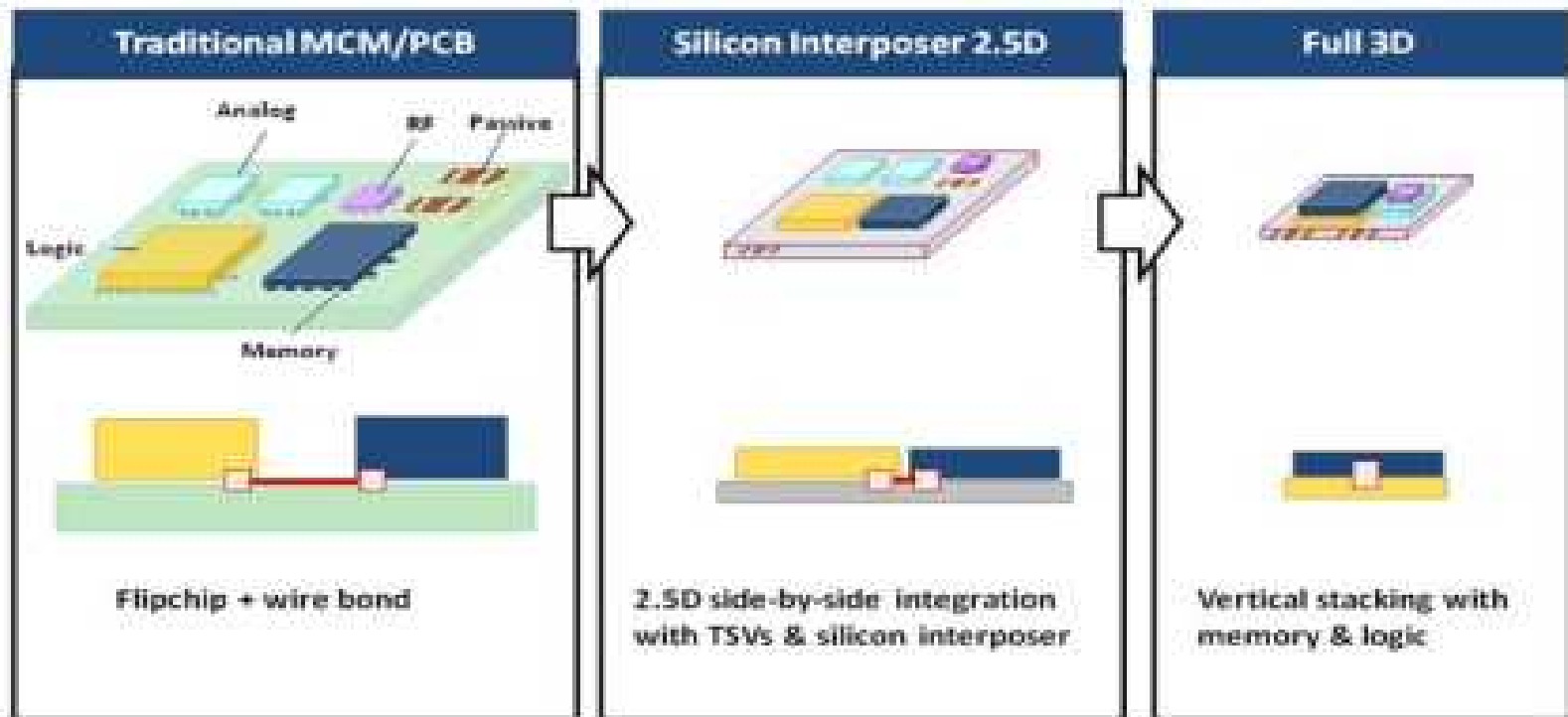
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Tiled 3D FPA Architecture
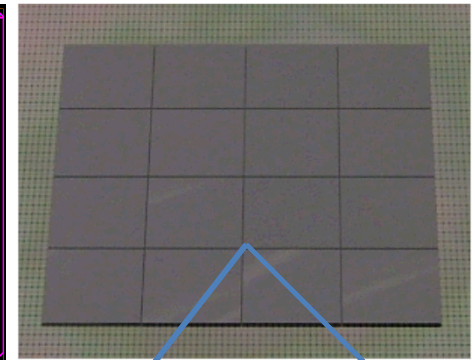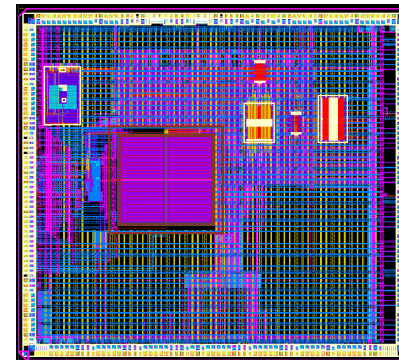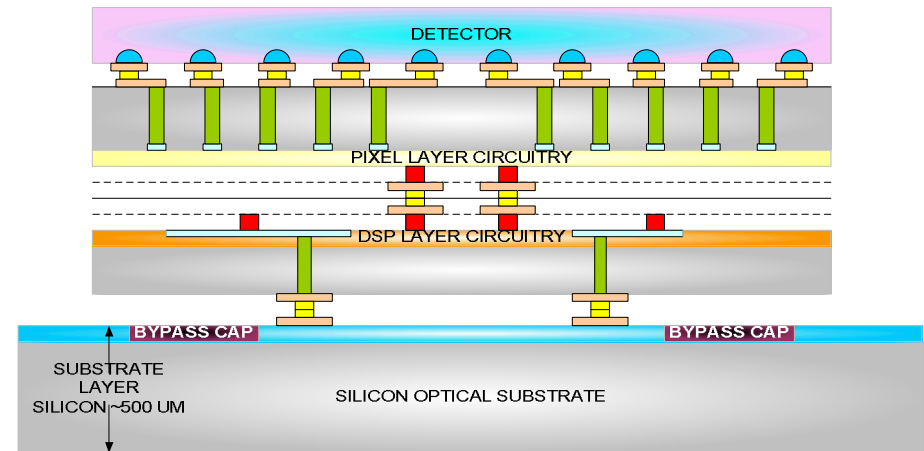
- **Large Format Array**
  - Precision Singulation
  - 4-Side Abutment
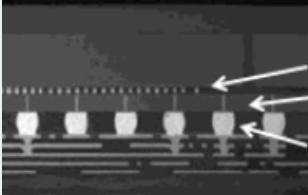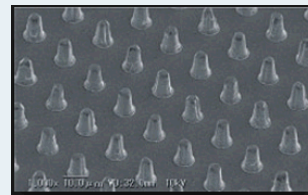 - Modular
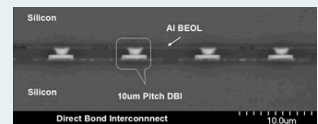 - Monolithic Detector
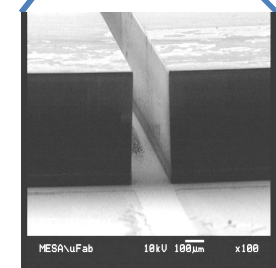
Backup

2.5D, 3D, 5.5D Integration

- 2.5D — Interposer Only Design (pcb evolution)
- 3D — Vertically Integrated (face-to-face & tsv)
- 5.5D — 3D+2.5D (Hybird memory cube + FPGA)

3D Bonding Technology

	C4	μBump	Indium Bump	DBI (Ziptronics®)
Density	Low	Moderate	Moderate	High
Minimum Pitch	300μm	150-20μm	10-15um	3μm
Method	D2D, D2W	D2D, D2W	D2D	W2W, D2W
Underfill	Yes	Yes	Yes	No
Maturity	High	High	High	Moderate
Images				

W2W   = Wafer-to-Wafer Bonding

D2W   = Die-to-Wafer Bonding

D2D   = Die-to-Die Bonding

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