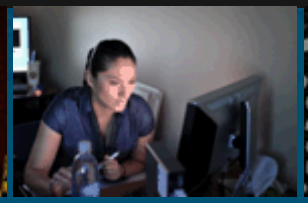
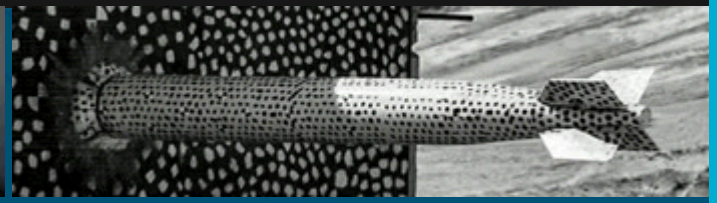
CMOS compatible processing for phosphorous delta-layer nanoscale electronics





PRESENTED BY

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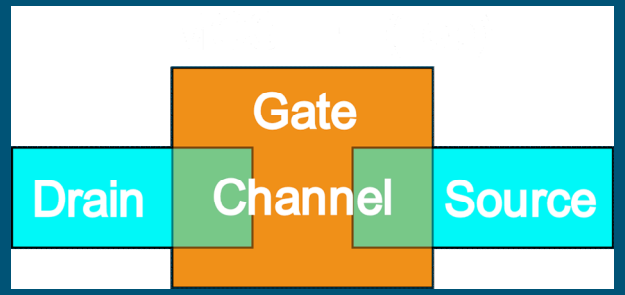
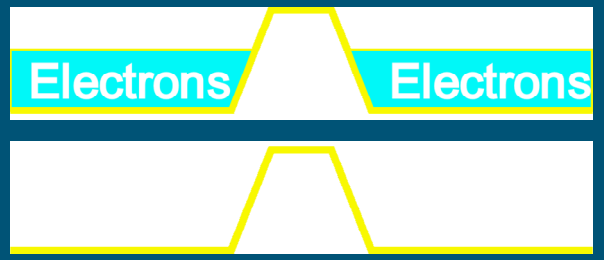
Phosphorous Delta-Layer Electronics

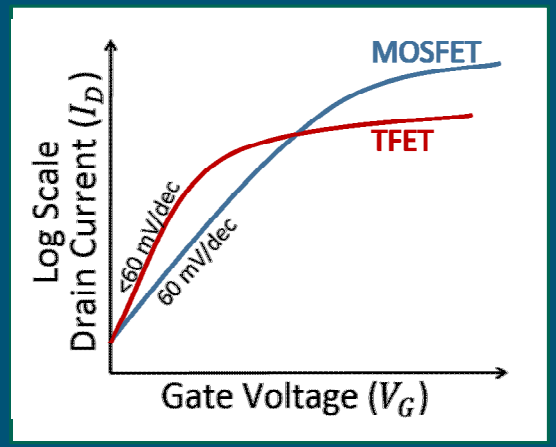
MOSFET:
- Thermionic emission modulation to overcome barrier.
- Limited by room temperature and thermionic emission

TFETs:
- Relies on band-to-band tunneling through a barrier
- Limited by the precision of fabrication.

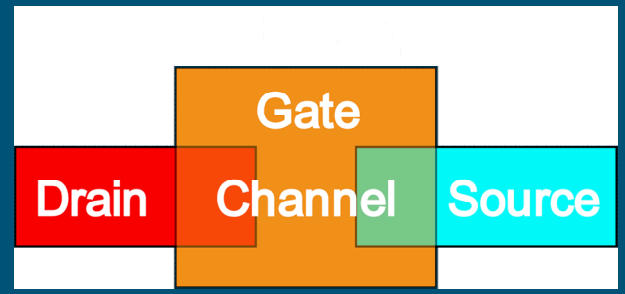


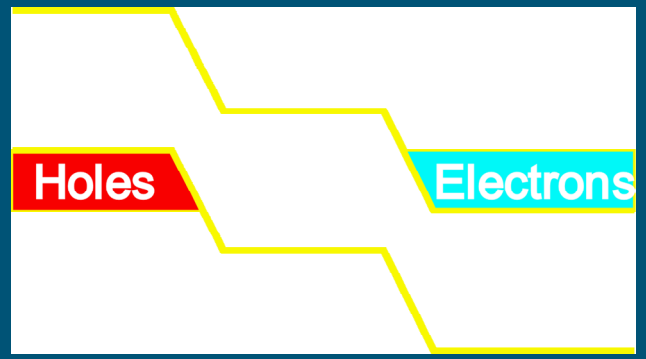


Thermionic emission



TFETs ideal for making ultra-efficient low power electronics

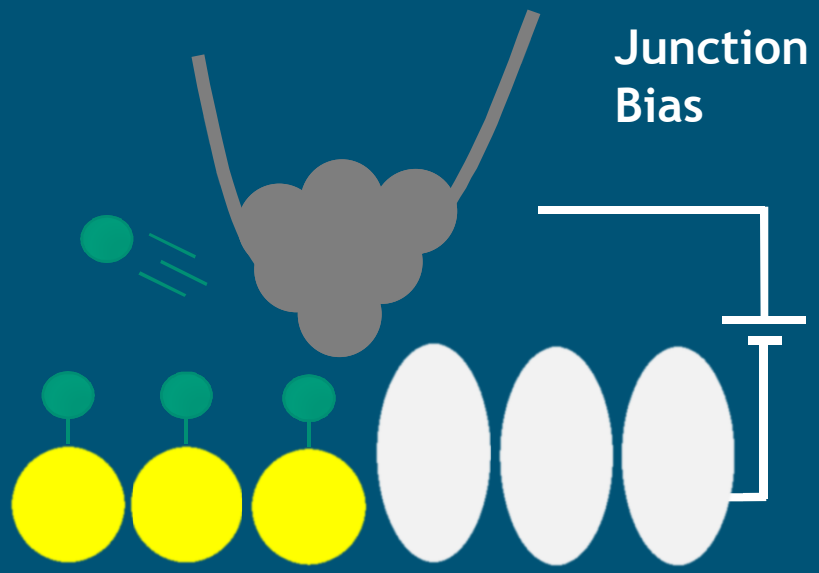


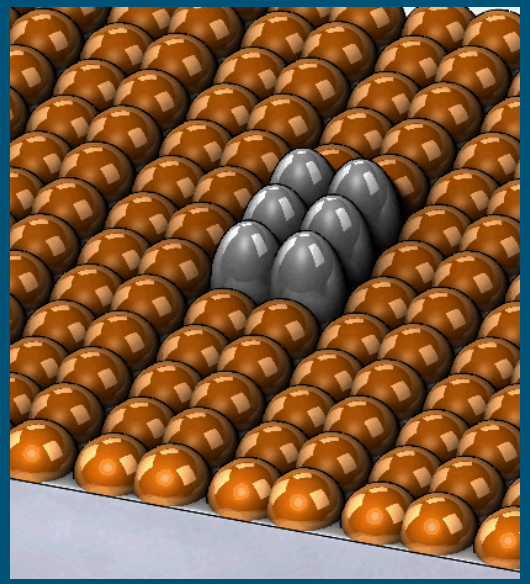


Band-to-band tunneling

Creating Atomically Precise TFETs with Scanning Tunneling Microscopy

TFETs power efficiency limited to precision of fabrication





Use hydrogen lithography via an STM to create an atomically precise TFET

A High Yield, High Throughput Fabrication Path

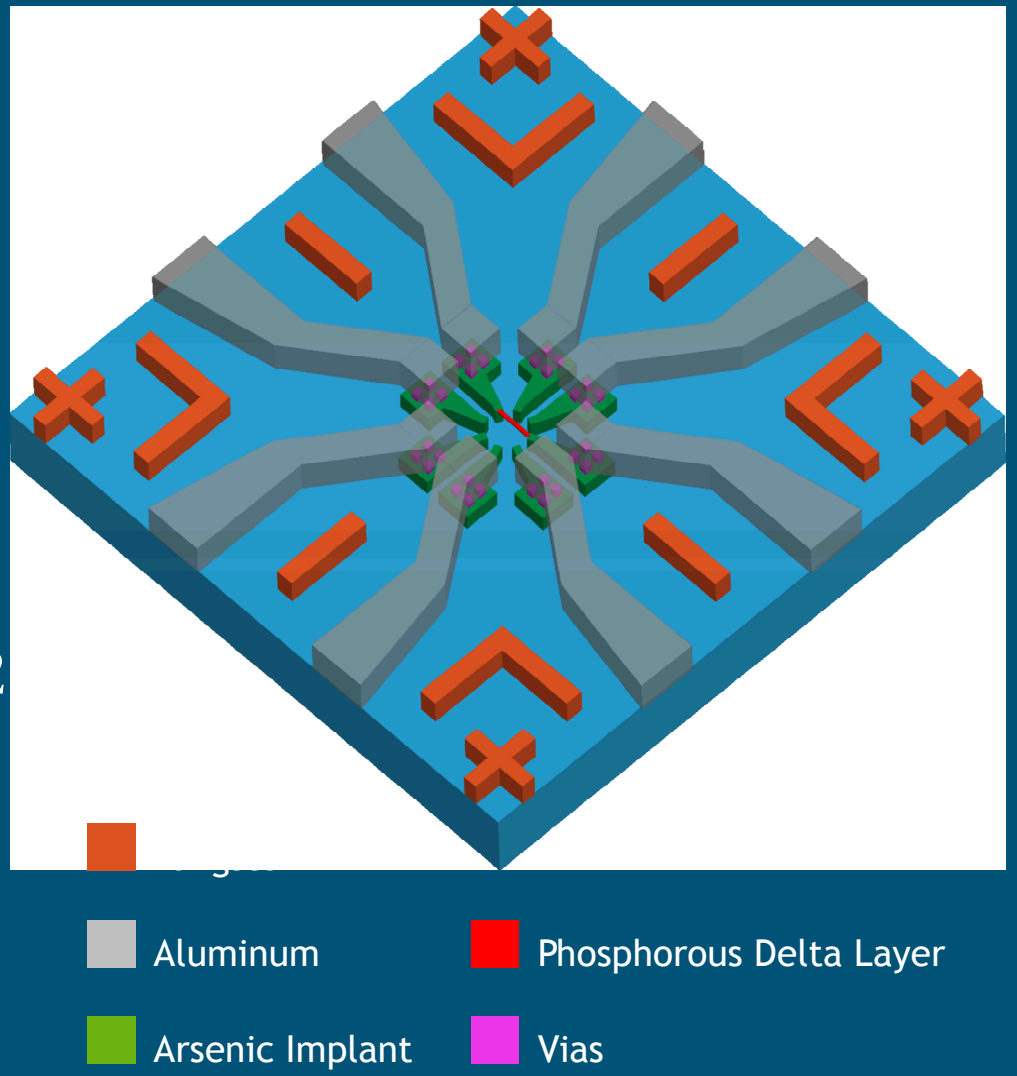
Low temperature STM sample prep

CMOS compatible

Eliminated need for E-beam lithography

Shortened process time from 1 month to 2

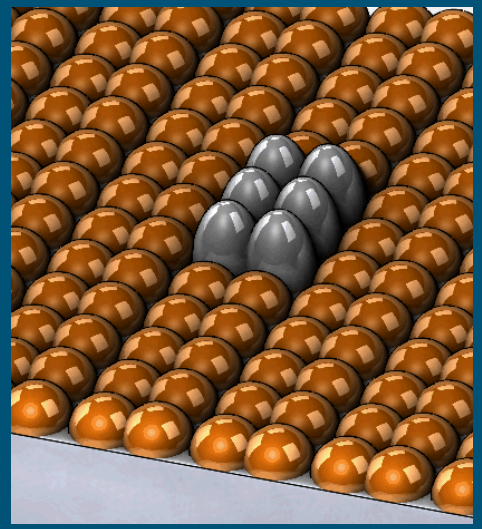
STM → Cleanroom → Measurement



D. R. Ward, *et al.* App. Phys. Lett. 111, 193101 (2017).

Fabrication Challenge – Contacting the Device

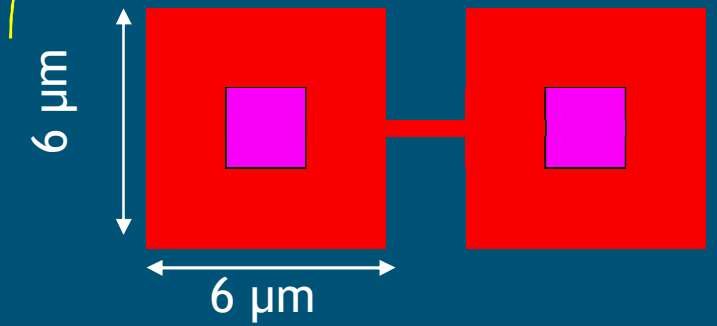
Atom by atom device patterning



Single µm size devices

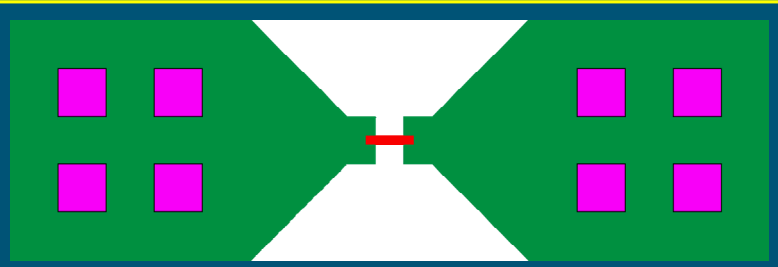
Contact Methods

Direct Contact



Direct contact with basic photolithography dedicates 99% of STM write time to making contacts

Indirect Contact via Implant



Implanted contacts allow for STM write time to focus on device

Use ion implantation for contacts

δ Layer

Via

Arsenic Implant

Tungsten

Implanted Device Contacts

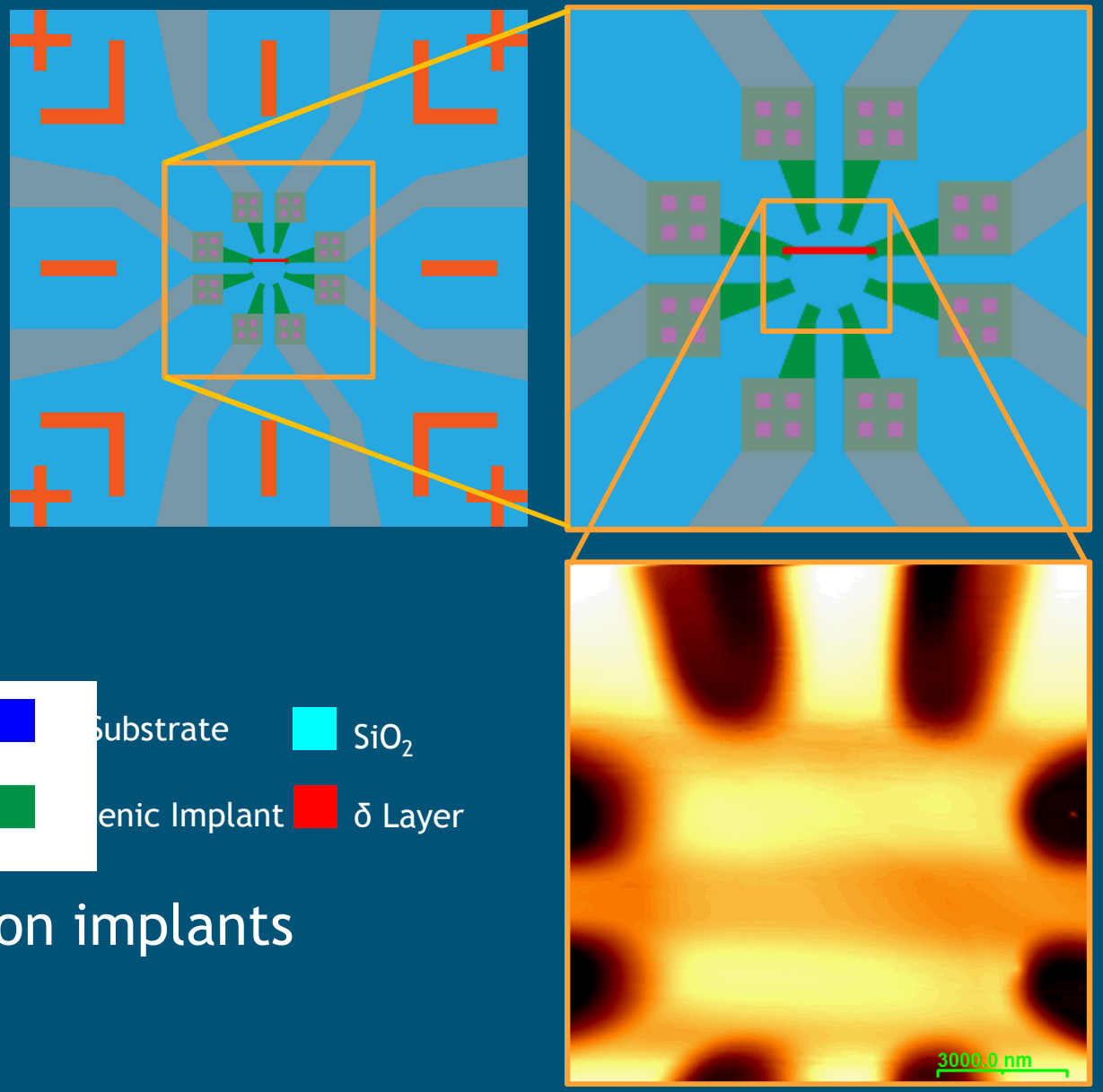
Previously done with comb design[1]

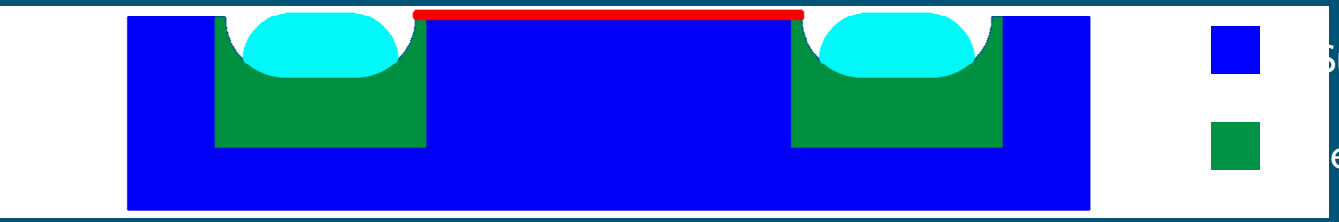
Heavy dopants (As) minimize surface & bulk diffusion

Contacts must be completed before STM process

Device dimensions 100 nm x 10 μm

Contact to ion implanted ohmics → extremely robust process

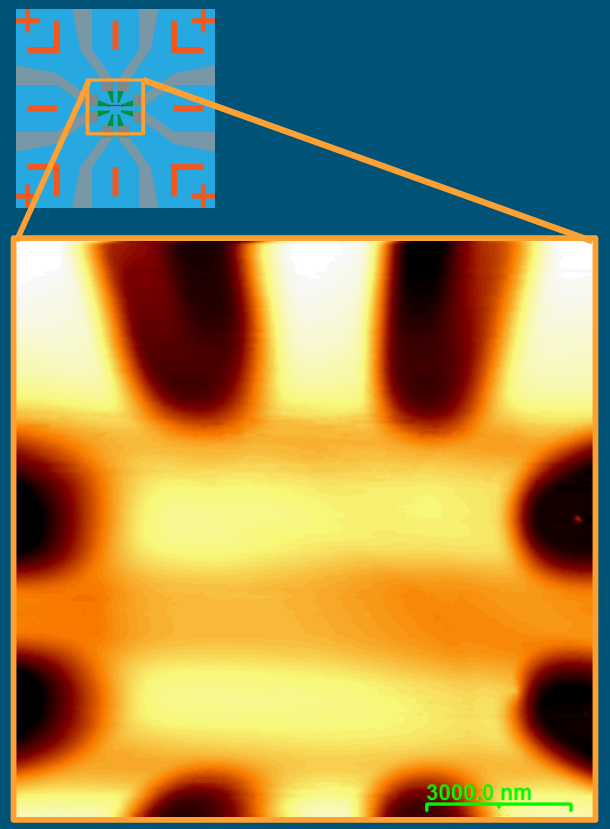




Directly pattern device between ion implants

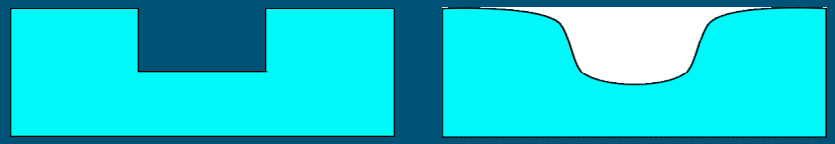
1. J. C. Kim, J. S. Kline, and J. R. Tucker, Appl. Surf. Sci. 239, 335 (2005).

Locating the device



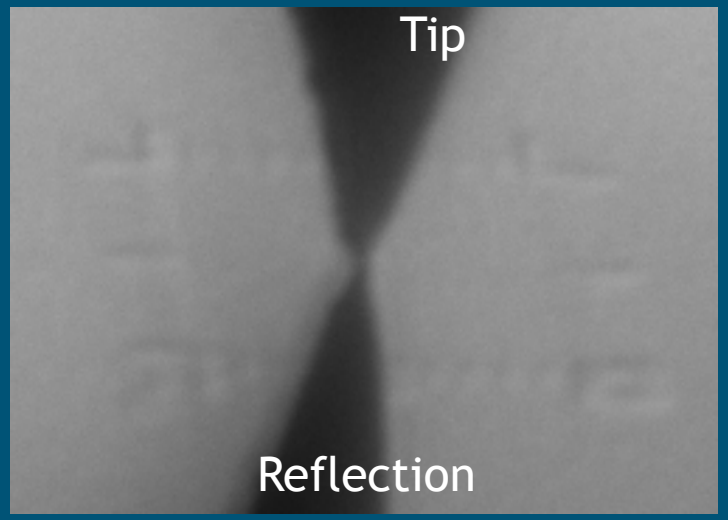
Ohmics visible in the STM but difficult to see in camera

Si Etch Marks



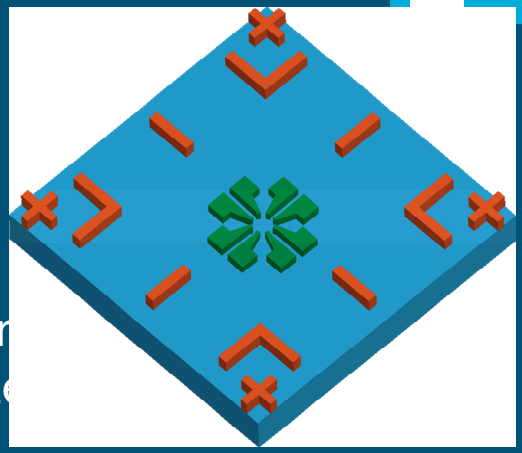
Before flash After flash

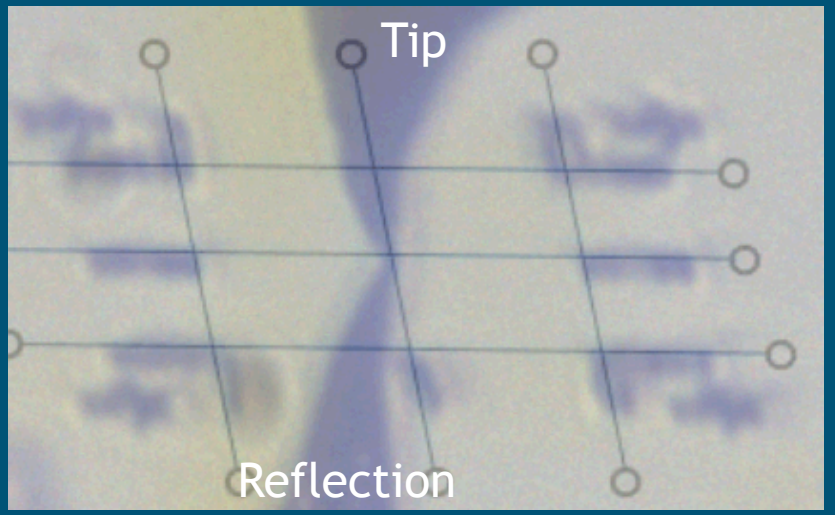
Cross-section views



Si etch marks have low contrast, soft edges after cleans

Solution:
Tungsten marker
alignment reticl





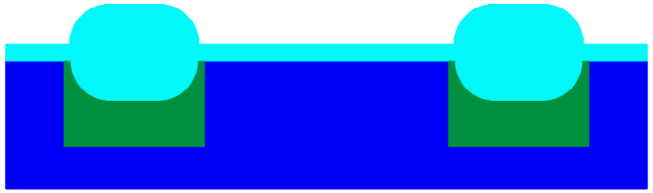
Repeated tip placement within 2 μm of the same location

Front-End-Of-Line Device Fabrication

1. Starting material is P-type (10-20 Ohm cm) Si (100) with a 10 nm pad oxide. Wafer level markers are etched into the Si.

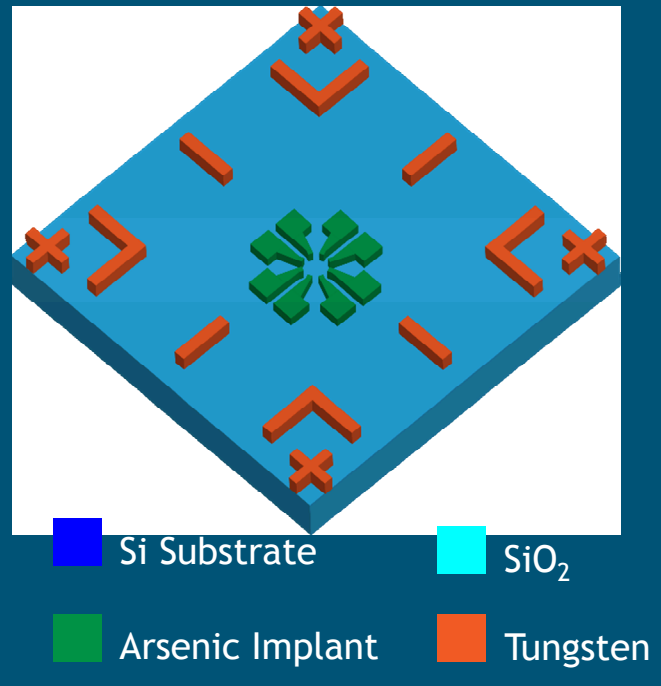
2. Arsenic ohmic contacts are implanted (40 keV, 3x1015 ions/cm2)

3. Pad oxide is stripped to expose clean Si



4. A 8-10 nm steam oxide is grown at 850C to activate the dopants and protect the device

5. Tungsten markers are deposited



Low Temperature STM Clean

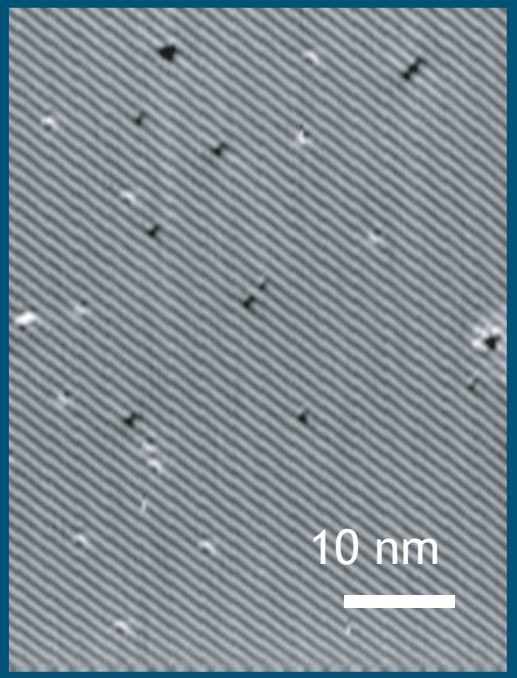
Clean requirements:

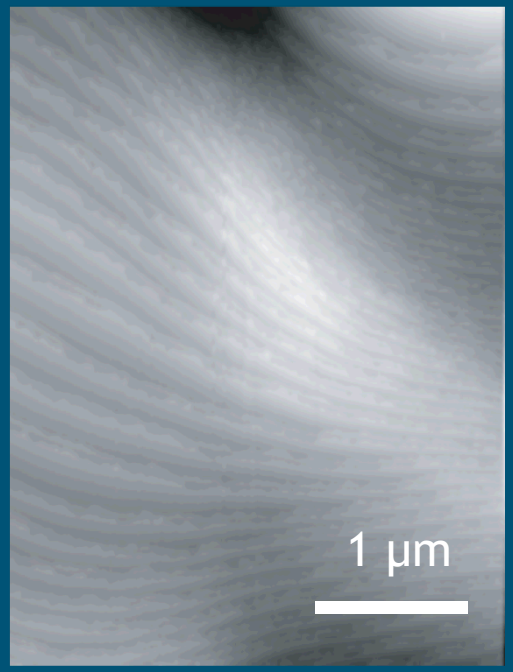
- Atomically clean
- W alignment marks must survive
- Minimize dopant diffusion

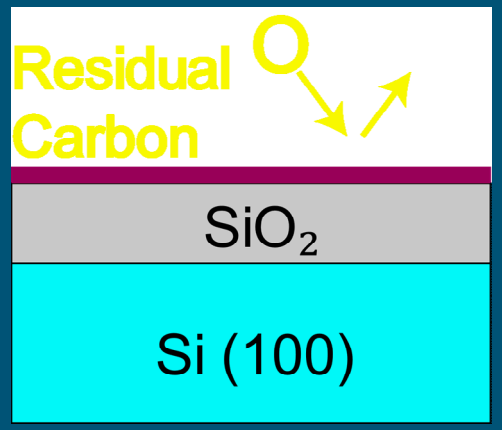
Can not use typical STM clean process:

- RCA1/RCA2 cleans
- 1200C flash of sample in STM

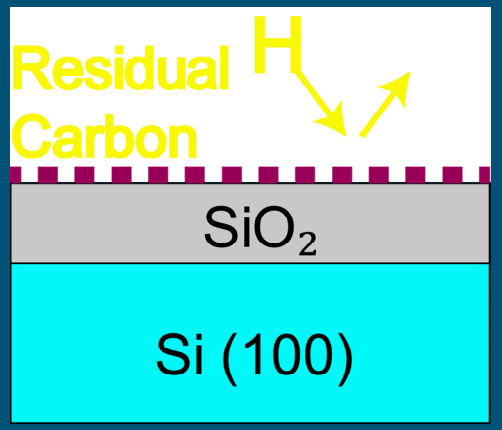
Solution: Low temperature clean



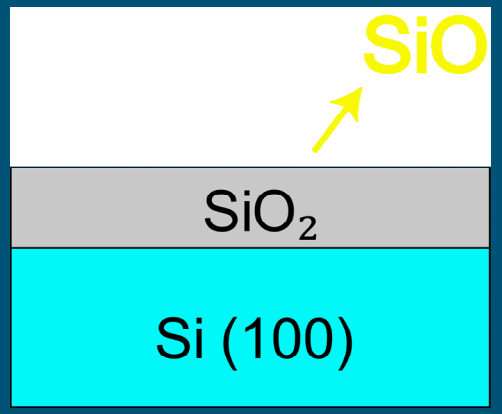




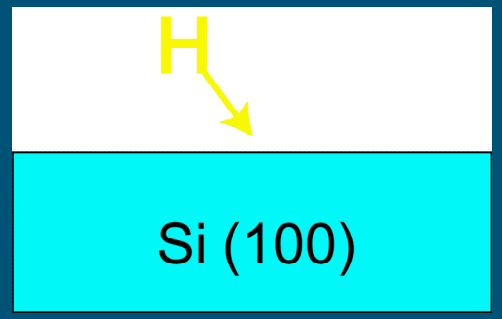
Oxygen Plasma Clean



600C Hydrogen Bake



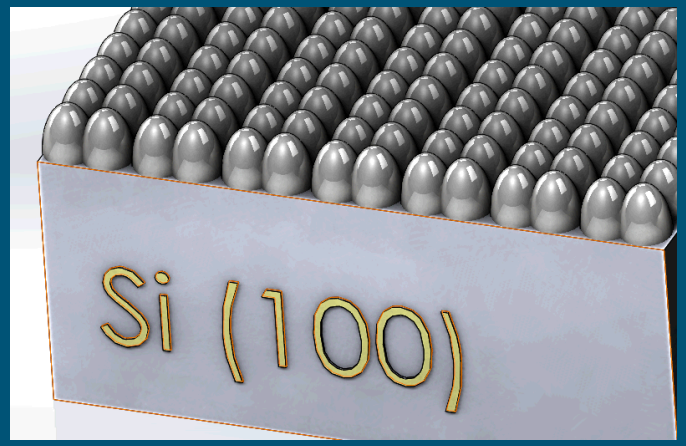
800C Bake



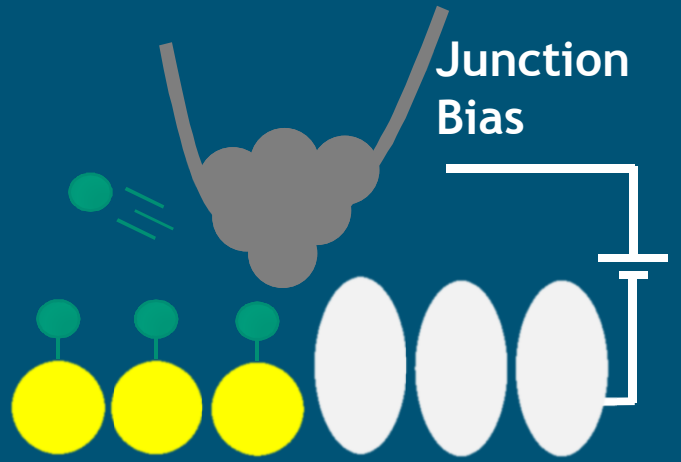
Hydrogen Terminate

Atomic Precision Fabrication

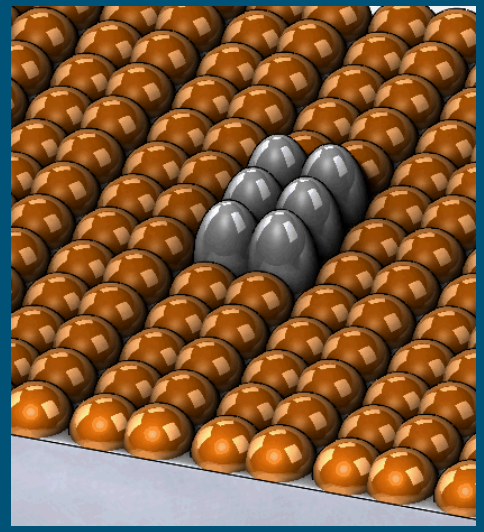
Si (100) has dangling bonds



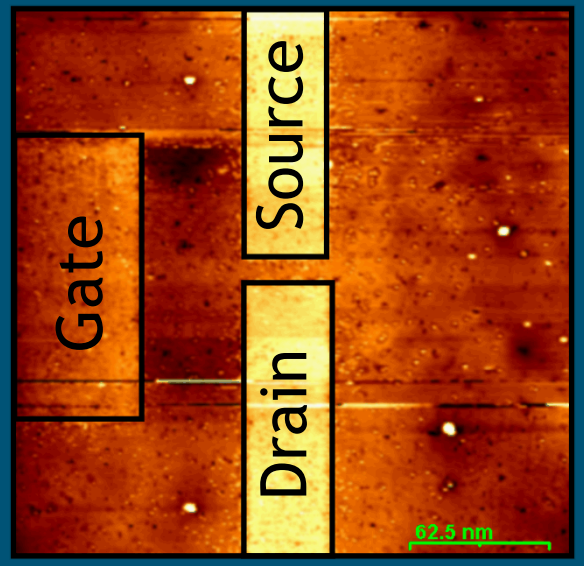
Terminate bonds with H



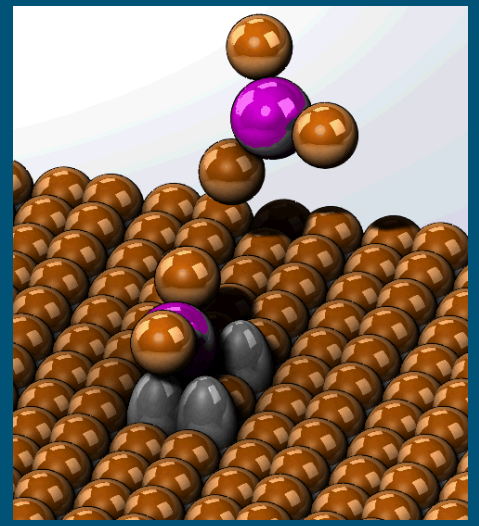
Selectively remove H



Patterned Resist



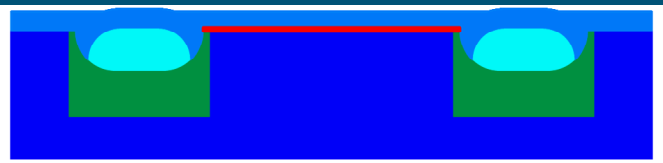
PH_3 chemistry → donor device



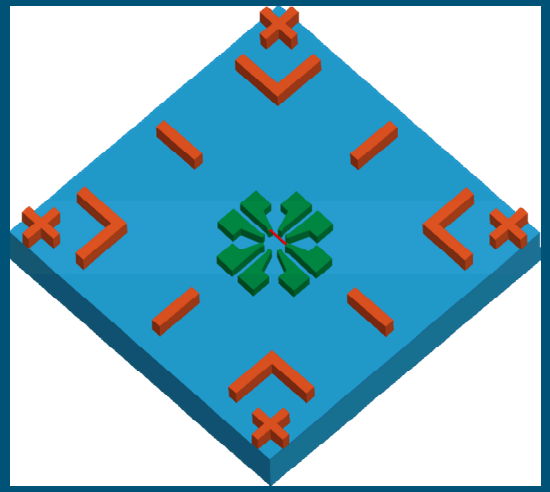
Back-end-of-line fabrication process

Si Substrate SiO_2 Epi-Si

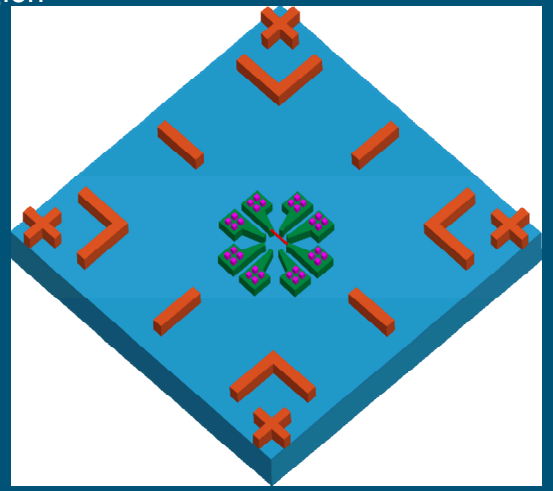
Arsenic Implant δ Layer Aluminum

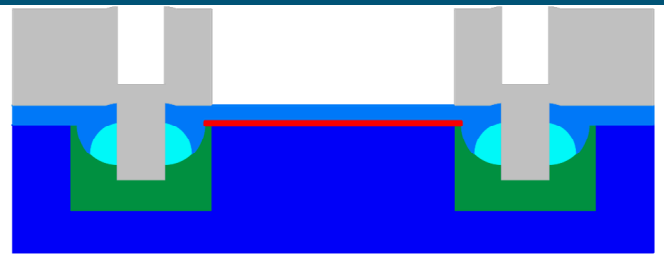


1. Device as it arrives in BEOL after STM

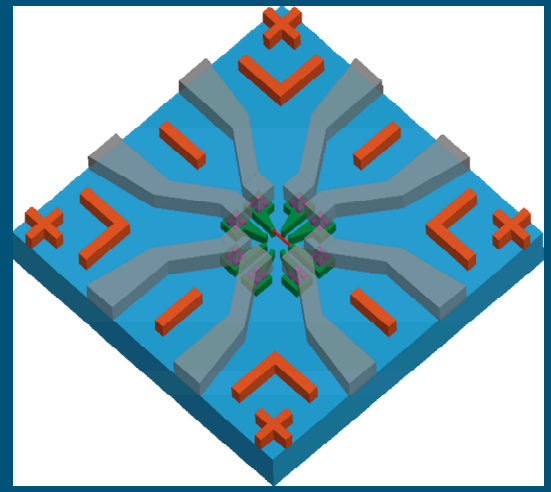


2. Vias are etched through Si Cap, remaining oxide, and into the implanted region





3. Aluminum contacts are deposited into vias and connect to macroscopic bond pads



Conclusion

Novel low temperature STM sample preparation → CMOS compatible

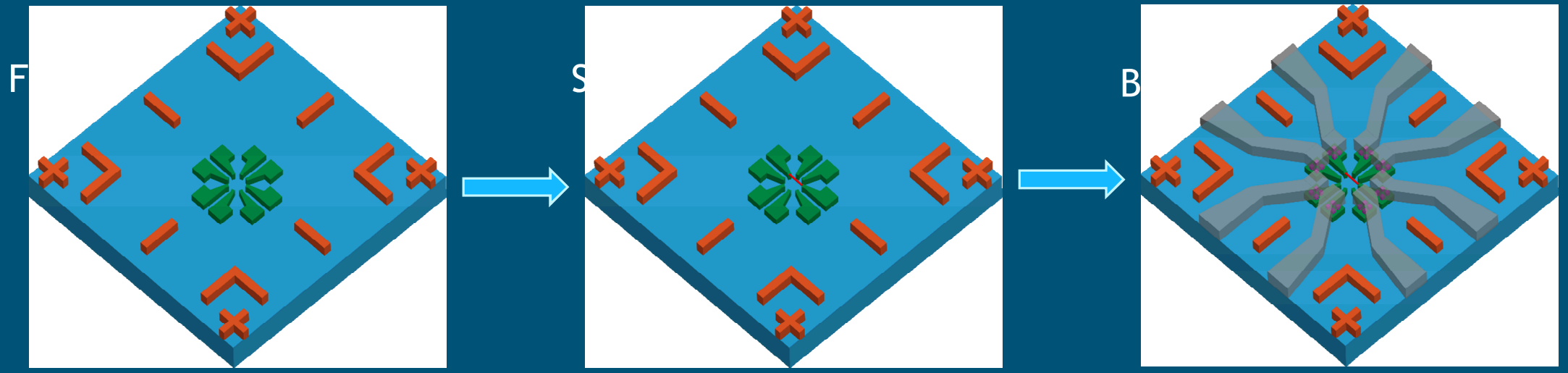
Using only contact optical lithography & CMOS compatible materials: scale from nanoscale (STM pattern) to macroscopic (bond pads)

High yield of functional device contacts: 100% of contacts on over 20 devices

Outlook:

- Different dopants
- Push limits of implant dimensions to further shrink STM device size

More details in: D. R. Ward, *et al*. App. Phys. Lett. 111, 193101 (2017).



Electrical testing of delta-layer devices in next talk