Preprint
UCRL-JC-147012

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This article was submitted to
2002 International Power Modulator Conference, Hollywood, CA.,
June 30-July 3, 2002

June 24, 2002

This work was performed under the auspices of the United States Department of Energy by the University of California, Lawrence Livermore National Laboratory under contract No. W-7405-Eng-48.

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Abstract

The ability to extract particle beam bunches from a ring accelerator in arbitrary order can greatly extend an accelerator's capabilities and applications. A prototype solid-state kicker pulser capable of generating asynchronous bursts of 50 kV pulses has been designed and tested into a 50Ω load. The pulser features fast rise and fall times and is capable of generating an arbitrary pattern of pulses with a maximum burst frequency exceeding 5 MHz If required, the pulse-width of each pulse in the burst is independently adjustable. This kicker modulator uses multiple solid-state modules stacked in an inductive-adder configuration where the energy is switched into each section of the adder by a parallel array of MOSFETs. Test data, capabilities, and limitations of the prototype pulser are described.

I. BACKGROUND

The Advanced Hydrodynamic Facility (AHF), a 50GeV proton ring accelerator currently in design at LANL, will be capable of supporting 24 bunches with a center-to-center bunch spacing of ~200ns within a ring having a revolution time of approximately 5μs. In order to fully exploit the full potential of this facility, an extraction kicker/pulser system must be capable of generating a string of pulses at arbitrary times within a total time duration of 100 microseconds or more. The complete AHF requirements for this pulser are listed in Table 1. The full range of desired pulse-train requirements cannot be reasonably met with commonly used pulse-forming cables or networks switched with thyratrons. A 20kV pulser recently designed and tested at LLNL for the DARHT kicker/pulser system has demonstrated many of the required capabilities albeit at lower voltage and with a somewhat different pulse format [1]. Before this pulser concept can be adopted for use in AHF, a working prototype that satisfies the ring accelerator pulse parameters for pulse voltage, current, rise-time, and fall-time needed to be fabricated and tested. Most of these requirements are established by the duration and spacing of bunches within the ring and a requirement that trajectory of other bunches not be affected by the extraction of a single bunch or group of consecutive bunches. The type of extraction kicker determines other pulse requirements: the current approach uses parallel-plate transmission-line kickers driven with ±50kV pulses in a push-pull mode. This kicker type was chosen because it can be designed for a fast rise time and flat impedance over a wide frequency range [2].

Table 1. AHF Pulser Performance Requirements

Parameter	Requirement
Output Voltage	50kV into 50Ω
Voltage Rise/Fall-time	≤64ns (0-100%)
Flattop Pulse-width	73ns minimum w/flatness and ripple/droop < 1.0% for each pulse and entire burst
Burst Rate	24 pulse asynchronous burst w/maximum 5MHz burst frequency
Intra-pulse voltage ripple	< 300 volts within 300ns of pulse falling edge

The kicker pulser design is based on a transformer coupled voltage-adder approach that uses MOSFET-switched capacitors to provide the primary-side drive pulse. Personnel within the Beam Research Program at LLNL had developed considerable expertise with parallel and series arrays of power MOSFETs during the successful design and testing of the Advanced Radiograph Machine (ARM) modulator, a high power pulser developed to show feasibility of solid-state modulators for driving induction accelerators [3]. After consideration of various circuit topologies and types of solid-state devices, a variation of the adder configuration used by ARM was selected as the baseline for the kicker modulator and MOSFETs were selected as the solid-state switching device. To minimize development cost for the AHF prototype, the adder design developed for DARHT was scaled to the higher voltage and current required for an AHF kicker. This approach would allow for all the AHF pulse parameters to be evaluated with the exception of the full pulse burst capability and voltage droop during the burst.

II. DEVICE EVALUATION AND SELECTION

The process for selecting the MOSFET to be used in this prototype was the same as used for selecting the device used in the DARHT kicker pulser [1]. The substantially higher current required for the AHF pulser led to the selection of APT10050LVR, a device having a 1000V maximum drain to source rating, an average current rating of 21A, and a pulsed current rating of 84A. This device is available in a standard TO-247 package from Advanced Power Technology.

During the early testing of MOSFETs, it was apparent that the MOSFET gate drive circuit was also an essential element in achieving the best performance from the

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individual devices. The coupling between the drive circuit and the MOSFET had to have very low loop inductance, as the peak drive current required to achieve fast switching performance was on the order of tens of amperes. Even the devices within the gate drive circuit had to be very fast and have short turn-on and turn-off delay times. An early decision was that each MOSFET would require its own dedicated gate drive. A simplified schematic of the drive circuit is shown in Fig. 1. The input device of the gate drive has a level shifting TTL input circuit internally coupled to a MOSFET totem pole output. This circuit drives a fast, high current MOSFET (peak current ±20 amperes) totem pole device which drives the gate of the power MOSFET (capacitive load) to turn it on and sinks current from the MOSFET to turn it off. The gate drive circuit components require a dc voltage of ~ 15 volts.

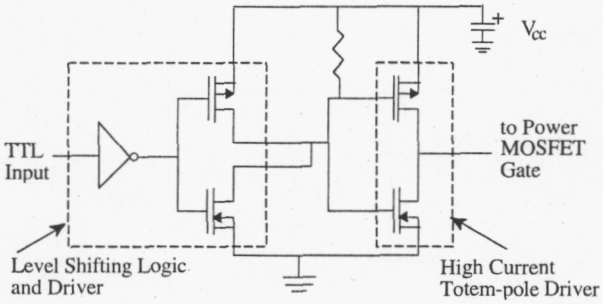

Figure 1. Simplified Schematic of MOSFET Drive

III. CIRCUIT TOPOLOGY

In the adder configuration shown in Fig. 2, the secondary windings of a number of 1:1 pulse transformers are connected in series. Typically, for fast pulse applications, both the primary and secondary winding consists of a single turn to minimize the leakage inductance. In this configuration, the output voltage on the secondary winding is the sum of all the voltages appearing on the primary windings.

In the primary-side circuit, the source impedance of the MOSFET array and the DC capacitor bank must be very low (<<1Ω) to be able to provide the total secondary current, any additional current loads in the primary circuit, plus the magnetization current for the transformer core. The layout for this circuit is critical since it is essential that total loop inductance be minimized. The MOSFETs shown in Fig. 2 have their source lead connected to ground. This is chosen so that all the gate drive circuits are also ground referenced, thereby eliminating the need for floating and isolated power supplies. The pulse power ground and the drive circuit ground have a common point at the MOSFET source connection but otherwise do not share common current paths; thereby reducing switching transients being coupled into the low-level gate drive circuits. Transient protection for the MOSFETs is provided by the series combination of snubber capacitor and diode tightly coupled to the MOSFET. Good performance of the over-voltage circuit requires a low inductance capacitor and a diode with a low forward recovery voltage.

Not shown in the simplified circuit layout is the reset circuit for the magnetic cores. The cores require reset so that they do not saturate during the pulse burst. As the adder operates with a well-defined pulse format, it is not necessary to actively reset the core between pulses. Consequently, a DC reset circuit is used and is implemented by connecting a DC power supply through a large isolation inductor to the ungrounded end of the secondary winding of the adder stack. In the interval between bursts, the reset current will reset and bias the magnetic cores.

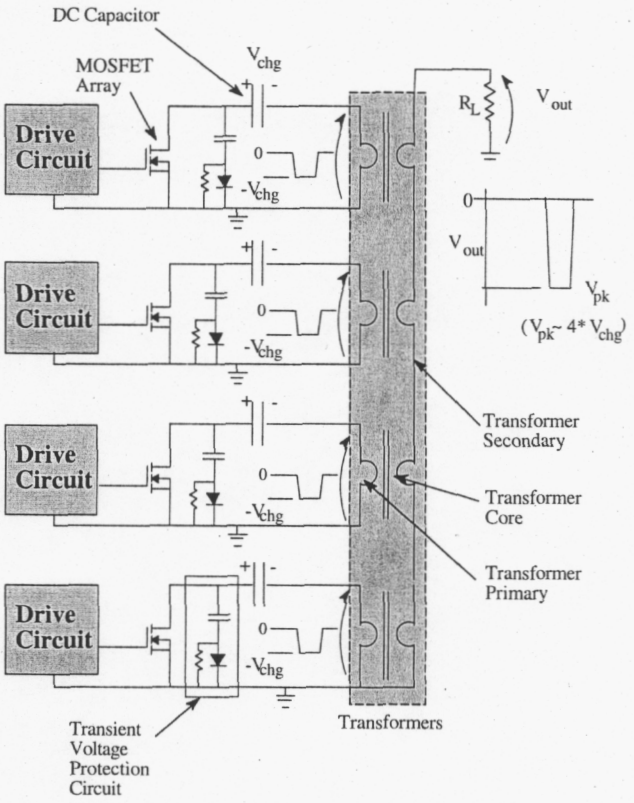

Figure 2. Simplified Schematic of Adder Circuit – Four Adder Cells Shown

IV. TRANSFORMER DESIGN AND COMPONENT LAYOUT

The adder transformer is designed to look very much like an accelerator cell of a linear induction accelerator with the primary winding totally enclosing the magnetic core (an annealed and Namlite insulated Metlgas® 2605 S1A tape-wound toroid purchased from National/Arnold). As shown in Fig. 3, the input drive connection between the transformer primary and ground has sliding contacts that make electrical connections to a printed circuit board (PCB) when the PCB is inserted between the contacts. Two boards (designated MOSFET carrier boards) are inserted into the transformer from opposite sides. Modules of this configuration are stacked (toroidal center axis vertical) to form the adder. The number of modules determines the final output voltage.

Each MOSFET carrier board consists of a distributed capacitor bank, 12 MOSFETs each with a dedicated gate drive circuit and transient protection circuits laid out such

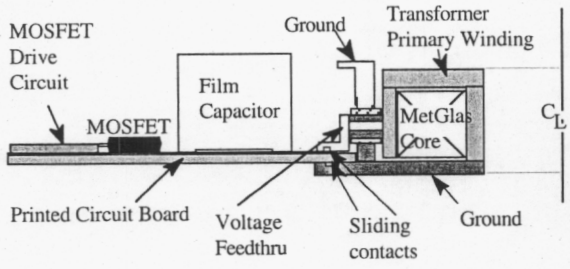

Figure 3. Simplified Cross-section of the Pulse Transformer with PCB Inserted

that the load current is uniformly shared by the switching devices. The gate drive circuit boards receive their trigger pulses from a single trigger circuit (also mounted on the MOSFET carrier board) which is connected to an external pulse generator by coaxial cable. A single carrier board plugged into a transformer assembly is show in Figure 4.

A complete prototype kicker adder assembly consisting

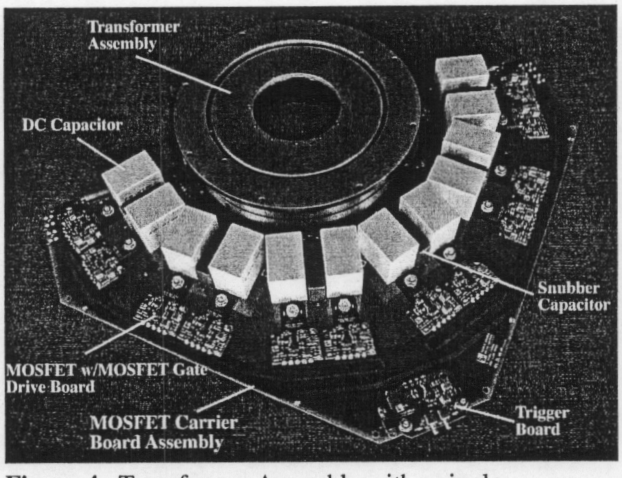

Figure 4. Transformer Assembly with a single MOSFET Carrier Board Inserted

of a stack of 75 transformer assemblies bolted together is shown in Fig. 5. The MOSFET carrier boards are shown inserted into the transformer assemblies. This modular configuration is intended to allow for easy maintenance: in the event of a component failure, the entire board can be replaced in minutes. The secondary winding for the pulser is a metal rod that is positioned on the axial centerline of the adder stack. The rod may be grounded at either end of the adder stack to generate an output voltage of either polarity. The 50Ω high-voltage output cable enters the pulser from the top of the enclosure.

V. Test Results

The prototype modulator is undergoing extensive testing into resistive loads at LLNL. The modulator has been operated at variable pulse-widths and at burst frequencies exceeding 5 MHz. All data are measurements for the pulser while driving a 50Ω load resistance.

Fig. 6 is a measurement of the load voltage where the waveshape is a five pulse, 5MHz burst. The peak load voltage is approximately 50kV. The same burst expanded

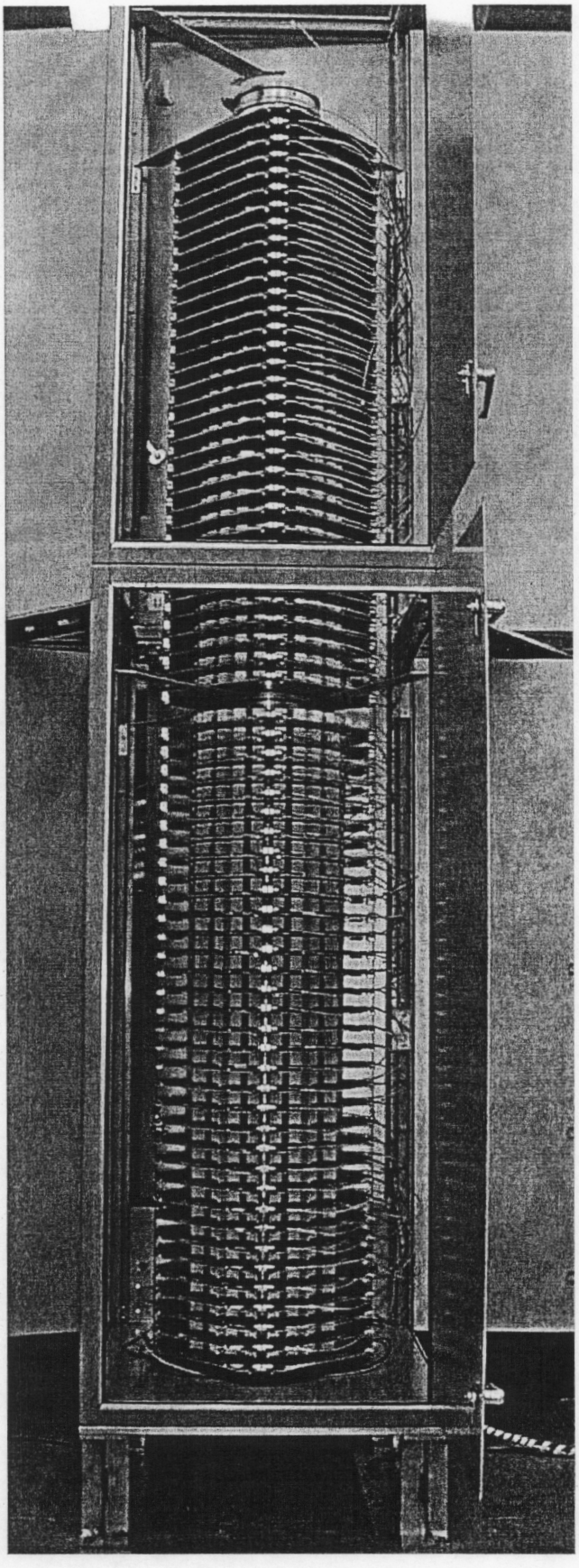

Figure 5. Complete AHF Prototype Adder Assembly

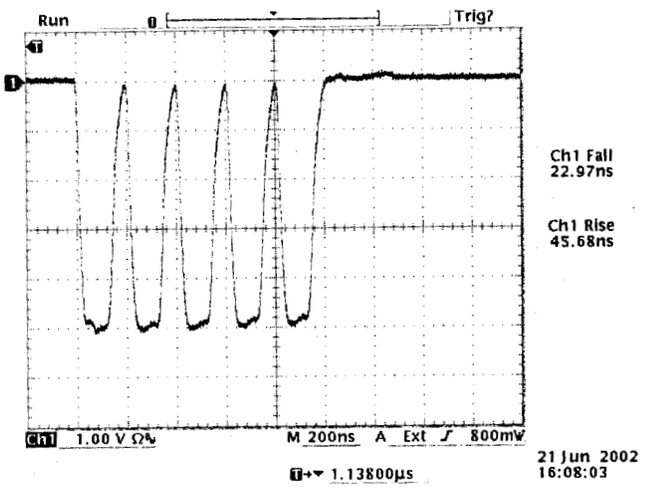

Figure 6. Load voltage at 10 kV/division – 5 Pulse, 5MHz Burst without Reset

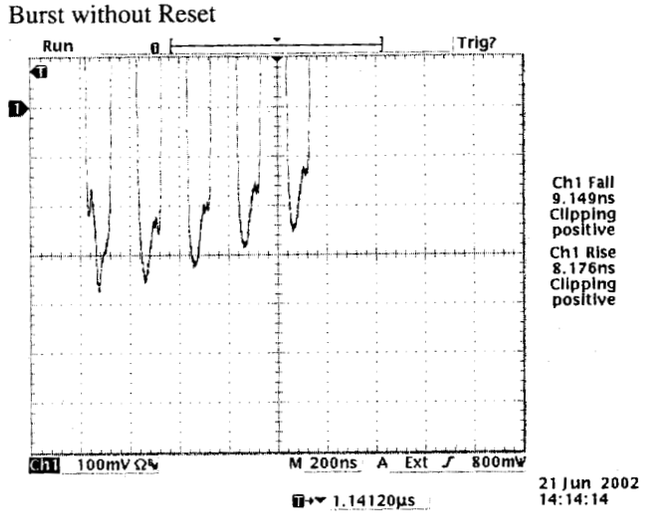

Figure 7. Load Voltage Droop at 1kV/division (2% per division) – 5Pulse, 5MHz Burst without Reset

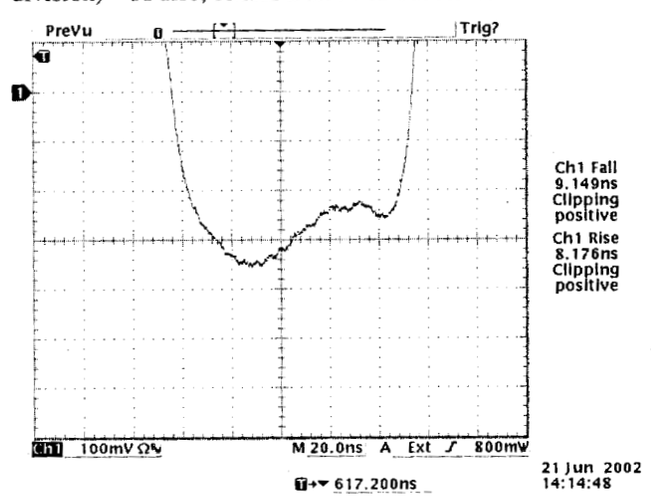

Figure 8. Load Voltage at 1kV/division (2%/div) – 2nd Pulse of 5 Pulse, 5MHz Burst without Reset

on the flattop is shown in Fig. 7 and Fig. 8. Examination of this data shows that the risetime and falltime requirements are easily met. Voltage ripple for an entire pulse is within the range of ± 1.2% with most of this ripple attributed to a slight impedance mismatch between the stalk and the output cable. The load voltage droop during the burst is due to voltage sag on the capacitor bank. Measurements have shown that reset current induces a slight oscillation in the intra-pulse period that can be eliminated by physically disconnecting the reset inductor from the adder circuit. Intra-pulse voltage after the last pulse is shown in Fig. 9. This data indicates ~400 volts is measured at the load for approximately 300ns after the last pulse at which time the voltage drops to < 100 volts.

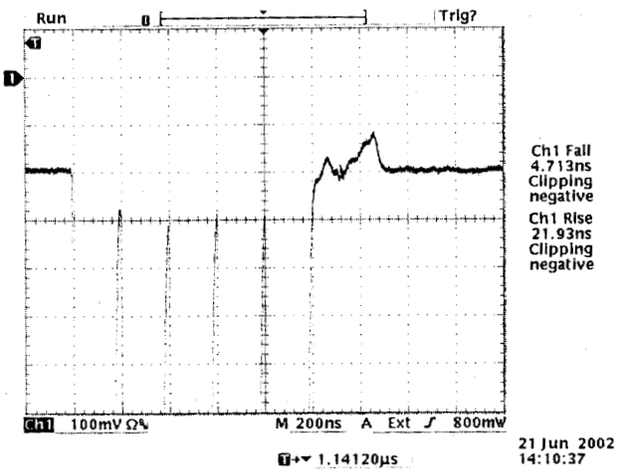

Figure 9. Intra-pulse Load Voltage at 1kV/division - 5 Pulse, 5MHz Burst without Reset

VI. CONCLUSIONS

A prototype fast kicker pulser based on MOSFET switched adder technology has been designed and tested. MOSFET arrays in an adder configuration have demonstrated the ability to generate short duration and very fast risetime and falltime high-voltage pulses. This pulser also meets most of the other requirements regarding flattop and intra-pulse voltage ripple. Voltage droop can be addressed by increasing the size of the capacitor banks on the drive boards.

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