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IEEE ITRW Materials and Devices Working Group – Position Paper

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The purpose of the International Technology Roadmap for Wide-bandgap power semiconductors (ITRW) materials and devices working group, which considers the materials science of Wide- and Ultra-Wide-Band-Gap (WBG and UWBG) semiconductors, in addition to device design, fabrication, and evaluation, is to formulate a long-term, international roadmap for WBG and UWBG materials and devices, consistent with the packaging and applications working groups of ITRW. The working group is co-chaired by Victor Veliadis (primarily representing Silicon Carbide, SiC, and related materials) and Robert Kaplar (primarily representing Gallium Nitride, GaN, and related materials) and is split into four sub-working-groups, which are:

1. SiC materials and devices (co-chairs Jon Zhang and Mietek Bakowski)
2. Lateral GaN materials and devices (co-chairs Sameh Khalil and Peter Moens)
3. Vertical GaN materials and devices (co-chairs TBD)
4. Emerging UWBG materials and devices (co-chairs TBD)

Given that the first two categories are much more mature than the latter two, and are now finding their way into applications, the focus at present is on them. Future activity will focus on the latter two sub-groups as those technologies mature. Descriptions of the first two sub-working-groups follow.

SiC Materials and Devices Sub-Working-Group

The SiC Materials and Devices sub-Working-Group (SiC-MDWG) of the ITRW is composed of members from industry and academia with specialization in SiC materials and devices. The progress in material development has had a significant impact on the roadmap for SiC devices. In addition, the device roadmap is based on application needs, and it is essential to coordinate with application groups. The goals of the SiC-MDWG are three-fold. First, it aims to identify key applications that will experience game-changing performance by adopting the appropriate SiC technology in large volume. Second, based on specific applications identified, it will highlight the device criteria that manufacturers should target so the benefits of SiC components are fully

realized in these design spaces. Third, for the long-term development in SiC devices, it will define devices that do not yet exist and will create a roadmap of what needs to be worked on to realize these devices. To accomplish these tasks, the team has identified SiC experts to provide feedback and to establish the desired characteristics of SiC components utilized in these areas. A timeline has been established to complete the first iteration, with results to follow at a conference later this year.

To facilitate the roadmap-building process, a template has been created to standardize the data that is collected for the roadmap. First, the team is documenting SiC power devices at a high level. This includes desired device types (e.g. MOSFET, JFET, IGBT, GTO, etc.) and applications, operation conditions, and required voltage and current ratings in the short-term (~5 years), medium-term (~10 years) and long-term (~15 years). The cost target in $/A is key for SiC devices to be widely adopted in power systems, and is emphasized in this section.

With the general specifications of the devices fully defined, the template turns its attention to the power devices themselves including dynamic, gate charge, and reverse diode characteristics. The purpose is to collect data on the following important device characteristics for each application in various years of development: gate driver design, followed by maximum gate-source voltage and threshold voltage, and concluding with capacitive values including input, output, and Miller capacitances. A few key parameters such as turn-on and turn-off losses and C_{oss} stored energy are included to quantify the switching losses in hard- and resonant-switching conditions, respectively. Device data on Figures Of Merit (FOMs, e.g. R_{DS_ON} vs. Q_G), body diode characteristics, and fault-tolerance capabilities (e.g. short-circuit protection time) are also collected in this section.

Since the progress in SiC materials, including substrates and epitaxy, will largely determine device cost and ultimately performance, it is critical to gather this material information for the roadmap. This is done in the section entitled “SiC Material Parameters” of the template. The data collected includes wafer area, identification of major killer defects, percentage of defect-free wafer area, minority-carrier lifetime, etc., specified for the short-, medium, and long-term time scales.

At the end of the template, a short questionnaire is included (included in the Appendix to this document) to gather additional information on the use of devices in their intended applications. Suggestions and comments on the benefits of using SiC devices in various applications, cost considerations, desired packages and modules, major barriers preventing SiC devices from gaining wide adoption, reliability status, etc., are asked for. Along with these details, the roadmap will estimate points in time when SiC devices will reach cost parity with their Si-based counterparts.

Lateral GaN Materials and Devices Sub-Working-Group

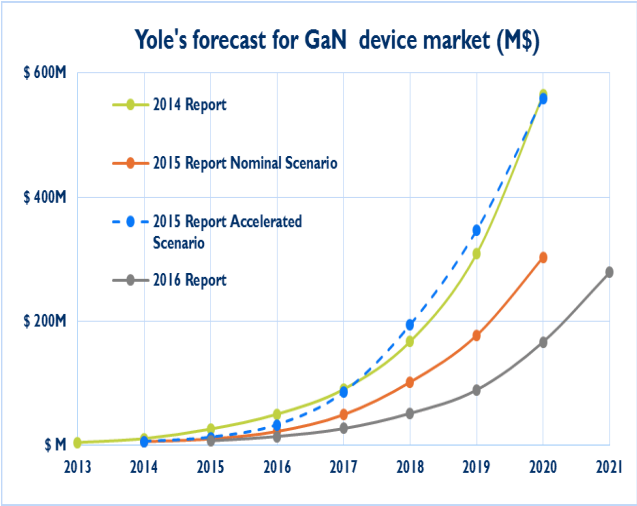

Figure 1. GaN Market Forecast [1].

The Lateral GaN Materials and Devices sub-Working-Group (L-GaN-MDWG) of the ITRW covers a similar scope as the SiC-MDWG described above, but with a focus on Lateral GaN power devices (AlGaN/GaN High Electron Mobility Transistors, HEMTs). Such devices are expected to play major role in future power electronics due to their superior intrinsic material properties as compared with the current silicon-based power devices. GaN-based Radio-Frequency (RF) devices have already demonstrated commercial success valued at more than $100M, and while GaN power device R&D efforts have nearly reached their 15-year mark, revenue forecasts have been lowered over the last few years as shown in Figure 1, signaling market penetration slower than originally projected. However, the fundamentals of the value proposition remain the same, and industry is moving forward with development efforts supported

by the emergence of several key industry-wide efforts which will help to shape a path forward with a good level of convergence, one of which is ITRW (another is an effort from JEDEC and JETTA concerning the standardization of reliability testing, qualification, parametric testing, and datasheets). These efforts will contribute to the widespread adoption of emerging GaN power electronics technologies.

This IEEE ITRW effort will address the GaN HEMT device roadmap in close collaboration with the GaN applications working group as well as the SiC-MDWG discussed above. The premise is a top-down approach where key power electronics applications and high-value markets will be identified and prioritized. They will then be matched to the specific WBG devices (either GaN or SiC). SiC devices are expected to target high-value applications with voltage ratings above 1200 V, and lateral GaN devices are expected to address high-value applications at 600 V and below. However, some overlap in the 600 to 1200 V range is likely to occur. Metrics defining the value proposition for high-value applications will drive device design, packages and modules, and circuit topologies. Example device parameters are shown in Table 1. The device specifications and reliability requirements, e.g. for consumer, industrial, or automotive markets will be assigned for the various voltage and current nodes. A questionnaire will be sent out, of similar form to the SiC questionnaire described above, to gather and distill an initial position for the roadmap for lateral GaN power devices. The targeted performance, applications, cost per Amp, efficiency, frequency, and power density, will be the basis for charting a roadmap with short-, medium-, and long-term projections for GaN power devices.

	Silicon	SiC	GaN
Concept	super junction	planar MOSFET	eMode HEMT
Blocking voltage	600V	900V	600V
On-state resistance (typ.)	56 mOhm	65 mOhm	55 mOhm
Reverse recovery charge	6000 nC	130 nC	0 nC
Energy stored in Coss @ 400V	8.1 µJ	8.8 µJ	6.4 µJ
Charge stored in Coss @ 400V	420 nC	70 nC	40 nC
Turn-off loss @ 10A / 400V	15 µJ	10 µJ	10 µJ

Table 1. Key device metrics for benchmarking power devices [2].

The L-GaN-MDWG will address various specific topics, including: Possible lateral GaN power device configurations; Gate drives; Packaging; Wafer size; Defect density; Electric field management; Reliability targets and qualification methods; Device robustness (short-circuit, UIS, ESD, etc.); and Cost per unit area for the various voltage nodes. These topics will be addressed during calendar year 2018 through team leadership formation, including recruitment of team chair and two co-chairs (complete); Recruitment of a team of experts from the field representing industry, academia, national laboratories, and government agencies (April 2018); Proposing a meeting structure and initiating working group meetings, including teleconferences and face-to-face meetings at the major conferences (APEC, ISPSD, WiPDA, IEDM, IRPS, etc.) (June 2018); Sending out a questionnaire (June 2018); Receiving feedback from the questionnaire (Sept. 2018); and Completing the initial roadmap document (Dec. 2018).

Path Forward

The team will convene at this year's Applied Power Electronics Conference (APEC 2018) to present its strategy for defining the SiC and GaN power device roadmaps. Afterwards, the topic co-chairs will assemble teams and will spend the next few months collecting data to populate the templates for their applications. Later in the year, the team will evaluate the findings and begin to write up the roadmap. It will summarize the data contained from the template and will provide supporting tables and graphs to corroborate the findings. The goal for 2018 is to complete the initial survey task, formulate a preliminary roadmap, and present the findings at an international conference late in the year.

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References

[1] Yole Annual Market Report (2016).

[2] G. Deboy et al., "Si, SiC, and GaN Power Devices: An Un-Biased View on Key Performance Indications," *in Proc*. *IEDM* (2016).

Appendix: SiC Questionnaire

SiC Devices

Device type(s): _____ Application(s): _____

Current rating (A): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Voltage rating (V): _____ (Years 1-5) _____ (Year 5-10) _____ (Years 10-15)

Operation temperature range (°C): _____

Cost target ($/A): _____ (Years 1- 5) _____ (Years 5 - 10) _____ (Years 10-15)

Preferred Device Parameters:

Maximum G-S voltage (V): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Gate threshold voltage (V): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Transconductance (S): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Input capacitance (pF): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Output capacitance (pF): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Miller capacitance (pF): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Turn-on energy (μJ): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Turn-off energy (μJ): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

C_{oss} stored energy (μJ): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

$R_{on} \cdot Q_G$ (mΩ·nC): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Body diode forward voltage (V): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Maximum dV/dt (V/ns): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Short-circuit protection time (μs): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Qualification required:

(1) Updated JEDEC for SiC: _____

(2) Updated AEC-Q101 for SiC: _____

When do you expect the SiC device for your application to reach cost parity with its Si-based counterpart? _____ years.

What is the desired lifetime of the SiC device in your application? _____ years.

SiC Material Parameters:

Substrate area (inch): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Substrate cost target ($/wafer): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Epitaxy target cost for 1200V devices ($/wafer): _____ (Years 1-5) _____ (Years 5-10) _____ (Year 10-15)

Percentage of defect-free wafer area (%): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Major killer defect(s): _____

Minority-carrier lifetime (μs): _____ (Years 1-5) _____ (Years 5-10) _____ (Years 10-15)

Suggestions and Comments:

1. What are the main benefits of using this SiC device in your application?

2. What is the desired package/module for this device?

3. What is the desired maximum temperature, T_{max}, for the package?

4. What is the desired thermal impedance, R_{th}?

5. What is the desired maximum stray inductance L_s?

6. What is the desired maximum t_{on} and t_{off}?

7. What is the biggest application in which your device will be adopted in the next 1-5 years?

8. What barriers must be overcome for your SiC device to reach cost-parity with its Si counterpart?

9. In how many years do you expect your SiC device to commercially replace its Si counterpart?

10. What is presently the biggest factor limiting wide commercial adoption of your device (choose one)?
a. cost
b. reliability
c. workforce educated in its use and benefits

11. What device information do you need from SiC power electronics users?

12. What device information do you need from SiC material suppliers?